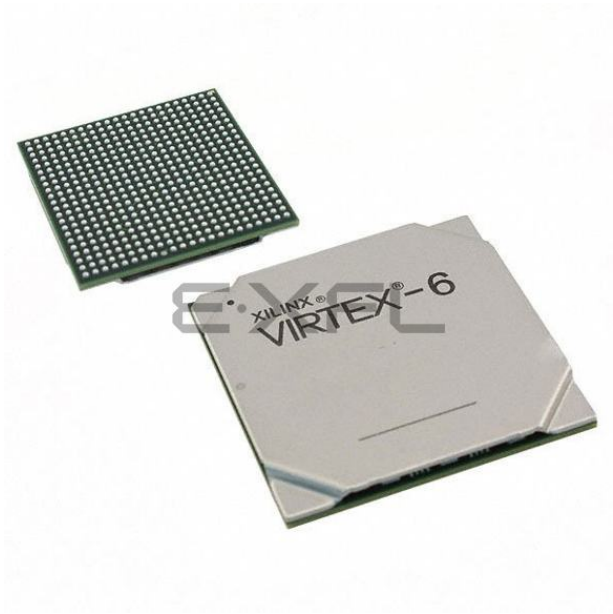
AMD Xilinx - XC6VCX75T-2FFG784I Datasheet



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5820
Number of Logic Elements/Cells	74496
Total RAM Bits	5750784
Number of I/O	360
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	784-BBGA, FCBGA
Supplier Device Package	784-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vcx75t-2ffg784i

Virtex-6 CXT FPGA Documentation

In addition to the data sheet information found herein, complete and up-to-date documentation of the Virtex-6 family of FPGAs is available on the Xilinx website and available for download:

Virtex-6 FPGA Configuration Guide **(UG360)**

This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.

Virtex-6 FPGA SelectIO Resources User Guide **(UG361)**

This guide describes the SelectIO™ resources available in all the Virtex-6 CXT devices.

Virtex-6 FPGA Clocking Resources User Guide **(UG362)**

This guide describes the clocking resources available in all the Virtex-6 CXT devices, including the MMCM and clock buffers.

Virtex-6 FPGA Memory Resources User Guide **(UG363)**

This guide describes the Virtex-6 CXT device block RAM and FIFO capabilities.

Virtex-6 FPGA CLB User Guide **(UG364)**

This guide describes the capabilities of the configurable logic blocks (CLB) available in all Virtex-6 CXT devices.

Virtex-6 FPGA DSP48E1 Slice User Guide **(UG369)**

This guide describes the architecture of the DSP48E1 slice in Virtex-6 CXT FPGAs and provides configuration examples.

Virtex-6 FPGA GTX Transceivers User Guide **(UG366)**

This guide describes the GTX transceivers available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Tri-Mode Ethernet MAC User Guide **(UG368)**

This guide describes the dedicated tri-mode Ethernet media access controller (TEMAC) available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Data Sheet: DC and Switching Characteristics **(DS152)**

Reference this data sheet when considering device migration to the Virtex-6 LXT and SXT families. It contains the DC and Switching Characteristic specifications specifically for the Virtex-6 LXT and SXT families.

Virtex-6 FPGA Packaging and Pinout Specifications **(UG365)**

These specifications includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications of the Virtex-6 LXT and SXT families. Reference these specifications when considering device migration to the Virtex-6 LXT and SXT families.

Configuration Bitstream Overview for CXT Devices

This section contains two tables similar to those in the *Virtex-6 FPGA Configuration Guide* only updated for the CXT family. The Virtex-6 CXT FPGA bitstream contains commands to the FPGA configuration logic as well as configuration data. Table 3 gives a typical bitstream length and Table 4 gives the specific device ID codes for the Virtex-6 CXT devices.

Table 3: **Virtex-6 CXT FPGA Bitstream Length**

Device	Total Number of Configuration Bits
XC6VCX75T	26,239,328
XC6VCX130T	43,719,776
XC6VCX195T	61,552,736
XC6VCX240T	73,859,552

Table 4: **Virtex-6 CXT FPGA Device ID Codes**

Device	ID Code (Hex)
XC6VCX75T	0x042C4093
XC6VCX130T	0x042CA093
XC6VCX195T	0x042CC093
XC6VCX240T	0x042D0093

CLB Overview for CXT Devices

Table 5, updated specifically for the CXT family from a similar table in the *Virtex-6 FPGA CLB User Guide*, shows the available resources in all Virtex-6 CXT FPGA CLBs.

Table 5: **Virtex-6 CXT FPGA Logic Resources Available in All CLBs**

Device	Total Slices	SLICELs	SLICEMs	Number of 6-Input LUTs	Maximum Distributed RAM (Kb)	Shift Register (Kb)	Number of Flip-Flops
XC6VCX75T	11,640	7,460	4,180	46,560	1045	522.5	93,120
XC6VCX130T	20,000	13,040	6,960	80,000	1740	870	160,000
XC6VCX195T	31,200	19,040	12,160	124,800	3140	1570	249,600
XC6VCX240T	37,680	23,080	14,600	150,720	3770	1885	301,440

Regional Clock Management for CXT Devices

Table 6, updated from the *Virtex-6 FPGA Clocking Resources User Guide* specifically for the CXT family, shows the number of clock regions in all Virtex-6 CXT FPGA CLBs.

Table 6: **Virtex-6 CXT FPGA Clock Regions**

Device	Number of Clock Regions
XC6VCX75T	6
XC6VCX130T	10
XC6VCX195T	10
XC6VCX240T	12

CXT Packaging Specifications

Table 7, updated from the *Virtex-6 FPGA Packaging and Pinout Specifications* specifically for the CXT family, shows the number of GTX transceiver I/O channels. Table 8 shows the number of available I/Os and the number of differential I/O pairs for each Virtex-6 device/package combination.

Table 7: **Number of Serial Transceivers (GTs) I/O Channels/Device**

I/O Channels	Device			
	CX75T(1)	CX130T(2)	CX195T(3)	CX240T(4)
MGTRXP	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTRXN	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTTXP	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTTXN	8 or 12	8, 12, or 16	12 or 16	12 or 16

Notes:

1. The XC6VCX75T has 8 GTX I/O channels in the FF484/FFG484 package and 12 GTX I/O channels in the FF784/FFG784 package.
2. The XC6VCX130T has 8 GTX I/O channels in the FF484/FFG484 package, 12 GTX I/O channels in the FF784/FFG784 package, and 16 GTX I/O channels in the FF1156/FFG1156 package.
3. The XC6VCX195T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.
4. The XC6VCX240T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.

FF484 Package Placement Diagrams

Figure 2 and Figure 3 show the placement diagrams for the GTX transceivers in the FF484 package.

Note: Unbonded locations in the FF484 package are:

- CX75T: X0Y8, X0Y9, X0Y10, X0Y11
- CX130T: X0Y0, X0Y1, X0Y2, X0Y3, and X0Y12, X0Y13, X0Y14, X0Y15

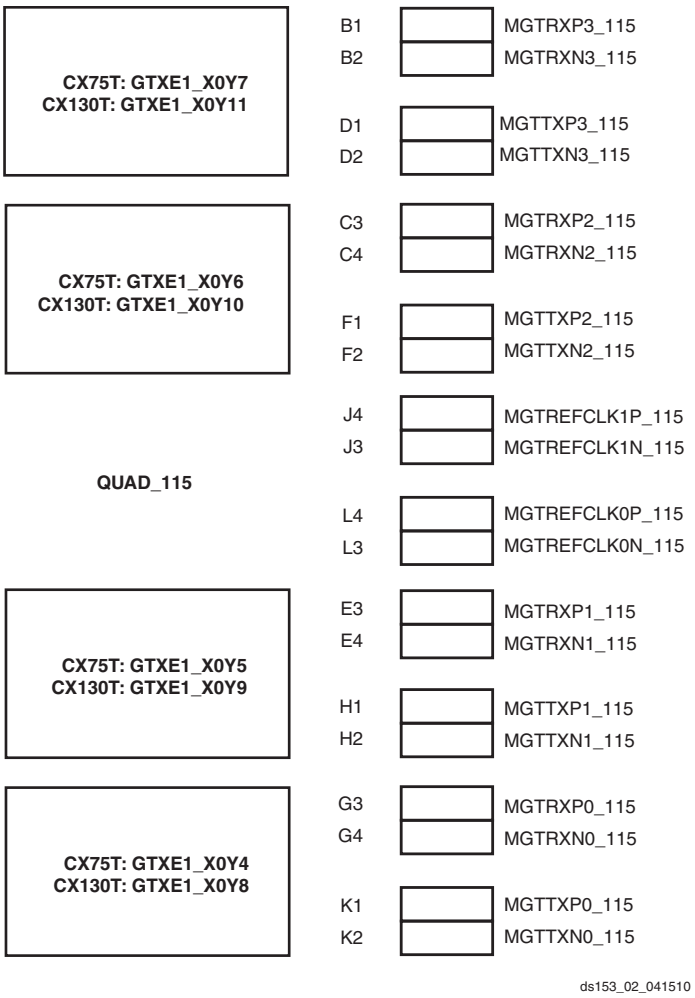

Figure 2: **Placement Diagram for the FF484 Package (1 of 2)**

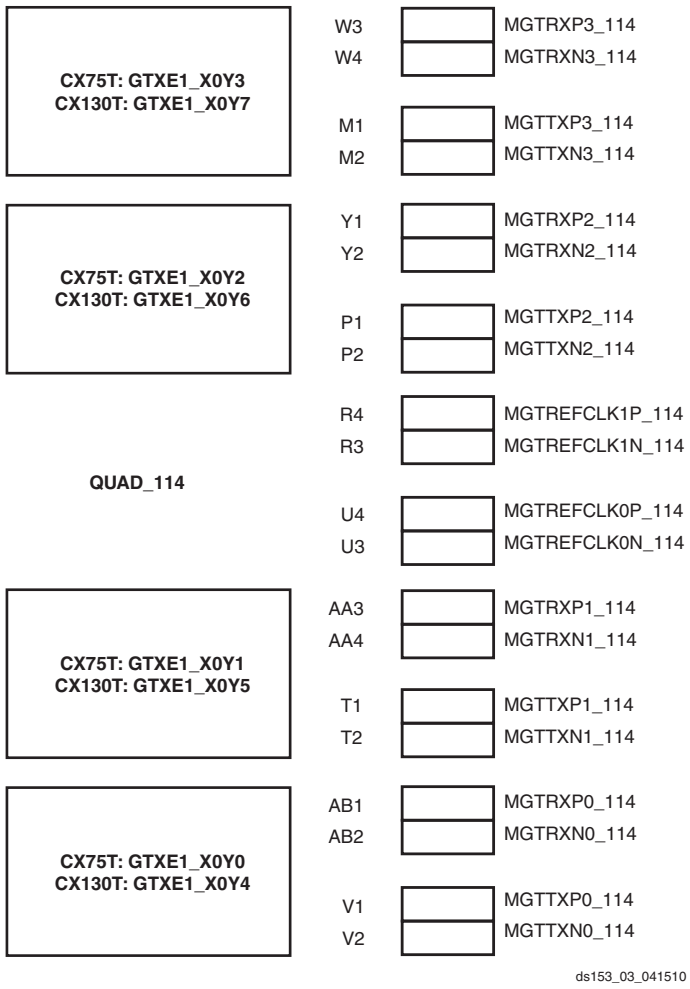

Figure 3: **Placement Diagram for the FF484 Package (2 of 2)**

FF1156 Package Placement Diagrams

Figure 7 through Figure 10 show the placement diagrams for the GTX transceivers in the FF1156 package.

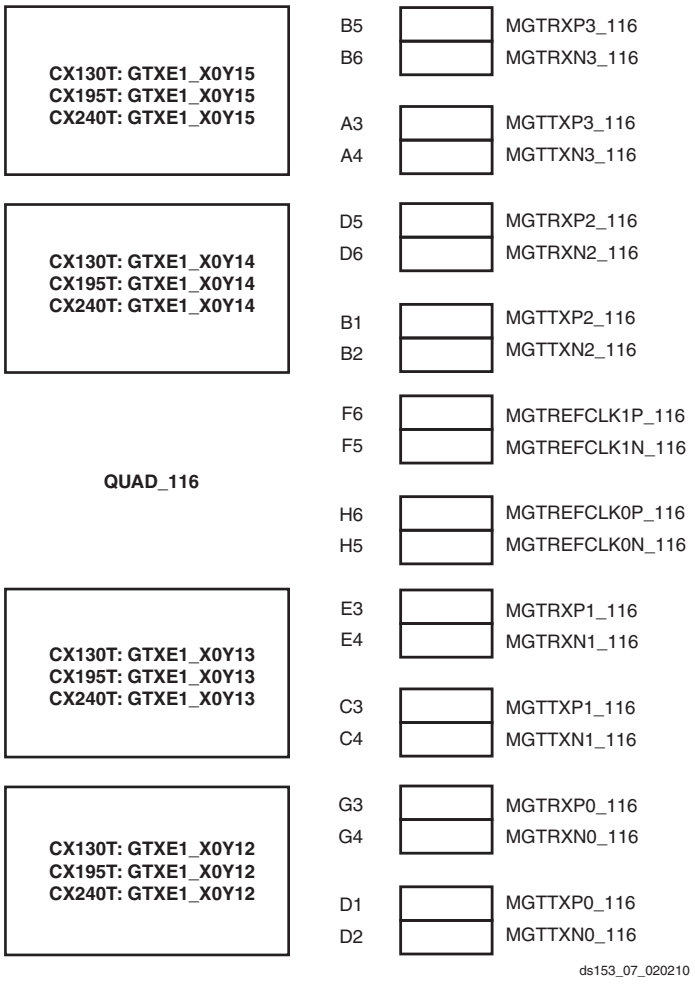

Figure 7: **Placement Diagram for the FF1156 Package (1 of 4)**

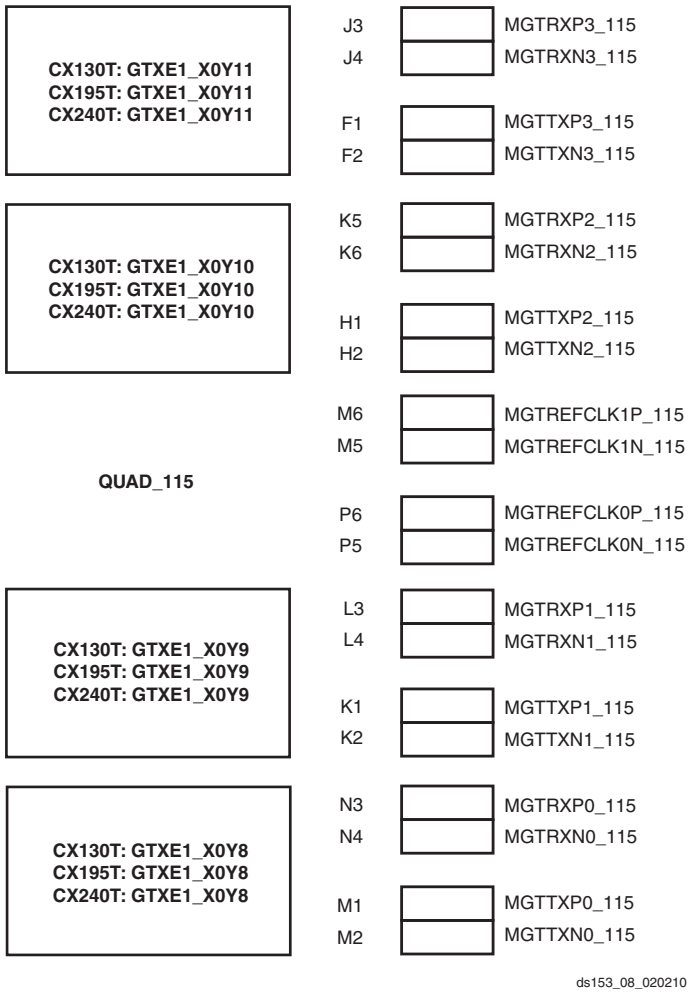

Figure 8: **Placement Diagram for the FF1156 Package (2 of 4)**

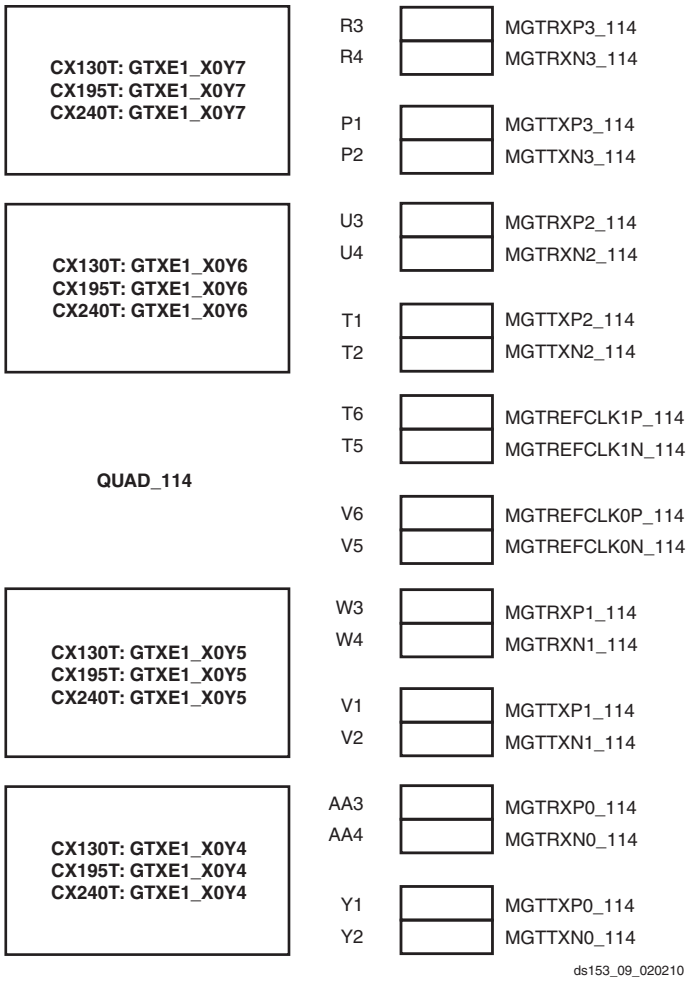

Figure 9: **Placement Diagram for the FF1156 Package (3 of 4)**

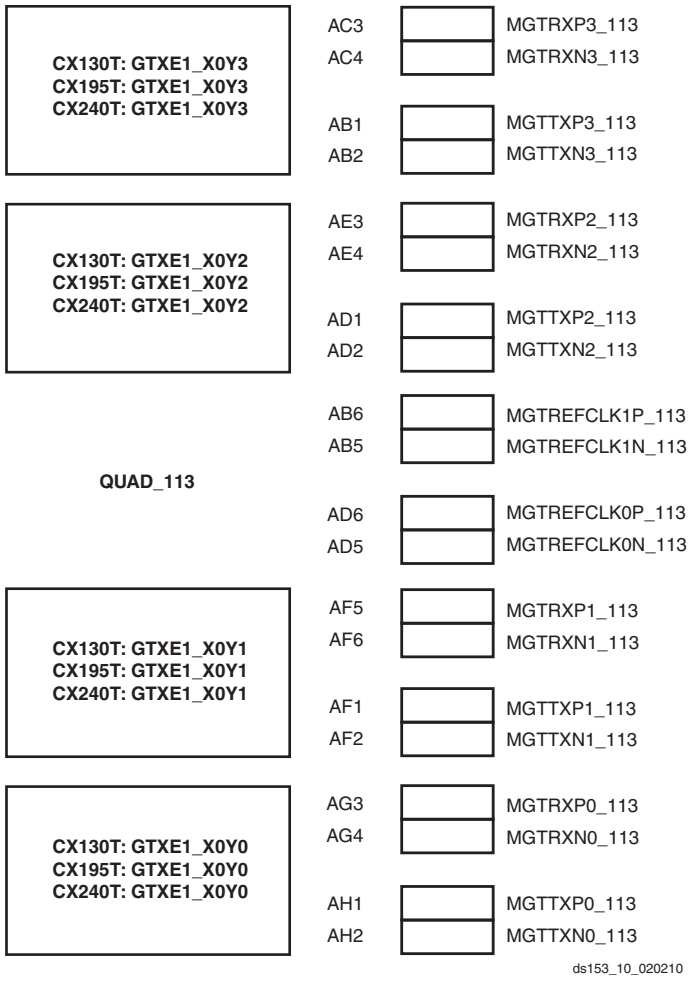

Figure 10: **Placement Diagram for the FF1156 Package (4 of 4)**

Table 10: **Recommended Operating Conditions**

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_j = 0°C to +85°C	0.95	1.05	V
	Internal supply voltage relative to GND, T_j = –40°C to +100°C	0.95	1.05	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_j = 0°C to +85°C	2.375	2.625	V
	Auxiliary supply voltage relative to GND, T_j = –40°C to +100°C	2.375	2.625	V
V_{CCO}(1)(2)(3)	Supply voltage relative to GND, T_j = 0°C to +85°C	1.14	2.625	V
	Supply voltage relative to GND, T_j = –40°C to +100°C	1.14	2.625	V
V_{IN}	2.5V supply voltage relative to GND, T_j = 0°C to +85°C	GND – 0.20	2.625	V
	2.5V supply voltage relative to GND, T_j = –40°C to +100°C	GND – 0.20	2.625	V
	2.5V and below supply voltage relative to GND, T_j = 0°C to +85°C	GND – 0.20	V_{CCO} + 0.2	V
	2.5V and below supply voltage relative to GND, T_j = –40°C to +100°C	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}(4)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
V_{BATT}(5)	Battery voltage relative to GND, T_j = 0°C to +85°C	1.0	2.5	V
	Battery voltage relative to GND, T_j = –40°C to +100°C	1.0	2.5	V
V_{FS}(6)	External voltage supply for eFUSE programming	2.375	2.625	V

Notes:

1. Configuration data is retained even if V_{CCO} drops to 0V.
2. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
3. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}.
4. A total of 100 mA per bank should not be exceeded.
5. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
6. When not programming eFUSE, connect V_{FS} to GND.
7. All voltages are relative to ground.

Table 11: **DC Characteristics Over Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	10	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	10	µA
C_{IN}(3)	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	20	–	80	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	8	–	40	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	5	–	30	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	1	–	20	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 2.5V	3	–	80	µA
I_{BATT}	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

Virtex-6 CXT devices require a power-on sequence of V_{CCINT}, V_{CCAUX}, and V_{CCO}. If the requirement can not be met, then V_{CCAUX} must always be powered prior to V_{CCO}. V_{CCAUX} and V_{CCO} can be powered by the same supply, therefore, both V_{CCAUX} and V_{CCO} are permitted to ramp simultaneously. Similarly, for the power-down sequence, V_{CCO} must be powered down prior to V_{CCAUX} or if powered by the same supply, V_{CCAUX} and V_{CCO} power-down simultaneously.

Table 13 shows the minimum current, in addition to I_{CCQ}, that are required by Virtex-6 CXT devices for proper power-on and configuration. If the current minimums shown in Table 12 and Table 13 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 13: **Power-On Current for Virtex-6 CXT Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ(1)	Typ(1)	Typ(1)	
XC6VCX75T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VCX130T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VCX195T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VCX240T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

Table 14: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 15: **SelectIO DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(5)	Note(5)
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
DIFF HSTL I(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 I	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
SSTL15	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	V_{TT} – 0.175	V_{TT} + 0.175	14.3	14.3

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 22: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	0.95	1.0	1.06	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.14	1.2	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 23: **GTX Transceiver Supply Current (per Lane) (1)(2)**

Symbol	Description	Typ	Max	Units
$I_{MGTAVTT}$	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
$I_{MGTAVCC}$	MGTAVCC supply current for one GTX transceiver	56.1		mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 24: **GTX Transceiver Quiescent Supply Current (per Lane)(1)(2)(3)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVTTQ}$	Quiescent MGTAVTT supply current for one GTX transceiver	0.9	Note 2	mA
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

Table 30: **GTX Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
T_{RX}	RXUSRCLK maximum frequency		234.38	234.38	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz
T_{TX}	TXUSRCLK maximum frequency		234.38	234.38	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz

Notes:

1. Clocking must be implemented as described in *Virtex-6 FPGA GTX Transceivers User Guide*.

Table 31: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.480	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	120	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	75	ns
$T_{J3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.34	UI
$D_{J3.75}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J3.125}$	Total Jitter(2)(3)	3.125 Gb/s	–	–	0.2	UI
$D_{J3.125}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$T_{J3.125L}$	Total Jitter(2)(3)	3.125 Gb/s(4)	–	–	0.35	UI
$D_{J3.125L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J2.5}$	Total Jitter(2)(3)	2.5 Gb/s(5)	–	–	0.20	UI
$D_{J2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$T_{J1.25}$	Total Jitter(2)(3)	1.25 Gb/s(6)	–	–	0.15	UI
$D_{J1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
T_{J600}	Total Jitter(2)(3)	600 Mb/s	–	–	0.1	UI
D_{J600}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Ethernet MAC Switching Characteristics

Consult *Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide* for further information.

Table 33: **Maximum Ethernet MAC Performance**

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
$F_{TEMACCLIENT}$	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5(1)	2.5(1)	MHz
		100 Mb/s – 8-bit width	25(2)	25(2)	MHz
		1000 Mb/s – 8-bit width	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	MHz
$F_{TEMACPHY}$	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 34: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency	125	125	MHz
$F_{USERCLK}$	User clock maximum frequency	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	MHz

Switching Characteristics

All values represented in this data sheet are based on the speed specification (version 1.08). Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 36 correlates the current status of each Virtex-6 CXT device on a per speed grade basis.

Table 36: **Virtex-6 CXT Device/Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VCX75T			-2, -1
XC6VCX130T			-2, -1
XC6VCX195T			-2, -1
XC6VCX240T			-2, -1

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 CXT devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 37 lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE® software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 37: **Virtex-6 CXT Device/Production Software and Speed Specification Release**

Device	Speed Grade Designations	
	-2	-1
XC6VCX75T	ISE 12.2 (with speed file patch) v1.06	
XC6VCX130T	ISE 12.1 v1.04	
XC6VCX195T	ISE 12.2 (with speed file patch) v1.06	
XC6VCX240T	ISE 12.1 v1.04	

Notes:

1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

IOB Pad Input/Output/3-State Switching Characteristics

Table 38 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 39 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 38: **IOB Switching Characteristics**

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVDS_25	1.09	1.09	1.68	1.68	1.68	1.68	ns
LVDSEXT_25	1.09	1.09	1.84	1.84	1.84	1.84	ns
HT_25	1.09	1.09	1.78	1.78	1.78	1.78	ns
BLVDS_25	1.09	1.09	1.67	1.67	1.67	1.67	ns
RSDS_25 (point to point)	1.09	1.09	1.68	1.68	1.68	1.68	ns
HSTL_I	1.06	1.06	1.73	1.73	1.73	1.73	ns
HSTL_II	1.06	1.06	1.74	1.74	1.74	1.74	ns
HSTL_III	1.06	1.06	1.71	1.71	1.71	1.71	ns
HSTL_I_18	1.06	1.06	1.75	1.75	1.75	1.75	ns
HSTL_II_18	1.06	1.06	1.81	1.81	1.81	1.81	ns
HSTL_III_18	1.06	1.06	1.71	1.71	1.71	1.71	ns
SSTL2_I	1.06	1.06	1.77	1.77	1.77	1.77	ns
SSTL2_II	1.06	1.06	1.72	1.72	1.72	1.72	ns
SSTL15	1.06	1.06	1.71	1.71	1.71	1.71	ns
LVCMOS25, Slow, 2 mA	0.66	0.66	6.01	6.01	6.01	6.01	ns
LVCMOS25, Slow, 4 mA	0.66	0.66	3.79	3.79	3.79	3.79	ns
LVCMOS25, Slow, 6 mA	0.66	0.66	3.08	3.08	3.08	3.08	ns
LVCMOS25, Slow, 8 mA	0.66	0.66	2.72	2.72	2.72	2.72	ns
LVCMOS25, Slow, 12 mA	0.66	0.66	2.17	2.17	2.17	2.17	ns
LVCMOS25, Slow, 16 mA	0.66	0.66	2.29	2.29	2.29	2.29	ns
LVCMOS25, Slow, 24 mA	0.66	0.66	2.02	2.02	2.02	2.02	ns
LVCMOS25, Fast, 2 mA	0.66	0.66	6.04	6.04	6.04	6.04	ns
LVCMOS25, Fast, 4 mA	0.66	0.66	3.82	3.82	3.82	3.82	ns
LVCMOS25, Fast, 6 mA	0.66	0.66	2.99	2.99	2.99	2.99	ns
LVCMOS25, Fast, 8 mA	0.66	0.66	2.65	2.65	2.65	2.65	ns
LVCMOS25, Fast, 12 mA	0.66	0.66	2.08	2.08	2.08	2.08	ns
LVCMOS25, Fast, 16 mA	0.66	0.66	2.13	2.13	2.13	2.13	ns
LVCMOS25, Fast, 24 mA	0.66	0.66	1.99	1.99	1.99	1.99	ns

Table 38: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
DIFF_SSTL18_II_T_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL15	1.06	1.06	1.71	1.71	1.71	1.71	ns
DIFF_SSTL15_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
DIFF_SSTL15_T_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns

Table 39: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{IOTPHZ}	T input to Pad high-impedance	0.99	0.99	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 40 shows the test setup parameters used for measuring input delay.

Table 40: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III	HSTL_III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
HT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 14.
6. The value given is the differential output voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 14 and Figure 15.

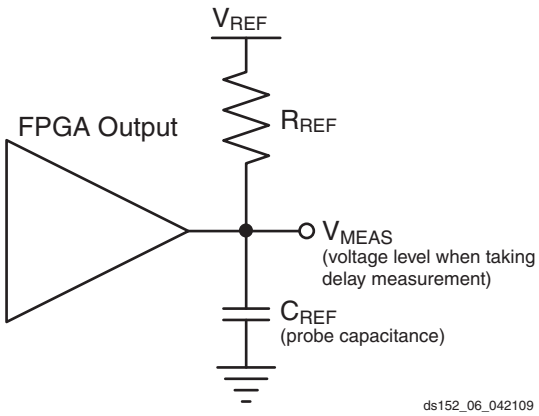

Figure 14: **Single Ended Test Setup**

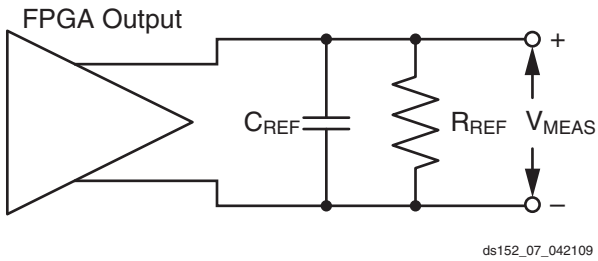

Figure 15: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 41.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 41: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0 (2)	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0 (2)	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0 (2)	0

Table 43: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.54/–0.11	0.54/–0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.22/–0.05	0.22/–0.05	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.71/–0.29	0.71/–0.29	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.56/–0.10	0.56/–0.10	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.21/–0.05	0.21/–0.05	ns
Combinatorial				
T_{DOQ}	D1 to OQ out or T1 to TQ out	1.01	1.01	ns
Sequential Delays				
T_{OCKQ}	CLK to OQ/TQ out	0.71	0.71	ns
T_{RQ}	SR pin to OQ/TQ out	1.05	1.05	ns
T_{GSRQ}	Global Set/Reset to Q outputs	10.51	10.51	ns
Set/Reset				
T_{RPW}	Minimum Pulse Width, SR inputs	1.20	1.20	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 44: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold for Control Lines				
$T_{ISCCK\_BITSLIP}/T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.09/0.17	0.09/0.17	ns
$T_{ISCCK\_CE}/T_{ISCKC\_CE}$ (2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.27/0.04	0.27/0.04	ns
$T_{ISCCK\_CE2}/T_{ISCKC\_CE2}$ (2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	–0.06/0.31	–0.06/0.31	ns
Setup/Hold for Data Lines				
T_{ISDCK_D}/T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.09/0.11	0.09/0.11	ns
$T_{ISDCK\_DDLY}/T_{ISCKD\_DDLY}$	DDLY pin Setup/Hold with respect to CLK (using IODELAY) (1)	0.14/0.07	0.14/0.07	ns
$T_{ISDCK\_D\_DDR}/T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	0.09/0.11	0.09/0.11	ns
$T_{ISDCK\_DDLY\_DDR}$ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) (1)	0.14/0.07	0.14/0.07	ns
Sequential Delays				
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.75	0.75	ns
Propagation Delays				
T_{ISDO_DO}	D input to DO output pin	0.25	0.25	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as $T_{ISCCK\_CE}/T_{ISCKC\_CE}$ in a TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 45: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.31/–0.12	0.31/–0.12	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.56/–0.08	0.56/–0.08	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.31/–0.08	0.31/–0.08	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.22/–0.05	0.22/–0.05	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.07	0.07	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.21/–0.05	0.21/–0.05	ns
Sequential Delays				
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.82	0.82	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.82	0.82	ns
Combinatorial				
T_{OSDO_TTQ}	T input to TQ Out	0.97	0.97	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the TRACE report.

Table 51: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Combinatorial Delays from Input Pins to Cascading Output Pins				
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.65	0.75	ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.24	6.03	ns
$T_{DSPDO\_D\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.94	5.68	ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.19	2.52	ns
$T_{DSPDO\_\_\{C, CARRYIN\}\_\{PCOUT, CARRYCASCOUT,MULTSIGNOUT\}}$	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.95	2.25	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins				
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT\}\_MULT}$	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	4.97	5.72	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT}$	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.92	2.21	ns
$T_{DSPDO\_\{ACIN; BCIN\}\_\{ACOUT; BCOUT\}}$	{ACIN, BCIN} input to {ACOUT, BCOUT} output	0.49	0.57	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.10	5.86	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.05	2.35	ns
$T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_ \{P, CARRYOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.60	1.83	ns
$T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_ \{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.72	1.98	ns
Clock to Outs from Output Register Clock to Output Pins				
$T_{DSPCKO\_\{P, CARRYOUT\}\_PREG}$	CLK (PREG) to {P, CARRYOUT} output	0.50	0.57	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_PREG}$	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.50	0.66	ns
Clock to Outs from Pipeline Register Clock to Output Pins				
$T_{DSPCKO\_\{P, CARRYOUT\}\_MREG}$	CLK (MREG) to {P, CARRYOUT} output	2.30	2.65	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MREG}$	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.43	2.79	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_ADREG\_MULT}$	CLK (ADREG) to {P, CARRYOUT} output	3.72	4.72	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_ADREG\_MULT}$	CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	3.84	4.42	ns
Clock to Outs from Input Register Clock to Output Pins				
$T_{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	5.36	6.16	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	2.27	2.61	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_CREG}$	CLK (CREG) to {P, CARRYOUT} output	2.27	2.61	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_DREG\_MULT}$	CLK (DREG) to {P, CARRYOUT} output	5.25	6.04	ns

Table 57: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs(3)	0.12	0.12	ns
$T_{OUTJITTER}$	MMCM Output Jitter(4)	Note 1		
$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision(5)	0.20	0.20	ns
$T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	µs
F_{OUTMAX}	MMCM Maximum Output Frequency	700	700	MHz
F_{OUTMIN}	MMCM Minimum Output Frequency(6)(7)	4.69	4.69	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max		
$RST_{MINPULSE}$	Minimum Reset Pulse Width	1.5	1.5	ns
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized(8)	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	135	135	MHz
	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	10.00	10.00	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle		
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and Hold of Phase Shift Enable	1.04/0.00	1.04/0.00	ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.38	0.38	ns

Notes:

1. When DIVCLK_DIVIDE = 3 or 4, F_{INMAX} is 315 MHz.
2. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
3. The static offset is measured between any MMCM outputs with identical phase.
4. Values for this parameter are available in the Architecture Wizard.
5. Includes global clock buffer.
6. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
7. When CASCADE4_OUT = TRUE, F_{OUTMIN} is 0.036 MHz.
8. In ISE software 12.3 (or earlier versions supporting the Virtex-6 family), the phase frequency detector Optimized bandwidth setting is equivalent to the High bandwidth setting. Starting with ISE software 12.4, the Optimized bandwidth setting is automatically adjusted to Low when the software can determine that the phase frequency detector input is less than 135 MHz.

Virtex-6 CXT Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 61. Values are expressed in nanoseconds unless otherwise noted.

Table 61: **Global Clock Input Setup and Hold Without MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM	XC6VCX75T	1.75/–0.01	1.75/–0.01	ns
		XC6VCX130T	1.88/–0.11	1.88/–0.11	ns
		XC6VCX195T	1.97/–0.14	1.97/–0.14	ns
		XC6VCX240T	1.97/–0.14	1.97/–0.14	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 62: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMGC}$/ $T_{PHMMCMGC}$	No Delay Global Clock Input and IFF(2) with MMCM	XC6VCX75T	1.72/–0.22	1.72/–0.22	ns
		XC6VCX130T	1.81/–0.21	1.81/–0.21	ns
		XC6VCX195T	1.82/–0.20	1.82/–0.20	ns
		XC6VCX240T	1.82/–0.20	1.82/–0.20	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 63: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay Clock-capable Clock Input and IFF(2) with MMCM	XC6VCX75T	1.86/–0.28	1.86/–0.28	ns
		XC6VCX130T	1.93/–0.28	1.93/–0.28	ns
		XC6VCX195T	1.96/–0.27	1.96/–0.27	ns
		XC6VCX240T	1.96/–0.27	1.96/–0.27	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.