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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

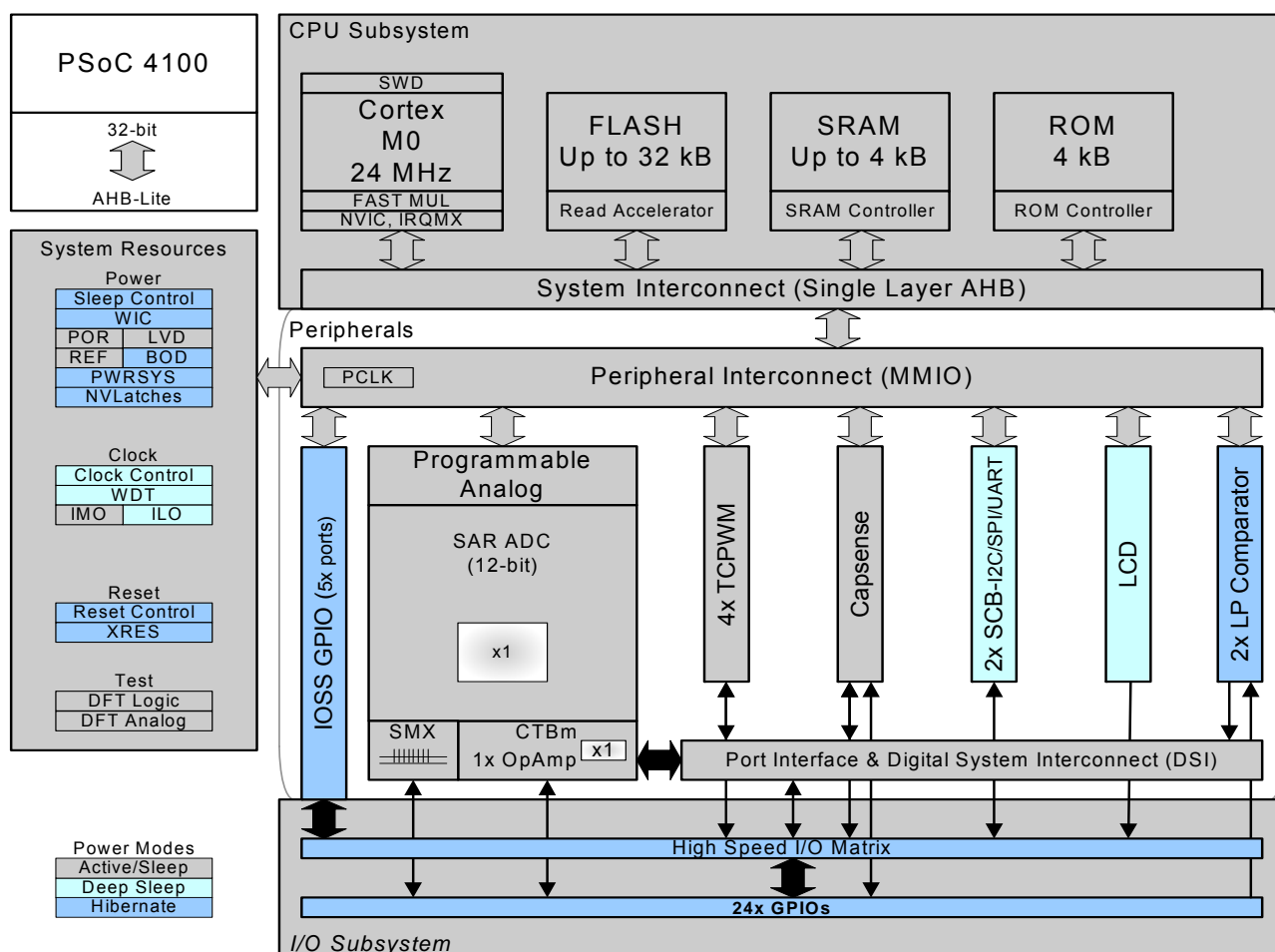
#### Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4124pva-442t">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4124pva-442t</a>

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## Block Diagram



## Functional Description

PSoC 4100 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial\_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 4100 devices. The SWD interface is fully compatible with industry standard third party tools. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip

programmable blocks, the PSoC 4100 family provides a level of security not possible with multi-chip application solutions or with microcontrollers.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4100 with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4100 allows the customer to make.

## Functional Overview

### CPU and Memory Subsystem

#### CPU

The Cortex-M0 CPU in PSoC 4100 is part of the 32-bit MCU subsystem, which is optimized for low power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from Deep Sleep mode allowing power to be switched off to the main processor when the chip is in Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt input (NMI), which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the Serial Wire Debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4100 has four break-point (address) comparators and two watchpoint (data) comparators.

#### Flash

PSoC 4100 has a flash module with a flash accelerator tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 0 wait-state (WS) access time at 24 MHz. Part of the flash module can be used to emulate EEPROM operation if required.

The PSoC 4100 flash supports the following flash protection modes at the memory sub-system level.

**Open:** No protection. Factory default mode that the product is shipped in.

**Protected:** User may change from Open to Protected. This mode disables debug interface accesses. The mode can be set back to Open but only after completely erasing the flash.

**Kill:** User may change from Open to Kill. This mode disables all debug accesses. The part cannot be erased externally, thus obviating the possibility of partial erasure by power interruption and potential malfunction and security leaks. This is an irrevocable mode.

In addition, row-level Read/Write protection is also supported to prevent inadvertent Writes as well as selectively block Reads. Flash Read/Write/Erase operations are always available for internal code using system calls.

#### SRAM

SRAM memory is retained during Hibernate.

#### SROM

A supervisory ROM that contains boot and configuration routines is provided.

## System Resources

### Power System

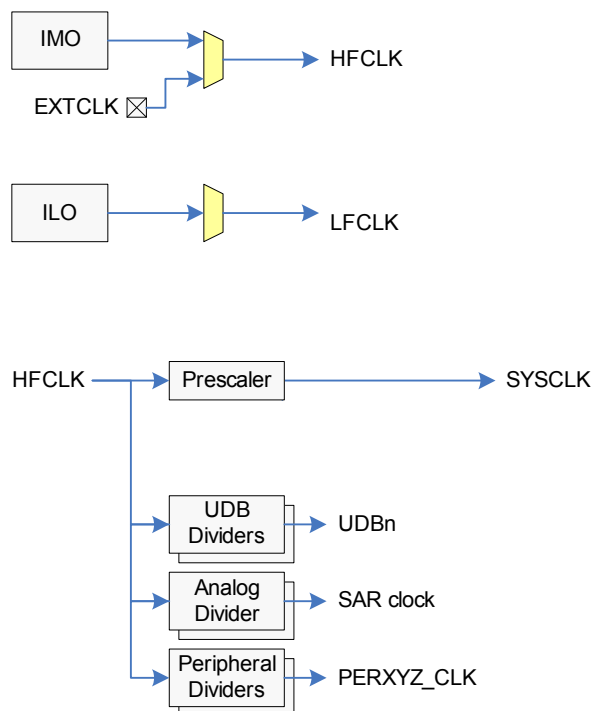
The power system is described in detail in the section [Power on page 10](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low-voltage detect (LVD)). The PSoC 4100 operates with a single external supply over the range of 1.71 V to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4100 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

### Clock System

The PSoC 4100 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for the PSoC 4100 consists of two internal oscillators, IMO and the ILO, and provision for an external clock.

**Figure 1. PSoC 4100 MCU Clocking Architecture**



The HFCLK signal can be divided down (see [PSoC 4100 MCU Clocking Architecture](#)) to generate synchronous clocks for the analog and digital peripherals. There are a total of 12 clock dividers for the PSoC 4100, each with 16-bit divide capability. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

### IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 MHz to 24 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is  $\pm 2\%$ .

### ILO Clock Source

The ILO is a very low power oscillator, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

### Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

### Reset

PSoC 4100 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the Reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

### Voltage Reference

The PSoC 4100 reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or to use an external reference for the SAR.

## Analog Blocks

### 12-bit SAR ADC

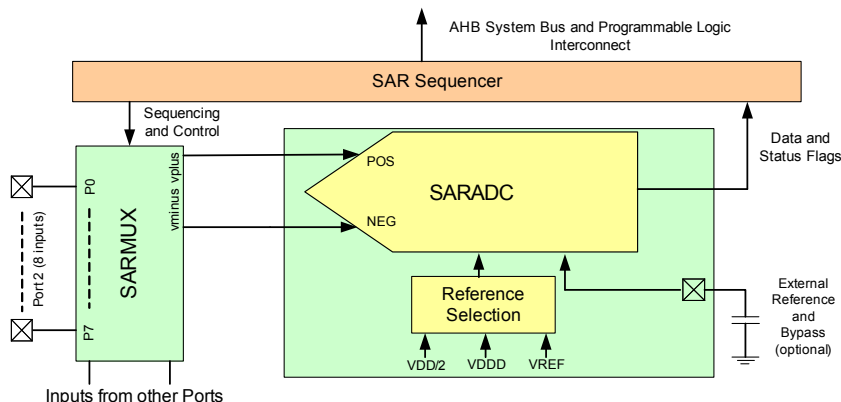
The 12-bit 806 Ksps SAR ADC can operate at a maximum clock rate of 14.5 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to  $\pm 1\%$ ) and by providing the choice (for the PSoC 4100 case) of three internal voltage references:  $V_{DD}$ ,  $V_{DD}/2$ , and  $V_{REF}$  (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision providing appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, aggregate sampling bandwidth is equal to 806 Ksps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

**Figure 2. SAR ADC System Diagram**





## Opamp (CTBm Block)

PSoC 4100 has an opamp with Comparator mode, which allows most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamp is designed with enough bandwidth to drive the S/H circuit of the ADC without requiring external buffering.

## Temperature Sensor

PSoC 4100 has one on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress supplied software that includes calibration and linearization.

## Low-power Comparators

PSoC 4100 has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

## Fixed Function Digital

### Timer/Counter/PWM Block

The Timer/Counter/PWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

### Serial Communication Blocks (SCB)

PSoC 4100 has two SCBs, which can each implement an I<sup>2</sup>C, UART, SPI, or LIN Slave interface.

**I<sup>2</sup>C Mode:** The hardware I<sup>2</sup>C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I<sup>2</sup>C peripheral is compatible with the I<sup>2</sup>C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus

I/O is implemented with GPIO in open-drain modes. The I<sup>2</sup>C bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. Required Rise and Fall times for different I<sup>2</sup>C speeds are guaranteed by using appropriate pull-up resistor values depending on V<sub>DD</sub>, Bus Capacitance, and resistor tolerance. For detailed information on how to calculate the optimum pull-up resistor value for your design, please refer to the UM10204 I<sup>2</sup>C bus specification and user manual, the newest revision is available at [www.nxp.com](http://www.nxp.com).

The PSoC 4100 is not completely compliant with the I<sup>2</sup>C spec in the following respects:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I<sup>2</sup>C system.
- Fast-mode Plus has an I<sub>OL</sub> specification of 20 mA at a V<sub>OL</sub> of 0.4 V. The GPIO cells can sink a maximum of 8 mA I<sub>OL</sub> with a V<sub>OL</sub> maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I<sup>2</sup>C Master, it interposes an IDLE state between NACK and Repeated Start; the I<sup>2</sup>C spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in I<sup>2</sup>C Slave mode, and Address Match on External Clock is enabled (EC\_AM = 1) along with operation in the internally clocked mode (EC\_OP = 0), then its I<sup>2</sup>C address must be even.

**UART Mode:** This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

**SPI Mode:** The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and also supports an EzSPI mode in which data interchange is reduced to reading and writing an array in memory.

**LIN Slave Mode:** The LIN Slave mode uses the SCB hardware block and implements a full LIN slave interface. This LIN slave is compliant with LIN v1.3 and LIN v2.1/2.2 specification standards. It is certified by C&S GmbH based on the standard protocol and data link layer conformance tests. The LIN slave can be operated at baud rates of up to ~20 Kbps with a maximum of 40-meter cable length. PSoC Creator software supports up to two LIN slave interfaces in the PSoC 4 device, providing built-in application programming interfaces (APIs) based on the LIN specification standard.

### GPIO

PSoC 4100 has 24 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100).

### Special Function Peripherals

#### LCD Segment Drive

The PSoC 4100 has an LCD controller which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

#### CapSense

CapSense is supported on all pins in the PSoC 4100 through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used. (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

## Pinouts

The following is the pin-list for PSoC 4100. Port 2 comprises of the high-speed Analog inputs for the SAR Mux. P1.7 is the optional external input and bypass for the SAR reference. Ports 3 and 4 contain the Digital Communication channels. All pins support CSD CapSense and Analog Mux Bus connections.

Pins		28-SSOP		Alternate Functions for Pins					Pin Description
Name	Type	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
VSSD	Power	DN	–	–	–	–	–	–	Digital Ground
P2.2	GPIO	5	P2.2	sarmux.2	–	–	–	–	Port 2 Pin 2: gpio, lcd, csd, sarmux
P2.3	GPIO	6	P2.3	sarmux.3	–	–	–	–	Port 2 Pin 3: gpio, lcd, csd, sarmux
P2.4	GPIO	7	P2.4	sarmux.4	tcpwm0_p[1]	–	–	–	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm
P2.5	GPIO	8	P2.5	sarmux.5	tcpwm0_n[1]	–	–	–	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm
P2.6	GPIO	9	P2.6	sarmux.6	tcpwm1_p[1]	–	–	–	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm
P2.7	GPIO	10	P2.7	sarmux.7	tcpwm1_n[1]	–	–	–	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm
P3.0	GPIO	11	P3.0	–	tcpwm0_p[0]	scb1_uart_rx[0]	scb1_i2c_scl[0]	scb1_spi_mosi[0]	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1
P3.1	GPIO	12	P3.1	–	tcpwm0_n[0]	scb1_uart_tx[0]	scb1_i2c_sda[0]	scb1_spi_miso[0]	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1
P3.2	GPIO	13	P3.2	–	tcpwm1_p[0]	–	swd_io	scb1_spi_clk[0]	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd
P3.3	GPIO	14	P3.3	–	tcpwm1_n[0]	–	swd_clk	scb1_spi_ssel_0[0]	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd
P4.0	GPIO	15	P4.0	–	–	scb0_uart_rx	scb0_i2c_scl	scb0_spi_mosi	Port 4 Pin 0: gpio, lcd, csd, scb0
P4.1	GPIO	16	P4.1	–	–	scb0_uart_tx	scb0_i2c_sda	scb0_spi_miso	Port 4 Pin 1: gpio, lcd, csd, scb0
P4.2	GPIO	17	P4.2	csd_c_mod	–	–	–	scb0_spi_clk	Port 4 Pin 2: gpio, lcd, csd, scb0
P4.3	GPIO	18	P4.3	csd_c_sh_tan_k	–	–	–	scb0_spi_ssel_0	Port 4 Pin 3: gpio, lcd, csd, scb0
P0.0	GPIO	19	P0.0	comp1_inp	–	–	–	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
P0.1	GPIO	20	P0.1	comp1_inn	–	–	–	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
P0.2	GPIO	21	P0.2	comp2_inp	–	–	–	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
P0.3	GPIO	22	P0.3	comp2_inn	–	–	–	–	Port 0 Pin 3: gpio, lcd, csd, comp
P0.6	GPIO	23	P0.6	–	ext_clk	–	–	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
P0.7	GPIO	24	P0.7	–	–	–	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup
XRES	XRES	25	XRES	–	–	–	–	–	Chip reset, active low
VCCD	Power	26	VCCD	–	–	–	–	–	Regulated supply, connect to 1 µF cap or 1.8 V
VDDD	Power	27	VDDD	–	–	–	–	–	Common power supply (Analog & Digital) 1.8 V–5.5 V
VSSA	Power	28(DN)	VSS	–	–	–	–	–	Analog Ground
P1.0	GPIO	1	P1.0	ctb.oa0.inp	tcpwm2_p[1]	–	–	–	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
P1.1	GPIO	2	P1.1	ctb.oa0.inm	tcpwm2_n[1]	–	–	–	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm
P1.2	GPIO	3	P1.2	ctb.oa0.out	tcpwm3_p[1]	–	–	–	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm
P1.7	GPIO	4	P1.7	ctb.oa1.inp_a lt_ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

### Notes:

1. tcpwm\_p and tcpwm\_n refer to tcpwm non-inverted and inverted outputs respectively.
2. P3.2 and P3.3 are SWD pins after boot (reset).

**Descriptions of the pin functions are as follows:**

**VDDD:** Power supply for both analog and digital sections (where there is no  $V_{DDA}$  pin).



**VDDA:** Analog  $V_{DD}$  pin where package pins allow; shorted to  $V_{DDD}$  otherwise.

**VSSA:** Analog ground pin where package pins allow; shorted to VSS otherwise

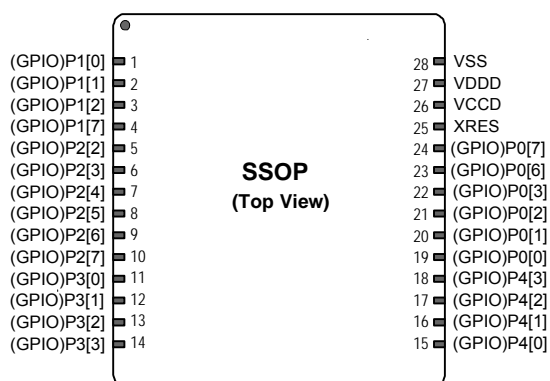
**VSS:** Ground pin.

**VCCD:** Regulated Digital supply (1.8 V  $\pm 5\%$ ).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

The following package is supported: 28-pin SSOP.

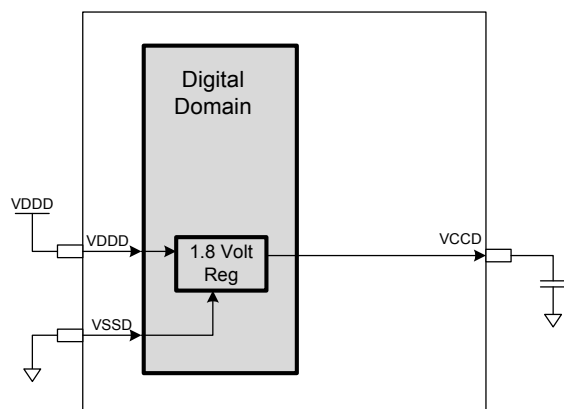
**Figure 3. 28-pin SSOP pinout**



## Power

The following power system diagram shows the minimum set of power supply pins as implemented for the PSoC 4100. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the  $V_{DDA}$  input. There are separate regulators for the Deep Sleep and Hibernate (lowered power supply and retention) modes. There is a separate low-noise regulator for the bandgap. The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

**Figure 4. PSoC 4 Power Supply**



The PSoC 4100 family allows two distinct modes of power supply operation: Unregulated External Supply, and Regulated External Supply modes.

### Unregulated External Supply

In this mode, PSoC 4100 is powered by an External Power Supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4100 supplies the internal logic and the VCCD output of the PSoC 4100 must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6  $\mu\text{F}$ ; X5R ceramic or better).

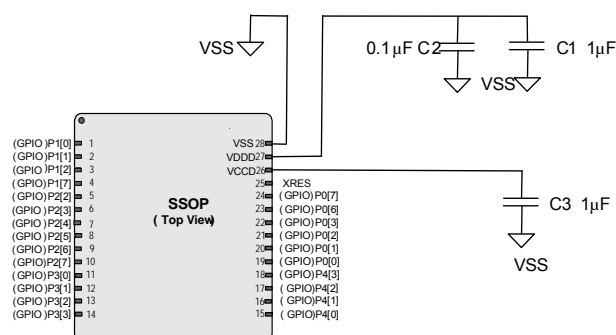
Bypass capacitors must be used from VDDD to ground, typical practice for systems in this frequency range is to use a capacitor in the 1- $\mu\text{F}$  range in parallel with a smaller capacitor (0.1  $\mu\text{F}$  for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme for the 28-pin SSOP package follows.

**Table 1. Example of a bypass scheme**

Power Supply	Bypass Capacitors
VDDD–VSS	0.1 $\mu\text{F}$ ceramic capacitor (C2) plus bulk capacitor 1 to 10 $\mu\text{F}$ (C1). Total Capacitance may be greater than 10 $\mu\text{F}$ .
VCCD–VSS	1 $\mu\text{F}$ ceramic capacitor at the VCCD pin (C3)
VREF–VSS (optional)	The internal bandgap may be bypassed with a 1 $\mu\text{F}$ to 10 $\mu\text{F}$ capacitor. Total capacitance may be greater than 10 $\mu\text{F}$ .

**Figure 5. 28-Pin SSOP Example**



### Regulated External Supply

In this mode, the PSoC 4100 is powered by an external power supply that must be within the range of 1.71 to 1.89 V ( $1.8 \pm 5\%$ ); note that this range needs to include power supply ripple too. In this mode, VCCD, and VDDD pins are all shorted together and bypassed. The internal regulator is disabled in firmware.

## Development Support

The PSoC 4100 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit [www.cypress.com/go/psoc4](http://www.cypress.com/go/psoc4) to find out more.

### Documentation

A suite of documentation supports the PSoC 4100 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide:** A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets:** The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes:** PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual:** The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at [www.cypress.com/psoc4](http://www.cypress.com/psoc4).

### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100 family is part of a development tool ecosystem. Visit us at [www.cypress.com/go/psoccreator](http://www.cypress.com/go/psoccreator) for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

**Table 3. DC Specifications** *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Sleep Mode, V <sub>DD</sub> = 1.7 V to 5.5 V							
SID25	I <sub>DD20</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on. 6 MHz.	–	1.3	1.8	mA	V <sub>DD</sub> = 1.71 V to 5.5 V
SID25A	I <sub>DD20A</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on. 12 MHz.	–	1.7	2.2	mA	V <sub>DD</sub> = 1.71 V to 5.5 V
Deep Sleep Mode, V <sub>DD</sub> = 1.8 V to 3.6 V (Regulator on)							
SID31	I <sub>DD26</sub>	I <sup>2</sup> C wakeup and WDT on.	–	1.3	–	μA	T = 25 °C
SID32	I <sub>DD27</sub>	I <sup>2</sup> C wakeup and WDT on.	–	–	45	μA	T = 85 °C
Deep Sleep Mode, V <sub>DD</sub> = 3.6 V to 5.5 V							
SID34	I <sub>DD29</sub>	I <sup>2</sup> C wakeup and WDT on	–	1.5	15	μA	Typ. at 25 °C Max at 85 °C
Deep Sleep Mode, V <sub>DD</sub> = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	I <sub>DD32</sub>	I <sup>2</sup> C wakeup and WDT on.	–	1.7	–	μA	T = 25 °C
SID38	I <sub>DD33</sub>	I <sup>2</sup> C wakeup and WDT on	–	–	60	μA	T = 85 °C
Deep Sleep Mode, +105 °C							
SID33Q	I <sub>DD28Q</sub>	I <sup>2</sup> C wakeup and WDT on. Regulator Off.	–	–	135	μA	V <sub>DD</sub> = 1.71 V to 1.89 V
SID34Q	I <sub>DD29Q</sub>	I <sup>2</sup> C wakeup and WDT on.	–	–	180	μA	V <sub>DD</sub> = 1.8 V to 3.6 V
SID35Q	I <sub>DD30Q</sub>	I <sup>2</sup> C wakeup and WDT on.	–	–	140	μA	V <sub>DD</sub> = 3.6 V to 5.5 V
Hibernate Mode, V <sub>DD</sub> = 1.8 V to 3.6 V (Regulator on)							
SID40	I <sub>DD35</sub>	GPIO & Reset active	–	150	–	nA	T = 25 °C
SID41	I <sub>DD36</sub>	GPIO & Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, V <sub>DD</sub> = 3.6 V to 5.5 V							
SID43	I <sub>DD38</sub>	GPIO & Reset active	–	150	–	nA	T = 25 °C
Hibernate Mode, V <sub>DD</sub> = 1.71 V to 1.89 V (Regulator bypassed)							
SID46	I <sub>DD41</sub>	GPIO & Reset active	–	150	–	nA	T = 25 °C
SID47	I <sub>DD42</sub>	GPIO & Reset active	–	–	1000	nA	T = 85 °C
Hibernate Mode, +105 °C							
SID42Q	I <sub>DD37Q</sub>	Regulator Off	–	–	19.4	μA	V <sub>DD</sub> = 1.71 V to 1.89 V
SID43Q	I <sub>DD38Q</sub>		–	–	17	μA	V <sub>DD</sub> = 1.8 V to 3.6 V
SID44Q	I <sub>DD39Q</sub>		–	–	16	μA	V <sub>DD</sub> = 3.6 V to 5.5 V
Stop Mode							
SID304	I <sub>DD43A</sub>	Stop Mode current; V <sub>DD</sub> = 3.3 V	–	20	80	nA	Typ at 25 °C. Max at 85 °C
		Stop Mode current; V <sub>DD</sub> = 5.5 V	–	20	750	nA	Typ at 25 °C Max at 85 °C
Stop Mode, +105 °C							
SID304Q	I <sub>DD43AQ</sub>	Stop Mode current; V <sub>DD</sub> = 3.6 V	–	–	5645	nA	
XRES current							
SID307	I <sub>DD_XR</sub>	Supply current while XRES asserted	–	2	5	mA	

### Analog Peripherals

#### Opamp

**Table 8. Opamp Specifications (Guaranteed by Characterization)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	$I_{DD}$	Opamp block current. No load.	–	–	–	–	
SID269	$I_{DD\_HI}$	Power = high	–	1100	1850	μA	
SID270	$I_{DD\_MED}$	Power = medium	–	550	950	μA	
SID271	$I_{DD\_LOW}$	Power = low	–	150	350	μA	
	GBW	Load = 20 pF, 0.1 mA. $V_{DDA} = 2.7$ V	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	$I_{OUT\_MAX}$	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–	–	
SID275	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
	$I_{OUT}$	$V_{DDA} = 1.71$ V, 500 mV from rail	–	–	–	–	
SID278	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID281	$V_{IN}$	Charge pump on, $V_{DDA} \geq 2.7$ V	–0.05	–	$V_{DDA} - 0.2$	V	
SID282	$V_{CM}$	Charge pump on, $V_{DDA} \geq 2.7$ V	–0.05	–	$V_{DDA} - 0.2$	V	
	$V_{OUT}$	$V_{DDA} \geq 2.7$ V	–	–	–	–	
SID283	$V_{OUT\_1}$	Power = high, Iload=10 mA	0.5	–	$V_{DDA} - 0.5$	V	
SID284	$V_{OUT\_2}$	Power = high, Iload=1 mA	0.2	–	$V_{DDA} - 0.2$	V	
SID285	$V_{OUT\_3}$	Power = medium, Iload=1 mA	0.2	–	$V_{DDA} - 0.2$	V	
SID286	$V_{OUT\_4}$	Power = low, Iload=0.1mA	0.2	–	$V_{DDA} - 0.2$	V	
SID288	$V_{OS\_TR}$	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	$V_{OS\_TR}$	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	$V_{OS\_TR}$	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	μV/°C	High mode $T_A \leq 85$ °C.
SID290Q	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–15	±3	15	μV/°C	High mode. $T_A \leq 105$ °C
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	μV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	μV/°C	Low mode
SID291	CMRR	DC	70	80	–	dB	$V_{DDD} = 3.6$ V
SID292	PSRR	At 1 kHz, 100 mV ripple	70	85	–	dB	$V_{DDD} = 3.6$ V
	Noise		–	–	–	–	
SID293	$V_{N1}$	Input referred, 1 Hz - 1GHz, power = high	–	94	–	μVrms	
SID294	$V_{N2}$	Input referred, 1 kHz, power = high	–	72	–	nV/rHz	
SID295	$V_{N3}$	Input referred, 10 kHz, power = high	–	28	–	nV/rHz	
SID296	$V_{N4}$	Input referred, 100 kHz, power = high	–	15	–	nV/rHz	

### SPI Specifications

**Table 22. Fixed SPI DC Specifications (Guaranteed by Characterization)**

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID163	I <sub>SPI1</sub>	Block current consumption at 1 Mb/s/sec	–	–	360	μA
SID164	I <sub>SPI2</sub>	Block current consumption at 4 Mb/s/sec	–	–	560	μA
SID165	I <sub>SPI3</sub>	Block current consumption at 8 Mb/s/sec	–	–	600	μA

**Table 23. Fixed SPI AC Specifications (Guaranteed by Characterization)**

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID166	F <sub>SPI</sub>	SPI operating frequency (master; 6X oversampling)	–	–	4	MHz

**Table 24. Fixed SPI Master mode AC Specifications (Guaranteed by Characterization)**

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID167	T <sub>DMO</sub>	MOSI valid after S <sub>clock</sub> driving edge	–	–	15	ns
SID168	T <sub>DSI</sub>	MISO valid before S <sub>clock</sub> capturing edge. Full clock, late MISO Sampling used	20	–	–	ns
SID169	T <sub>HMO</sub>	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns

**Table 25. Fixed SPI Slave mode AC Specifications (Guaranteed by Characterization)**

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID170	T <sub>DMI</sub>	MOSI valid before S <sub>clock</sub> capturing edge	40	–	–	ns
SID171	T <sub>DSO</sub>	MISO valid after S <sub>clock</sub> driving edge	–	–	42 + (3 × T <sub>scbclk</sub> )	ns
SID171A	T <sub>DSO_ext</sub>	MISO valid after S <sub>clock</sub> driving edge in Ext. Clock mode	–	–	48	ns
SID172	T <sub>HMO</sub>	Previous MISO data hold time	0	–	–	ns
SID172A	T <sub>SSEL_SCK</sub>	SSEL Valid to first SCK Valid edge	100	–	–	ns



## Memory

**Table 26. Flash DC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V <sub>PE</sub>	Erase and program voltage	1.71	–	5.5	V	

**Table 27. Flash AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T <sub>ROWWRITE</sub> <sup>[3]</sup>	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes. –40 °C ≤ T <sub>A</sub> ≤ 85 °C
			–	–	26	ms	Row (block) = 128 bytes. –40 °C ≤ T <sub>A</sub> ≤ 105 °C
SID175	T <sub>ROWERASE</sub> <sup>[3]</sup>	Row erase time	–	–	13	ms	
SID176	T <sub>ROWPROGRAM</sub> <sup>[3]</sup>	Row program time after erase	–	–	7	ms	–40 °C ≤ T <sub>A</sub> ≤ 85 °C
			–	–	13	ms	–40 °C ≤ T <sub>A</sub> ≤ 105 °C
SID178	T <sub>BULKERASE</sub> <sup>[3]</sup>	Bulk erase time (32 KB)	–	–	35	ms	
SID180	T <sub>DEVPROG</sub> <sup>[3]</sup>	Total device program time	–	–	7	seconds	Guaranteed by characterization
SID181	F <sub>END</sub>	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F <sub>RET</sub>	Flash retention. T <sub>A</sub> ≤ 55 °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. T <sub>A</sub> ≤ 85 °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	F <sub>RETQ</sub>	Flash retention. T <sub>A</sub> ≤ 105 °C, 10K P/E cycles, ≤ three years at T <sub>A</sub> ≥ 85 °C.	10	20	–		Guaranteed by characterization.

## System Resources

*Power-on-Reset (POR) with Brown Out*

**Table 28. Imprecise Power On Reset (PRES)**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	V <sub>RISEIPOR</sub>	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	V <sub>FALLIPOR</sub>	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization
SID187	V <sub>IPORHYST</sub>	Hysteresis	15	–	200	mV	Guaranteed by characterization

**Table 29. Precise Power On Reset (POR)**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	V <sub>FALLPPOR</sub>	BOD trip voltage in active and sleep modes	1.64	–	–	V	Full functionality between 1.71 V and BOD trip voltage is guaranteed by characterization
SID192	V <sub>FALLDPSLP</sub>	BOD trip voltage in Deep Sleep	1.4	–	–	V	Guaranteed by characterization
BID55	Svdd	Maximum power supply ramp rate	–	–	67	kV/sec	

### Note

- It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

### Internal Main Oscillator

**Table 33. IMO DC Specifications (Guaranteed by Design)**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID219	I <sub>IMO2</sub>	IMO operating current at 24 MHz	–	–	325	μA	
SID220	I <sub>IMO3</sub>	IMO operating current at 12 MHz	–	–	225	μA	
SID221	I <sub>IMO4</sub>	IMO operating current at 6 MHz	–	–	180	μA	
SID222	I <sub>IMO5</sub>	IMO operating current at 3 MHz	–	–	150	μA	

**Table 34. IMO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F <sub>IMOTOL1</sub>	Frequency variation from 3 to 24 MHz	–	–	±2	%	+3% if T <sub>A</sub> > 85 °C and IMO frequency < 24 MHz
SID226	T <sub>STARTIMO</sub>	IMO startup time	–	–	12	μs	
SID227	T <sub>JITRMSIMO1</sub>	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	T <sub>JITRMSIMO2</sub>	RMS Jitter at 24 MHz	–	145	–	ps	

### Internal Low-Speed Oscillator

**Table 35. ILO DC Specifications (Guaranteed by Design)**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I <sub>ILO1</sub>	ILO operating current at 32 kHz	–	0.3	1.05	μA	Guaranteed by Characterization
SID233	I <sub>ILOLEAK</sub>	ILO leakage current	–	2	15	nA	Guaranteed by Design

**Table 36. ILO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	T <sub>STARTILO1</sub>	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	T <sub>ILODUTY</sub>	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	F <sub>ILOTRIM1</sub>	32 kHz trimmed frequency	15	32	50	kHz	Max. ILO frequency is 70 kHz if T <sub>A</sub> > 85 °C

**Table 37. External Clock Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	24	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at V <sub>DD/2</sub>	45	–	55	%	Guaranteed by characterization

The field values are listed in Table 40.

**Table 40. Field Values**

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family within architecture	1	4100 Family
		2	4200 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
DE	Package Code	PV	SSOP
F	Temperature Range	A/S	Automotive
GHI	Attributes Code	000-999	Code of feature set in specific family
Z	Fab location change		

## Packaging

**Table 41. Package Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Operating ambient temperature	For A grade devices	–40	25.00	85	°C
T <sub>A</sub>	Operating ambient temperature	For S grade devices	–40	25.00	105	°C
T <sub>J</sub>	Operating junction temperature	For A grade devices	–40	–	100	°C
T <sub>J</sub>	Operating junction temperature	For S grade devices	–40	–	120	°C
T <sub>JA</sub>	Package $\theta_{JA}$ (28-pin SSOP)		–	66.58	–	°C/W
T <sub>JC</sub>	Package $\theta_{JC}$ (28-pin SSOP)		–	46.28	–	°C/W

**Table 42. Solder Reflow Peak Temperature**

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
28-pin SSOP	260 °C	30 seconds

**Table 43. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

Package	MSL
28-pin SSOP	MSL 3

PSoC4 CAB Libraries with Schematics Symbols and PCB Footprints are on the Cypress web site at [http://www.cypress.com/cad-resources/psoc-4-cad-libraries?source=search&cat=technical\\_documents](http://www.cypress.com/cad-resources/psoc-4-cad-libraries?source=search&cat=technical_documents)

**Table 44. Acronyms Used in this Document** *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC <sup>®</sup>	Programmable System-on-Chip <sup>™</sup>
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA

**Table 44. Acronyms Used in this Document** *(continued)*

Acronym	Description
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

## Document Conventions

### Units of Measure

**Table 45. Units of Measure**

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
Ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

### Document History Page

Document Title: Automotive PSoC® 4: PSoC 4100 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-93576				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*B	5071385	THOR / KIKU	01/21/2016	Changed status from Preliminary to Final.
*C	5117912	MVRE	01/31/2016	Updated <a href="#">Features</a> : Updated <a href="#">Programmable Analog</a> : Replaced “Two opamps” with “One opamp”. Updated <a href="#">Block Diagram</a> : Replaced “2x” with “1x”. Updated <a href="#">Functional Overview</a> : Updated <a href="#">Analog Blocks</a> : Updated <a href="#">Opamp (CTBm Block)</a> : Replaced “Two opamps” with “Opamp” in heading. Updated description. Updated <a href="#">Power</a> : Updated <a href="#">Unregulated External Supply</a> : Updated <a href="#">Table 1</a> : Updated details in “Bypass Capacitors” column corresponding to “VDDD–VSS” and “VCCD–VSS” power supplies.
*D	5331416	MVRE	07/04/2016	Updated <a href="#">Functional Overview</a> : Updated <a href="#">CPU and Memory Subsystem</a> : Updated <a href="#">Flash</a> : Updated description. Updated <a href="#">Fixed Function Digital</a> : Updated <a href="#">Serial Communication Blocks (SCB)</a> : Updated description. Updated <a href="#">Pinouts</a> : Updated description. Updated <a href="#">Figure 3</a> . Updated <a href="#">Power</a> : Added <a href="#">Figure 4</a> . Updated <a href="#">Unregulated External Supply</a> : Updated <a href="#">Table 1</a> : Updated details in “Bypass Capacitors” column corresponding to “VDDD–VSS” and “VREF–VSS (optional)” Power Supply.



## Document History Page *(continued)*

Document Title: Automotive PSoC® 4: PSoC 4100 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-93576				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*D (cont.)	5331416	MVRE	07/04/2016	Updated <a href="#">Electrical Specifications</a> : Updated <a href="#">System Resources</a> : Updated <a href="#">Power-on-Reset (POR) with Brown Out</a> : Updated <a href="#">Table 29</a> : Updated details in “Details/Conditions” column corresponding to $V_{FALLPPOR}$ parameter. Added $Svdd$ parameter and its details. Updated <a href="#">Internal Main Oscillator</a> : Updated <a href="#">Table 34</a> : Updated details in “Details/Conditions” column corresponding to $F_{IMOTOL1}$ parameter. Updated <a href="#">Internal Low-Speed Oscillator</a> : Updated <a href="#">Table 36</a> : Updated details in “Details/Conditions” column corresponding to $F_{ILOTRIM1}$ parameter. Updated <a href="#">Packaging</a> : Updated description. Updated to new template. Completing Sunset Review.
*E	5675099	SNPR	03/28/2017	Updated <a href="#">Ordering Information</a> .