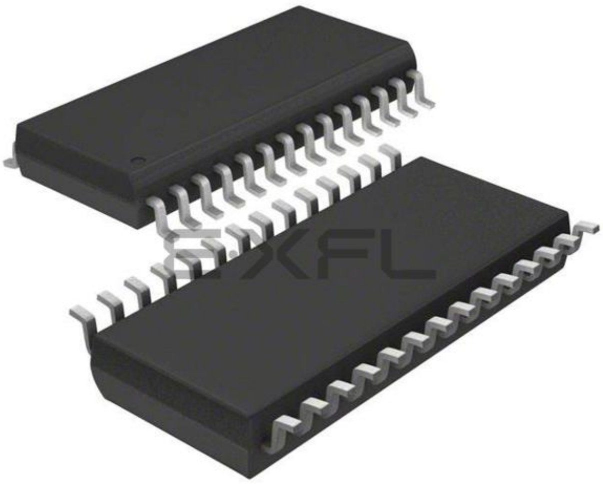

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 24MHz |
| Connectivity | I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 24 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 8x12b SAR; D/A 2xIDAC |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4124pva-442zt |

# Functional Overview

## CPU and Memory Subsystem

*CPU*

The Cortex-M0 CPU in PSoC 4100 is part of the 32-bit MCU subsystem, which is optimized for low power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from Deep Sleep mode allowing power to be switched off to the main processor when the chip is in Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt input (NMI), which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the Serial Wire Debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4100 has four break-point (address) comparators and two watchpoint (data) comparators.

*Flash*

PSoC 4100 has a flash module with a flash accelerator tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 0 wait-state (WS) access time at 24 MHz. Part of the flash module can be used to emulate EEPROM operation if required.

The PSoC 4100 flash supports the following flash protection modes at the memory sub-system level.

**Open:** No protection. Factory default mode that the product is shipped in.

**Protected:** User may change from Open to Protected. This mode disables debug interface accesses. The mode can be set back to Open but only after completely erasing the flash.

**Kill:** User may change from Open to Kill. This mode disables all debug accesses. The part cannot be erased externally, thus obviating the possibility of partial erasure by power interruption and potential malfunction and security leaks. This is an irrecvocable mode.

In addition, row-level Read/Write protection is also supported to prevent inadvertent Writes as well as selectively block Reads. Flash Read/Write/Erase operations are always available for internal code using system calls.

*SRAM*

SRAM memory is retained during Hibernate.

*SROM*

A supervisory ROM that contains boot and configuration routines is provided.

## System Resources

*Power System*

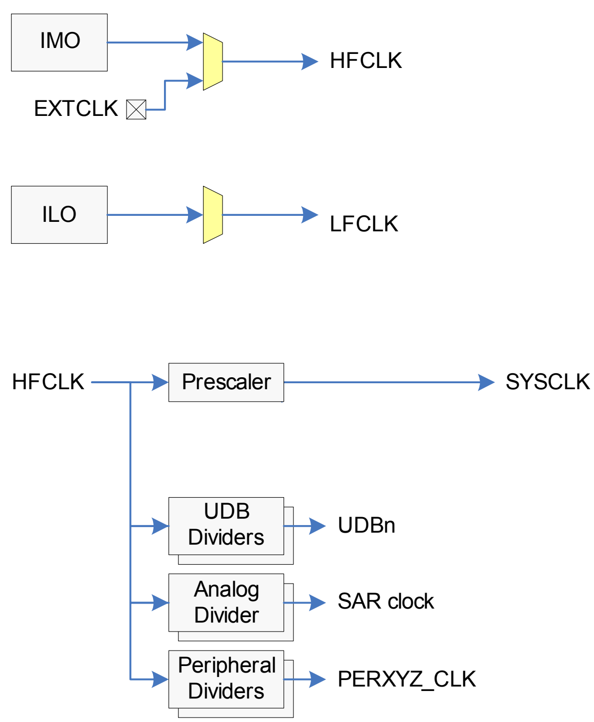
The power system is described in detail in the section Power on page 10. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low-voltage detect (LVD)). The PSoC 4100 operates with a single external supply over the range of 1.71 V to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4100 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

*Clock System*

The PSoC 4100 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for the PSoC 4100 consists of two internal oscillators, IMO and the ILO, and provision for an external clock.

**Figure 1. PSoC 4100 MCU Clocking Architecture**




The HFCLK signal can be divided down (see PSoC 4100 MCU Clocking Architecture) to generate synchronous clocks for the analog and digital peripherals. There are a total of 12 clock dividers for the PSoC 4100, each with 16-bit divide capability. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

*IMO Clock Source*

The IMO is the primary source of internal clocking in the PSoC 4100. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 MHz to 24 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is ±2%.

*ILO Clock Source*

The ILO is a very low power oscillator, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

*Watchdog Timer*

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

*Reset*

PSoC 4100 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the Reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

*Voltage Reference*

The PSoC 4100 reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or to use an external reference for the SAR.

## Analog Blocks

*12-bit SAR ADC*

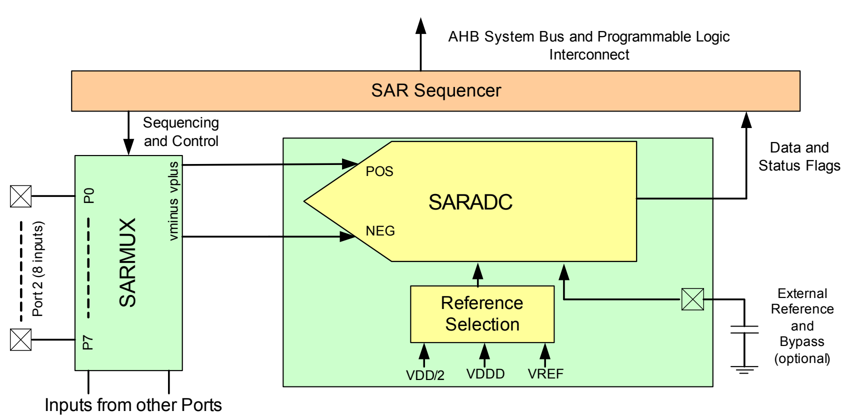
The 12-bit 806 Ksps SAR ADC can operate at a maximum clock rate of 14.5 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice (for the PSoC 4100 case) of three internal voltage references: $V_{DD}$, $V_{DD}/2$, and $V_{REF}$ (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision providing appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, aggregate sampling bandwidth is equal to 806 Ksps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

**Figure 2. SAR ADC System Diagram**



*Opamp (CTBm Block)*

PSoC 4100 has an opamp with Comparator mode, which allows most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamp is designed with enough bandwidth to drive the S/H circuit of the ADC without requiring external buffering.

*Temperature Sensor*

PSoC 4100 has one on-chip temperature sensor This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress supplied software that includes calibration and linearization.

*Low-power Comparators*

PSoC 4100 has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

### Fixed Function Digital

*Timer/Counter/PWM Block*

The Timer/Counter/PWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

*Serial Communication Blocks (SCB)*

PSoC 4100 has two SCBs, which can each implement an $I^2C$, UART, SPI, or LIN Slave interface.

**$I^2C$ Mode**: The hardware $I^2C$ block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The $I^2C$ peripheral is compatible with the $I^2C$ Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP $I^2C$-bus specification and user manual (UM10204). The $I^2C$ bus I/O is implemented with GPIO in open-drain modes. The I2C bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. Required Rise and Fall times for different I2C speeds are guaranteed by using appropriate pull-up resistor values depending on $V_{DD}$, Bus Capacitance, and resistor tolerance. For detailed information on how to calculate the optimum pull-up resistor value for your design, please refer to the UM10204 $I^2C$ bus specification and user manual, the newest revision is available at www.nxp.com.

The PSoC 4100 is not completely compliant with the $I^2C$ spec in the following respects:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the $I^2C$ system.
- Fast-mode Plus has an $I_{OL}$ specification of 20 mA at a $V_{OL}$ of 0.4 V. The GPIO cells can sink a maximum of 8 mA $I_{OL}$ with a $V_{OL}$ maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an $I^2C$ Master, it interposes an IDLE state between NACK and Repeated Start; the $I^2C$ spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in $I^2C$ Slave mode, and Address Match on External Clock is enabled (EC_AM = 1) along with operation in the internally clocked mode (EC_OP = 0), then its $I^2C$ address must be even.

**UART Mode**: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

**SPI Mode**: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and also supports an EzSPI mode in which data interchange is reduced to reading and writing an array in memory.

**LIN Slave Mode**: The LIN Slave mode uses the SCB hardware block and implements a full LIN slave interface. This LIN slave is compliant with LIN v1.3 and LIN v2.1/2.2 specification standards. It is certified by C&S GmbH based on the standard protocol and data link layer conformance tests. The LIN slave can be operated at baud rates of up to ~20 Kbps with a maximum of 40-meter cable length. PSoC Creator software supports up to two LIN slave interfaces in the PSoC 4 device, providing built-in application programming interfaces (APIs) based on the LIN specification standard.

### GPIO

PSoC 4100 has 24 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100).

### Special Function Peripherals

*LCD Segment Drive*

The PSoC 4100 has an LCD controller which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

*CapSense*

CapSense is supported on all pins in the PSoC 4100 through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used.(both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

**VDDA**: Analog $V_{DD}$ pin where package pins allow; shorted to $V_{DDD}$ otherwise.

**VSSA:** Analog ground pin where package pins allow; shorted to VSS otherwise

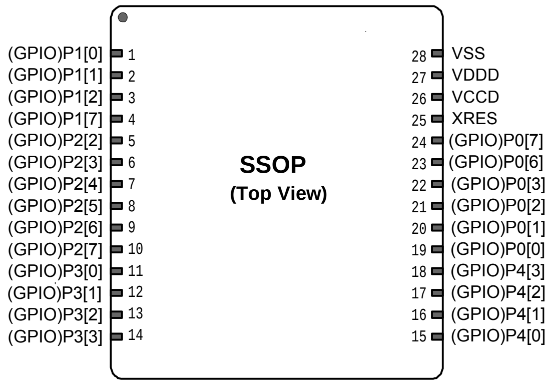
**VSS**: Ground pin.

**VCCD**: Regulated Digital supply (1.8 V ±5%).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

The following package is supported: 28-pin SSOP.

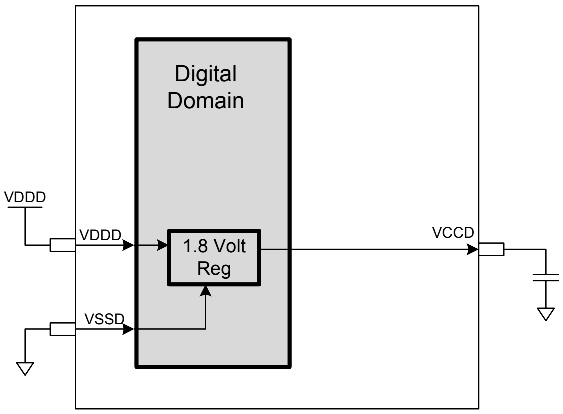
**Figure 3. 28-pin SSOP pinout**



## Power

The following power system diagram shows the minimum set of power supply pins as implemented for the PSoC 4100. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the $V_{DDA}$ input. There are separate regulators for the Deep Sleep and Hibernate (lowered power supply and retention) modes. There is a separate low-noise regulator for the bandgap. The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

**Figure 4. PSoC 4 Power Supply**




The PSoC 4100 family allows two distinct modes of power supply operation: Unregulated External Supply, and Regulated External Supply modes.

### Unregulated External Supply

In this mode, PSoC 4100 is powered by an External Power Supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4100 supplies the internal logic and the VCCD output of the PSoC 4100 must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6 µF; X5R ceramic or better).

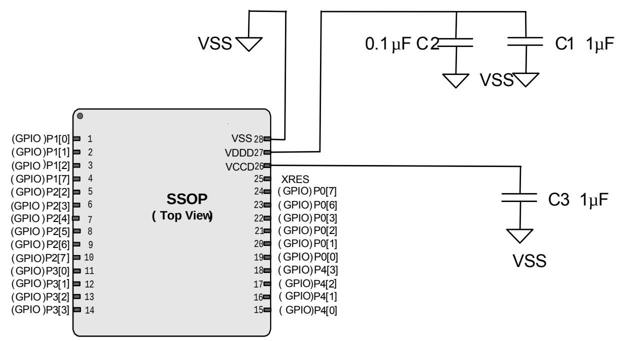
Bypass capacitors must be used from VDDD to ground, typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (0.1 µF for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme for the 28-pin SSOP package follows.

**Table 1. Example of a bypass scheme**

| Power Supply | Bypass Capacitors |
|---|---|
| VDDD–VSS | 0.1 µF ceramic capacitor (C2) plus bulk capacitor 1 to 10 µF (C1). Total Capacitance may be greater than 10 µF. |
| VCCD–VSS | 1 µF ceramic capacitor at the VCCD pin (C3) |
| VREF–VSS (optional) | The internal bandgap may be bypassed with a 1 µF to 10 µF capacitor. Total capacitance may be greater than 10 µF. |

**Figure 5. 28-Pin SSOP Example**




### Regulated External Supply

In this mode, the PSoC 4100 is powered by an external power supply that must be within the range of 1.71 to 1.89 V (1.8 ± 5%); note that this range needs to include power supply ripple too. In this mode, VCCD, and VDDD pins are all shorted together and bypassed. The internal regulator is disabled in firmware.

## Development Support

The PSoC 4100 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

### Documentation

A suite of documentation supports the PSoC 4100 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide**: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets**: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes**: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual**: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

**Table 10. Comparator AC Specifications**

(Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID91 | $T_{RESP1}$ | Response time, normal mode | – | – | 110 | ns | 50 mV overdrive |
| SID258 | $T_{RESP2}$ | Response time, low power mode | – | – | 200 | ns | 50 mV overdrive |
| SID92 | $T_{RESP3}$ | Response time, ultra low power mode ($V_{DDD}$ ≥ 2.2 V for Temp < 0 °C, $V_{DDD}$ ≥ 1.8 V for Temp > 0 °C) | – | – | 15 | µs | 200 mV overdrive |

*Temperature Sensor*

**Table 11. Temperature Sensor Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID93 | $T_{SENSACC}$ | Temperature sensor accuracy | –5 | ±1 | +5 | °C | –40 to +85 °C |

*SAR ADC*

**Table 12. SAR ADC DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID94 | A_RES | Resolution | – | – | 12 | bits | |
| SID95 | A_CHNIS_S | Number of channels - single ended | – | – | 8 | | 8 full speed |
| SID96 | A-CHNKS_D | Number of channels - differential | – | – | 4 | | Diff inputs use neighboring I/O |
| SID97 | A-MONO | Monotonicity | – | – | – | | Yes. Based on characterization |
| SID98 | A_GAINERR | Gain error | – | – | ±0.1 | % | With external reference. Guaranteed by characterization |
| SID99 | A_OFFSET | Input offset voltage | – | – | 2 | mV | Measured with 1-V $V_{REF.}$ Guaranteed by characterization |
| SID100 | A_ISAR | Current consumption | – | – | 1 | mA | |
| SID101 | A_VINS | Input voltage range - single ended | $V_{SS}$ | – | $V_{DDA}$ | V | Based on device characterization |
| SID102 | A_VIND | Input voltage range - differential | $V_{SS}$ | – | $V_{DDA}$ | V | Based on device characterization |
| SID103 | A_INRES | Input resistance | – | – | 2.2 | KΩ | Based on device characterization |
| SID104 | A_INCAP | Input capacitance | – | – | 10 | pF | Based on device characterization |

Table 13. SAR ADC AC Specifications (Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID106 | A_PSRR | Power supply rejection ratio | 70 | – | – | dB | |
| SID107 | A_CMRR | Common mode rejection ratio | 66 | – | – | dB | Measured at 1 V |
| SID108 | A_SAMP_1 | Sample rate with external reference bypass cap | – | – | 1 | Msps | |
| SID108A | A_SAMP_2 | Sample rate with no bypass cap. Reference = $V_{DD}$ | – | – | 806 | Ksps | |
| SID108B | A_SAMP_3 | Sample rate with no bypass cap. Internal reference | – | – | 100 | Ksps | |
| SID109 | A_SNDR | Signal-to-noise and distortion ratio (SINAD) | 65 | – | – | dB | $F_{IN}$ = 10 kHz |
| SID111 | A_INL | Integral non linearity | –1.7 | – | +2 | LSB | $V_{DD}$ = 1.71 to 5.5, 806 Ksps, Vref = 1 to 5.5. –40 °C ≤ $T_A$ ≤ 85 °C |
| | | | –1.9 | – | +2 | LSB | $V_{DD}$ = 1.71 to 5.5, 806 Ksps, Vref = 1 to 5.5. –40 °C ≤ $T_A$ ≤ 105 °C |
| SID111A | A_INL | Integral non linearity | –1.5 | – | +1.7 | LSB | $V_{DDD}$ = 1.71 to 3.6, 806 Ksps, Vref = 1.71 to $V_{DDD}$. –40 °C ≤ $T_A$ ≤ 85 °C |
| | | | –1.9 | – | +2 | LSB | $V_{DDD}$ = 1.71 to 3.6, 806 Ksps, Vref = 1.71 to $V_{DDD}$. –40 °C ≤ $T_A$ ≤ 105 °C |
| SID111B | A_INL | Integral non linearity | –1.5 | – | +1.7 | LSB | $V_{DDD}$ = 1.71 to 5.5, 500 Ksps, Vref = 1 to 5.5. |
| SID112 | A_DNL | Differential non linearity | –1 | – | +2.2 | LSB | $V_{DDD}$ = 1.71 to 5.5, 806 Ksps, Vref = 1 to 5.5. –40 °C ≤ $T_A$ ≤ 85 °C |
| | | | –1 | – | +2.3 | LSB | $V_{DDD}$ = 1.71 to 5.5, 806 Ksps, Vref = 1 to 5.5. –40 °C ≤ $T_A$ ≤ 105 °C |
| SID112A | A_DNL | Differential non linearity | –1 | – | +2 | LSB | $V_{DDD}$ = 1.71 to 3.6, 806 Ksps, Vref = 1.71 to $V_{DDD}$. –40 °C ≤ $T_A$ ≤ 85 °C |
| | | | –1 | – | +2.2 | LSB | $V_{DDD}$ = 1.71 to 3.6, 806 Ksps, Vref = 1.71 to $V_{DDD}$. –40 °C ≤ $T_A$ ≤ 105 °C |
| SID112B | A_DNL | Differential non linearity | –1 | – | +2.2 | LSB | $V_{DDD}$ = 1.71 to 5.5, 500 Ksps, Vref = 1 to 5.5. |
| SID113 | A_THD | Total harmonic distortion | – | – | –65 | dB | $F_{IN}$ = 10 kHz. |

*SPI Specifications*

**Table 22. Fixed SPI DC Specifications (Guaranteed by Characterization)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SID163 | $I_{SPI1}$ | Block current consumption at 1 Mbits/sec | – | – | 360 | µA |
| SID164 | $I_{SPI2}$ | Block current consumption at 4 Mbits/sec | – | – | 560 | µA |
| SID165 | $I_{SPI3}$ | Block current consumption at 8 Mbits/sec | – | – | 600 | µA |

**Table 23. Fixed SPI AC Specifications (Guaranteed by Characterization)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SID166 | $F_{SPI}$ | SPI operating frequency (master; 6X oversampling) | – | – | 4 | MHz |

**Table 24. Fixed SPI Master mode AC Specifications (Guaranteed by Characterization)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SID167 | $T_{DMO}$ | MOSI valid after Sclock driving edge | – | – | 15 | ns |
| SID168 | $T_{DSI}$ | MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used | 20 | – | – | ns |
| SID169 | $T_{HMO}$ | Previous MOSI data hold time with respect to capturing edge at Slave | 0 | – | – | ns |

**Table 25. Fixed SPI Slave mode AC Specifications (Guaranteed by Characterization)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SID170 | $T_{DMI}$ | MOSI valid before Sclock capturing edge | 40 | – | – | ns |
| SID171 | $T_{DSO}$ | MISO valid after Sclock driving edge | – | – | 42 + (3 × Tscbclk) | ns |
| SID171A | $T_{DSO\_ext}$ | MISO valid after Sclock driving edge in Ext. Clock mode | – | – | 48 | ns |
| SID172 | $T_{HSO}$ | Previous MISO data hold time | 0 | – | – | ns |
| SID172A | $T_{SSELSCK}$ | SSEL Valid to first SCK Valid edge | 100 | – | – | ns |

## Memory

**Table 26. Flash DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID173 | $V_{PE}$ | Erase and program voltage | 1.71 | – | 5.5 | V | |

**Table 27. Flash AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID174 | $T_{ROWWRITE}$[3] | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 128 bytes. –40 °C ≤ $T_A$ ≤ 85 °C |
| | | | – | – | 26 | ms | Row (block) = 128 bytes. –40 °C ≤ $T_A$ ≤ 105 °C |
| SID175 | $T_{ROWERASE}$[3] | Row erase time | – | – | 13 | ms | |
| SID176 | $T_{ROWPROGRAM}$[3] | Row program time after erase | – | – | 7 | ms | –40 °C ≤ $T_A$ ≤ 85 °C |
| | | | – | – | 13 | ms | –40 °C ≤ $T_A$ ≤ 105 °C |
| SID178 | $T_{BULKERASE}$[3] | Bulk erase time (32 KB) | – | – | 35 | ms | |
| SID180 | $T_{DEVPROG}$[3] | Total device program time | – | – | 7 | seconds | Guaranteed by characterization |
| SID181 | $F_{END}$ | Flash endurance | 100 K | – | – | cycles | Guaranteed by characterization |
| SID182 | $F_{RET}$ | Flash retention. $T_A$ ≤ 55 °C, 100 K P/E cycles | 20 | – | – | years | Guaranteed by characterization |
| SID182A | | Flash retention. $T_A$ ≤ 85 °C, 10 K P/E cycles | 10 | – | – | years | Guaranteed by characterization |
| SID182B | $F_{RETQ}$ | Flash retention. $T_A$ ≤ 105 °C, 10K P/E cycles, ≤ three years at $T_A$ ≥ 85 °C. | 10 | 20 | – | | Guaranteed by characterization. |

## System Resources

*Power-on-Reset (POR) with Brown Out*

**Table 28. Imprecise Power On Reset (PRES)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID185 | $V_{RISEIPOR}$ | Rising trip voltage | 0.80 | – | 1.45 | V | Guaranteed by characterization |
| SID186 | $V_{FALLIPOR}$ | Falling trip voltage | 0.75 | – | 1.4 | V | Guaranteed by characterization |
| SID187 | $V_{IPORHYST}$ | Hysteresis | 15 | – | 200 | mV | Guaranteed by characterization |

**Table 29. Precise Power On Reset (POR)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID190 | $V_{FALLPPOR}$ | BOD trip voltage in active and sleep modes | 1.64 | – | – | V | Full functionality between 1.71 V and BOD trip voltage is guaranteed by characterization |
| SID192 | $V_{FALLDPSLP}$ | BOD trip voltage in Deep Sleep | 1.4 | – | – | V | Guaranteed by characterization |
| BID55 | Svdd | Maximum power supply ramp rate | – | – | 67 | kV/sec | |

**Note**

3. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

*Internal Main Oscillator*

**Table 33. IMO DC Specifications (Guaranteed by Design)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID219 | $I_{IMO2}$ | IMO operating current at 24 MHz | – | – | 325 | µA | |
| SID220 | $I_{IMO3}$ | IMO operating current at 12 MHz | – | – | 225 | µA | |
| SID221 | $I_{IMO4}$ | IMO operating current at 6 MHz | – | – | 180 | µA | |
| SID222 | $I_{IMO5}$ | IMO operating current at 3 MHz | – | – | 150 | µA | |

**Table 34. IMO AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID223 | $F_{IMOTOL1}$ | Frequency variation from 3 to 24 MHz | – | – | ±2 | % | ±3% if $T_A$ > 85 °C and IMO frequency < 24 MHz |
| SID226 | $T_{STARTIMO}$ | IMO startup time | – | – | 12 | µs | |
| SID227 | $T_{JITRMSIMO1}$ | RMS Jitter at 3 MHz | – | 156 | – | ps | |
| SID228 | $T_{JITRMSIMO2}$ | RMS Jitter at 24 MHz | – | 145 | – | ps | |

*Internal Low-Speed Oscillator*

**Table 35. ILO DC Specifications (Guaranteed by Design)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID231 | $I_{ILO1}$ | ILO operating current at 32 kHz | – | 0.3 | 1.05 | µA | Guaranteed by Characterization |
| SID233 | $I_{ILOLEAK}$ | ILO leakage current | – | 2 | 15 | nA | Guaranteed by Design |

**Table 36. ILO AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID234 | $T_{STARTILO1}$ | ILO startup time | – | – | 2 | ms | Guaranteed by characterization |
| SID236 | $T_{ILODUTY}$ | ILO duty cycle | 40 | 50 | 60 | % | Guaranteed by characterization |
| SID237 | $F_{ILOTRIM1}$ | 32 kHz trimmed frequency | 15 | 32 | 50 | kHz | Max. ILO frequency is 70 kHz if $T_A$ > 85 °C |

**Table 37. External Clock Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID305 | ExtClkFreq | External Clock input Frequency | 0 | – | 24 | MHz | Guaranteed by characterization |
| SID306 | ExtClkDuty | Duty cycle; Measured at $V_{DD/2}$ | 45 | – | 55 | % | Guaranteed by characterization |

**Table 38. Block Specs**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID257 | $T_{WS24}$* | Number of wait states at 24 MHz | 0 | – | – | | CPU execution from Flash. Guaranteed by characterization |
| SID260 | $V_{REFSAR}$ | Trimmed internal reference to SAR | –1 | – | +1 | % | Percentage of Vbg (1.024 V). Guaranteed by characterization |
| SID262 | $T_{CLKSWITCH}$ | Clock switching from clk1 to clk2 in clk1 periods | 3 | – | 4 | Periods | Guaranteed by design |
| * Tws24 is guaranteed by design. | | | | | | | |

## Ordering Information

The PSoC 4100 part numbers and features are listed in the Table 39.

**Table 39. PSoC 4100 Family Ordering Information**

| Family | MPN | Features | | | | | | | | | | | | Package | Operating Temperature | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Max CPU Speed (MHz) | Flash (KB) | SRAM (KB) | UDB | Opamp (CTBm) | CapSense | Direct LCD Drive | 12-bit SAR ADC | LP Comparators | TCPWM Blocks | SCB Blocks | GPIO | 28-SSOP | –40 to +85 °C | –40 to +105 °C |
| 4100 | CY8C4124PVA-442Z | 24 | 16 | 4 | – | 1 | ✔ | ✔ | 806 Ksps | 2 | 4 | 2 | 24 | ✔ | ✔ | – |
| | CY8C4125PVA-482Z | 24 | 32 | 4 | – | 1 | ✔ | ✔ | 806 Ksps | 2 | 4 | 2 | 24 | ✔ | ✔ | – |
| | CY8C4124PVS-442Z | 24 | 16 | 4 | – | 1 | ✔ | ✔ | 806 Ksps | 2 | 4 | 2 | 24 | ✔ | – | ✔ |
| | CY8C4125PVS-482Z | 24 | 32 | 4 | – | 1 | ✔ | ✔ | 806 Ksps | 2 | 4 | 2 | 24 | ✔ | – | ✔ |

### Part Numbering Conventions

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

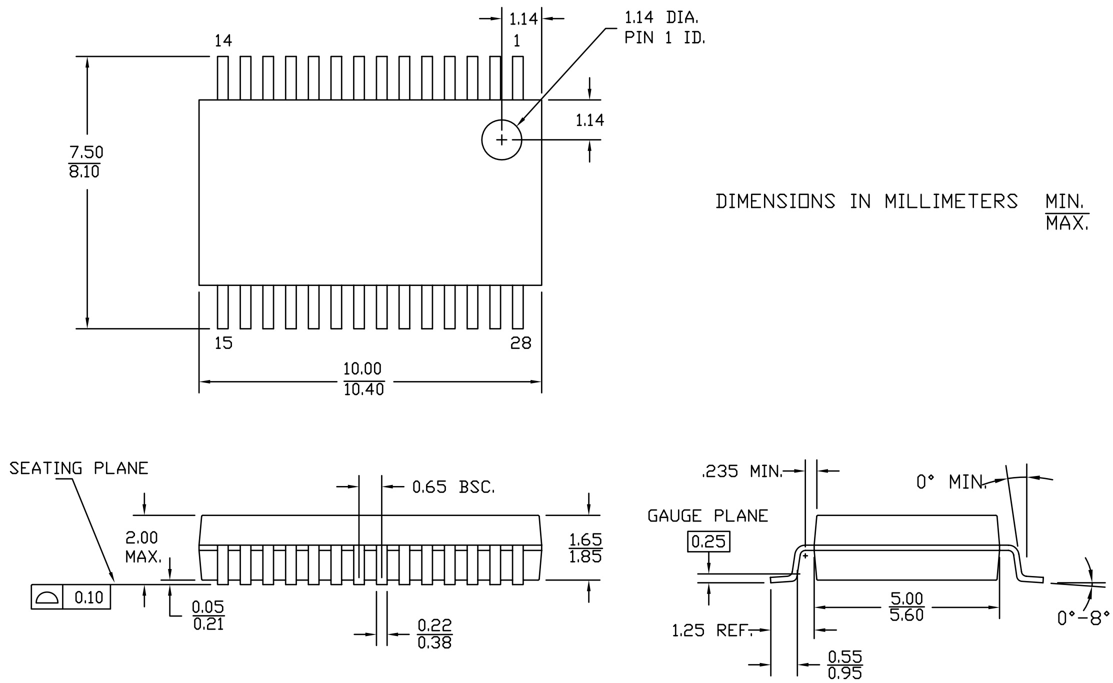
The part numbers are of the form CY8C4ABCDEF-GHI where the fields are defined as follows.

**Example**

**CY8C 4 A B C D E F - G H I Z**

| Example | | |
|---|---|---|
| | Cypress Prefix | CY8C |
| 4 : PSoC 4 | Architecture | 4 |
| 1 : 4100 Family | Family within Architecture | A |
| 2 : 24 MHz | Speed Grade | B |
| 5 : 32 KB | Flash Capacity | C |
| PV : SSOP | Package Code | DE |
| A: Automotive -40 to +85 °C<br>S: Automotive: -40 to +105 °C | Temperature Range | F |
| | Attributes Set | GHI |
| | Fab Location Change: Z | Z |

**Figure 6. 28-pin SSOP (210 Mils) Package Outline**




51-85079 *F

## Acronyms

**Table 44. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| ARM® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |

**Table 44. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| ETM | embedded trace macrocell |
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| $I^2C$, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |
| PC | program counter |
| PCB | printed circuit board |

# Document Conventions

## Units of Measure

Table 45. Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| Ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| µA | microampere |
| µF | microfarad |
| µH | microhenry |
| µs | microsecond |
| µV | microvolt |
| µW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

## Document History Page *(continued)*

| Document Title: Automotive PSoC® 4: PSoC 4100 Family Datasheet Programmable System-on-Chip (PSoC®)<br>Document Number: 001-93576 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *D (cont.) | 5331416 | MVRE | 07/04/2016 | Updated Electrical Specifications:<br>Updated Device-Level Specifications:<br>Updated Table 3:<br>Updated entire table.<br>Updated Analog Peripherals:<br>Updated Opamp:<br>Updated Table 8:<br>Updated values in “Typ” and “Max” columns for $I_{DD\_HI}$, $I_{DD\_MED}$, $I_{DD\_LOW}$ parameters.<br>Updated details in “Details/Conditions” column corresponding to “SID290” Spec ID and “$V_{OS\_DR\_TR}$” parameter.<br>Added SID290Q Spec ID corresponding to $V_{OS\_DR\_TR}$ parameter and its details.<br>Added SID299A Spec ID corresponding to OL_GAIN parameter and its details.<br>Updated Comparator:<br>Updated Table 9:<br>Updated details in “Description”, “Min”, “Typ”, “Max” columns corresponding to “$I_{CMP1}$”, “$I_{CMP2}$” and “$I_{CMP3}$” parameters.<br>Updated Table 10:<br>Updated details in “Description”, “Min”, “Typ”, “Max” columns corresponding to “$T_{RESP1}$”, “$T_{RESP2}$” and “$T_{RESP3}$” parameters.<br>Updated Digital Peripherals:<br>Removed “Timer”.<br>Removed “Counter”.<br>Removed “Pulse Width Modulation (PWM)”.<br>Added Timer/Counter/PWM.<br>Updated $I^2C$:<br>Updated Table 16:<br>Changed maximum value of $I_{I2C1}$ parameter from 10.5 µA to 50 µA.<br>Updated LCD Direct Drive:<br>Updated Table 20:<br>Changed maximum value of $I_{UART1}$ parameter from 9 µA to 55 µA.<br>Updated SPI Specifications:<br>Updated Table 25:<br>Replaced “FCPU” with “Tscbclk” in “Max” column corresponding to $T_{DSO}$ parameter.<br>Updated Memory:<br>Updated Table 27:<br>Added $F_{RETQ}$ parameter and its details. |

## Document History Page *(continued)*

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| **Document Title: Automotive PSoC® 4: PSoC 4100 Family Datasheet Programmable System-on-Chip (PSoC®)**<br>**Document Number: 001-93576** | | | | |
| *D (cont.) | 5331416 | MVRE | 07/04/2016 | Updated Electrical Specifications:<br>Updated System Resources:<br>Updated Power-on-Reset (POR) with Brown Out:<br>Updated Table 29:<br>Updated details in “Details/Conditions” column corresponding to $V_{FALLPPOR}$ parameter.<br>Added Svdd parameter and its details.<br>Updated Internal Main Oscillator:<br>Updated Table 34:<br>Updated details in “Details/Conditions” column corresponding to $F_{IMOTOL1}$ parameter.<br>Updated Internal Low-Speed Oscillator:<br>Updated Table 36:<br>Updated details in “Details/Conditions” column corresponding to $F_{ILOTRIM1}$ parameter.<br>Updated Packaging:<br>Updated description.<br>Updated to new template.<br>Completing Sunset Review. |
| *E | 5675099 | SNPR | 03/28/2017 | Updated Ordering Information. |

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