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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

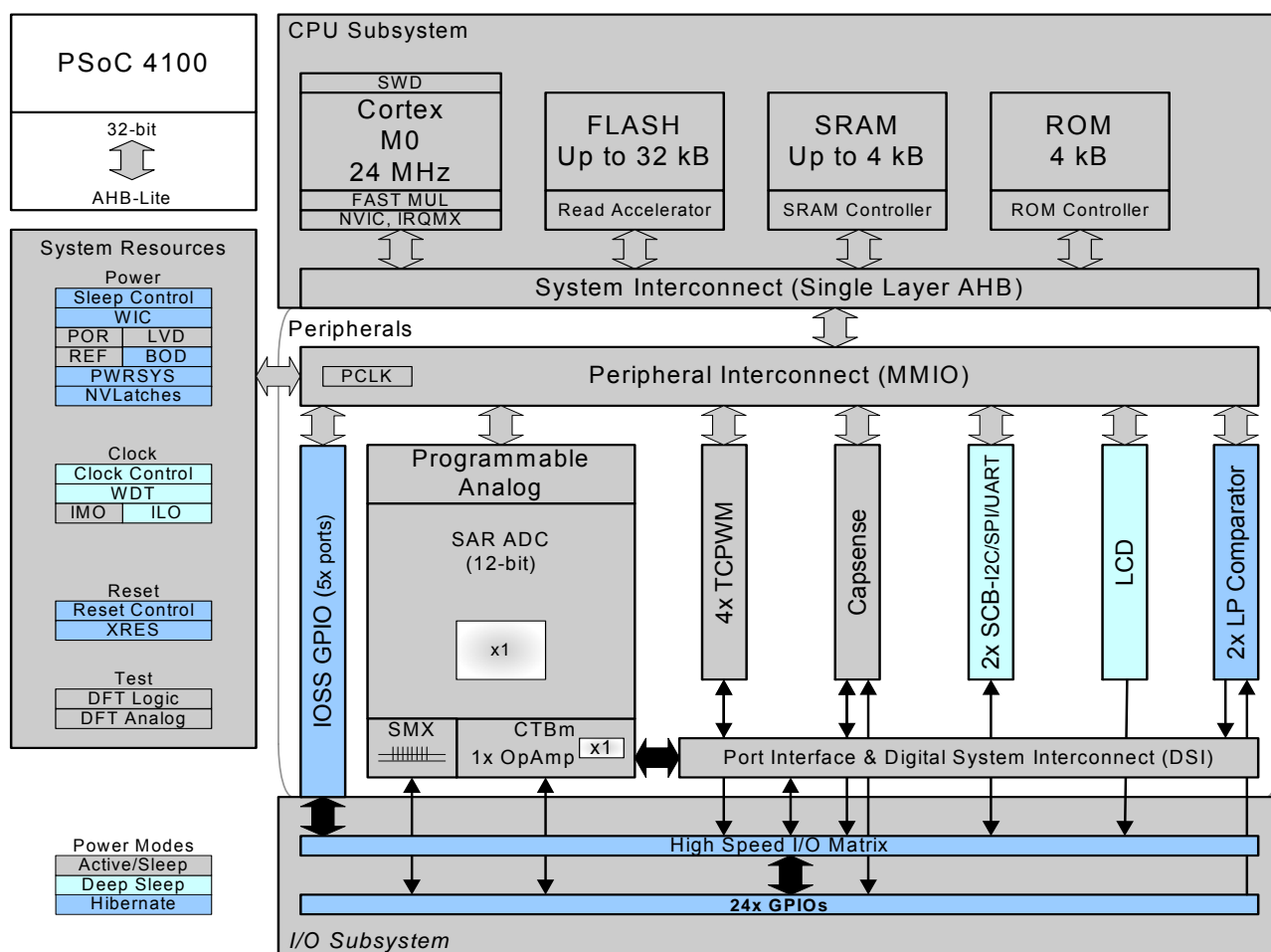
#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4125pva-482z">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4125pva-482z</a>

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### Block Diagram



### Functional Description

PSoC 4100 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial\_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 4100 devices. The SWD interface is fully compatible with industry standard third party tools. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip

programmable blocks, the PSoC 4100 family provides a level of security not possible with multi-chip application solutions or with microcontrollers.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4100 with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4100 allows the customer to make.

## Functional Overview

### CPU and Memory Subsystem

#### CPU

The Cortex-M0 CPU in PSoC 4100 is part of the 32-bit MCU subsystem, which is optimized for low power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from Deep Sleep mode allowing power to be switched off to the main processor when the chip is in Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt input (NMI), which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the Serial Wire Debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4100 has four break-point (address) comparators and two watchpoint (data) comparators.

#### Flash

PSoC 4100 has a flash module with a flash accelerator tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 0 wait-state (WS) access time at 24 MHz. Part of the flash module can be used to emulate EEPROM operation if required.

The PSoC 4100 flash supports the following flash protection modes at the memory sub-system level.

**Open:** No protection. Factory default mode that the product is shipped in.

**Protected:** User may change from Open to Protected. This mode disables debug interface accesses. The mode can be set back to Open but only after completely erasing the flash.

**Kill:** User may change from Open to Kill. This mode disables all debug accesses. The part cannot be erased externally, thus obviating the possibility of partial erasure by power interruption and potential malfunction and security leaks. This is an irrevocable mode.

In addition, row-level Read/Write protection is also supported to prevent inadvertent Writes as well as selectively block Reads. Flash Read/Write/Erase operations are always available for internal code using system calls.

#### SRAM

SRAM memory is retained during Hibernate.

#### SROM

A supervisory ROM that contains boot and configuration routines is provided.

## System Resources

### Power System

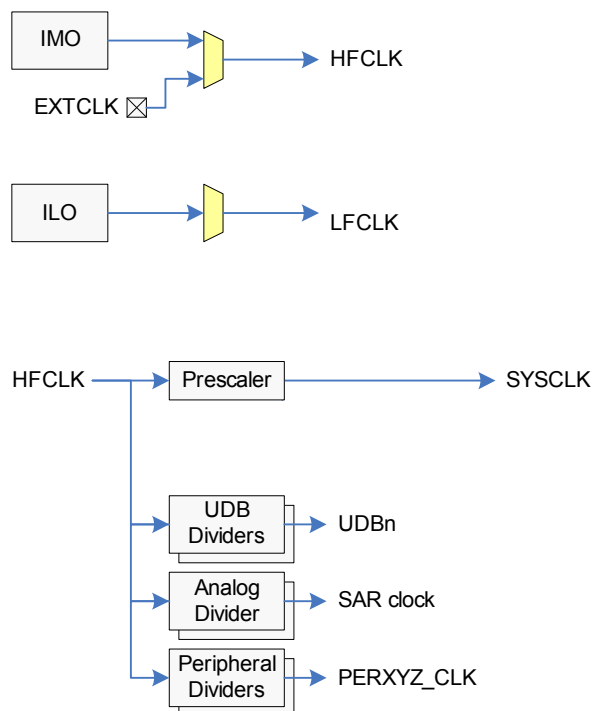
The power system is described in detail in the section [Power on page 10](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low-voltage detect (LVD)). The PSoC 4100 operates with a single external supply over the range of 1.71 V to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4100 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

### Clock System

The PSoC 4100 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for the PSoC 4100 consists of two internal oscillators, IMO and the ILO, and provision for an external clock.

**Figure 1. PSoC 4100 MCU Clocking Architecture**



The HFCLK signal can be divided down (see [PSoC 4100 MCU Clocking Architecture](#)) to generate synchronous clocks for the analog and digital peripherals. There are a total of 12 clock dividers for the PSoC 4100, each with 16-bit divide capability. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

### IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 MHz to 24 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is  $\pm 2\%$ .

### ILO Clock Source

The ILO is a very low power oscillator, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

### Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

### Reset

PSoC 4100 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the Reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

### Voltage Reference

The PSoC 4100 reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or to use an external reference for the SAR.

## Analog Blocks

### 12-bit SAR ADC

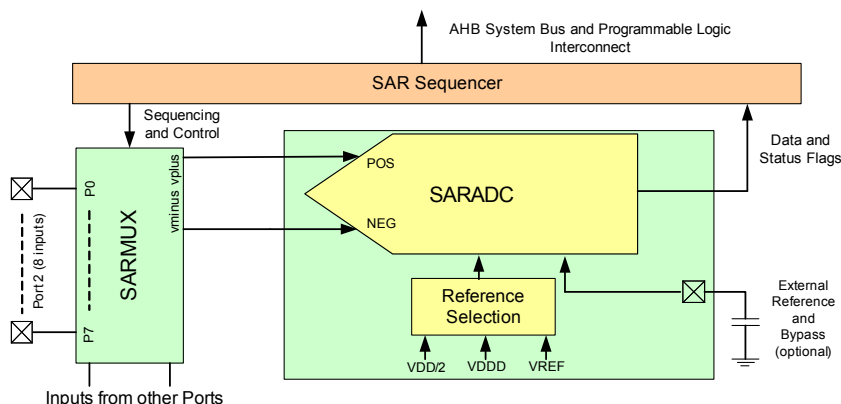
The 12-bit 806 Ksps SAR ADC can operate at a maximum clock rate of 14.5 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to  $\pm 1\%$ ) and by providing the choice (for the PSoC 4100 case) of three internal voltage references:  $V_{DD}$ ,  $V_{DD}/2$ , and  $V_{REF}$  (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision providing appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, aggregate sampling bandwidth is equal to 806 Ksps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

**Figure 2. SAR ADC System Diagram**



## GPIO

PSoC 4100 has 24 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100).

## Special Function Peripherals

### *LCD Segment Drive*

The PSoC 4100 has an LCD controller which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

### *CapSense*

CapSense is supported on all pins in the PSoC 4100 through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used. (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).



## Development Support

The PSoC 4100 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit [www.cypress.com/go/psoc4](http://www.cypress.com/go/psoc4) to find out more.

### Documentation

A suite of documentation supports the PSoC 4100 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide:** A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets:** The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes:** PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual:** The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at [www.cypress.com/psoc4](http://www.cypress.com/psoc4).

### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100 family is part of a development tool ecosystem. Visit us at [www.cypress.com/go/psoccreator](http://www.cypress.com/go/psoccreator) for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

## Electrical Specifications

### Absolute Maximum Ratings

**Table 2. Absolute Maximum Ratings**<sup>[1]</sup>

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID1	V <sub>DDD_ABS</sub>	Digital supply relative to V <sub>SSD</sub>	-0.5	–	6	V	Absolute max
SID2	V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to V <sub>SSD</sub>	-0.5	–	1.95	V	Absolute max
SID3	V <sub>GPI0_ABS</sub>	GPIO voltage	-0.5	–	V <sub>DD</sub> +0.5	V	Absolute max
SID4	I <sub>GPI0_ABS</sub>	Maximum current per GPIO	-25	–	25	mA	Absolute max
SID5	I <sub>GPI0_injection</sub>	GPIO injection current, Max for V <sub>IH</sub> > V <sub>DDD</sub> , and Min for V <sub>IL</sub> < V <sub>SS</sub>	-0.5	–	0.5	mA	Absolute max, current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	-200	–	200	mA	

### Device-Level Specifications

All specifications are valid for -40 °C ≤ T<sub>A</sub> ≤ 85 °C for A grade devices and -40 °C ≤ T<sub>A</sub> ≤ 105 °C for S grade devices, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

**Table 3. DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID53	V <sub>DD</sub>	Power supply input voltage (V <sub>DDA</sub> = V <sub>DDD</sub> = V <sub>DD</sub> )	1.8	–	5.5	V	With regulator enabled
SID255	V <sub>DDD</sub>	Power supply input voltage unregulated	1.71	1.8	1.89	V	Internally unregulated Supply
SID54	V <sub>CCD</sub>	Output voltage (for core logic)	–	1.8	–	V	
SID55	C <sub>EFC</sub>	External regulator voltage bypass	1	1.3	1.6	μF	X5R ceramic or better
SID56	C <sub>EXC</sub>	Power supply decoupling capacitor	–	1	–	μF	X5R ceramic or better
<b>Active Mode, V<sub>DD</sub> = 1.71 V to 5.5 V. Typical Values measured at V<sub>DD</sub> = 3.3 V.</b>							
SID9	I <sub>DD4</sub>	Execute from Flash; CPU at 6 MHz	–	–	2.8	mA	
SID10	I <sub>DD5</sub>	Execute from Flash; CPU at 6 MHz	–	2.2	–	mA	T = 25 °C
SID12	I <sub>DD7</sub>	Execute from Flash; CPU at 12 MHz	–	–	4.2	mA	
SID13	I <sub>DD8</sub>	Execute from Flash; CPU at 12 MHz	–	3.7	–	mA	T = 25 °C
SID16	I <sub>DD11</sub>	Execute from Flash; CPU at 24 MHz	–	6.7	–	mA	T = 25 °C
SID17	I <sub>DD12</sub>	Execute from Flash; CPU at 24 MHz	–	–	7.2	mA	

#### Note

- Usage above the absolute maximum conditions listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.



**Table 5. GPIO AC Specifications (Guaranteed by Characterization)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	$T_{RISEF}$	Rise time in fast strong mode	2	–	12	ns	3.3-V $V_{DDD}$ , Clload = 25 pF
SID71	$T_{FALLF}$	Fall time in fast strong mode	2	–	12	ns	3.3-V $V_{DDD}$ , Clload = 25 pF
SID72	$T_{RISES}$	Rise time in slow strong mode	10	–	60		3.3-V $V_{DDD}$ , Clload = 25 pF
SID73	$T_{FALLS}$	Fall time in slow strong mode	10	–	60		3.3-V $V_{DDD}$ , Clload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout; 3.3 V $\leq V_{DDD} \leq 5.5$ V. Fast strong mode.	–	–	24	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; 1.7 V $\leq V_{DDD} \leq 3.3$ V. Fast strong mode.	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; 3.3 V $\leq V_{DDD} \leq 5.5$ V. Slow strong mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout; 1.7 V $\leq V_{DDD} \leq 3.3$ V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	$F_{GPIOIN}$	GPIO input operating frequency; 1.71 V $\leq V_{DDD} \leq 5.5$ V	–	–	24	MHz	90/10% $V_{IO}$

### XRES

**Table 6. XRES DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	$V_{IH}$	Input voltage high threshold	$0.7 \times V_{DDD}$	–	–	V	CMOS Input
SID78	$V_{IL}$	Input voltage low threshold	–	–	$0.3 \times V_{DDD}$	V	CMOS Input
SID79	$R_{PULLUP}$	Pull-up resistor	3.5	5.6	8.5	k $\Omega$	
SID80	$C_{IN}$	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	$I_{DIODE}$	Current through protection diode to $V_{DDD}/V_{SS}$	–	–	100	$\mu$ A	Guaranteed by characterization

**Table 7. XRES AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	$\mu$ s	Guaranteed by characterization

### Analog Peripherals

#### Opamp

**Table 8. Opamp Specifications (Guaranteed by Characterization)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	$I_{DD}$	Opamp block current. No load.	–	–	–	–	
SID269	$I_{DD\_HI}$	Power = high	–	1100	1850	$\mu A$	
SID270	$I_{DD\_MED}$	Power = medium	–	550	950	$\mu A$	
SID271	$I_{DD\_LOW}$	Power = low	–	150	350	$\mu A$	
	GBW	Load = 20 pF, 0.1 mA. $V_{DDA} = 2.7 V$	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	$I_{OUT\_MAX}$	$V_{DDA} \geq 2.7 V$ , 500 mV from rail	–	–	–	–	
SID275	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
	$I_{OUT}$	$V_{DDA} = 1.71 V$ , 500 mV from rail	–	–	–	–	
SID278	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID281	$V_{IN}$	Charge pump on, $V_{DDA} \geq 2.7 V$	–0.05	–	$V_{DDA} - 0.2$	V	
SID282	$V_{CM}$	Charge pump on, $V_{DDA} \geq 2.7 V$	–0.05	–	$V_{DDA} - 0.2$	V	
	$V_{OUT}$	$V_{DDA} \geq 2.7 V$	–	–	–	–	
SID283	$V_{OUT\_1}$	Power = high, Iload=10 mA	0.5	–	$V_{DDA} - 0.5$	V	
SID284	$V_{OUT\_2}$	Power = high, Iload=1 mA	0.2	–	$V_{DDA} - 0.2$	V	
SID285	$V_{OUT\_3}$	Power = medium, Iload=1 mA	0.2	–	$V_{DDA} - 0.2$	V	
SID286	$V_{OUT\_4}$	Power = low, Iload=0.1mA	0.2	–	$V_{DDA} - 0.2$	V	
SID288	$V_{OS\_TR}$	Offset voltage, trimmed	1	$\pm 0.5$	1	mV	High mode
SID288A	$V_{OS\_TR}$	Offset voltage, trimmed	–	$\pm 1$	–	mV	Medium mode
SID288B	$V_{OS\_TR}$	Offset voltage, trimmed	–	$\pm 2$	–	mV	Low mode
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	$\pm 3$	10	$\mu V/^{\circ}C$	High mode $T_A \leq 85^{\circ}C$ .
SID290Q	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–15	$\pm 3$	15	$\mu V/^{\circ}C$	High mode. $T_A \leq 105^{\circ}C$
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	$\pm 10$	–	$\mu V/^{\circ}C$	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	$\pm 10$	–	$\mu V/^{\circ}C$	Low mode
SID291	CMRR	DC	70	80	–	dB	$V_{DDD} = 3.6 V$
SID292	PSRR	At 1 kHz, 100 mV ripple	70	85	–	dB	$V_{DDD} = 3.6 V$
	Noise		–	–	–	–	
SID293	$V_{N1}$	Input referred, 1 Hz - 1GHz, power = high	–	94	–	$\mu V_{rms}$	
SID294	$V_{N2}$	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	
SID295	$V_{N3}$	Input referred, 10 kHz, power = high	–	28	–	nV/rtHz	
SID296	$V_{N4}$	Input referred, 100 kHz, power = high	–	15	–	nV/rtHz	

**Table 10. Comparator AC Specifications**

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T <sub>RESP1</sub>	Response time, normal mode	–	–	110	ns	50 mV overdrive
SID258	T <sub>RESP2</sub>	Response time, low power mode	–	–	200	ns	50 mV overdrive
SID92	T <sub>RESP3</sub>	Response time, ultra low power mode (V <sub>DDD</sub> ≥ 2.2 V for Temp < 0 °C, V <sub>DDD</sub> ≥ 1.8 V for Temp > 0 °C)	–	–	15	µs	200 mV overdrive

### Temperature Sensor

**Table 11. Temperature Sensor Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	T <sub>SENSACC</sub>	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

### SAR ADC

**Table 12. SAR ADC DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	8		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference. Guaranteed by characterization
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V <sub>REF</sub> . Guaranteed by characterization
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

**Table 13. SAR ADC AC Specifications (Guaranteed by Characterization)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	1	Msp	
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = $V_{DD}$	–	–	806	Ksp	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	Ksp	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	$F_{IN} = 10$ kHz
SID111	A_INL	Integral non linearity	–1.7	–	+2	LSB	$V_{DD} = 1.71$ to 5.5, 806 Ksp, $V_{ref} = 1$ to 5.5. $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
			–1.9	–	+2	LSB	$V_{DD} = 1.71$ to 5.5, 806 Ksp, $V_{ref} = 1$ to 5.5. $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID111A	A_INL	Integral non linearity	–1.5	–	+1.7	LSB	$V_{DDD} = 1.71$ to 3.6, 806 Ksp, $V_{ref} = 1.71$ to $V_{DDD}$ . $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
			–1.9	–	+2	LSB	$V_{DDD} = 1.71$ to 3.6, 806 Ksp, $V_{ref} = 1.71$ to $V_{DDD}$ . $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID111B	A_INL	Integral non linearity	–1.5	–	+1.7	LSB	$V_{DDD} = 1.71$ to 5.5, 500 Ksp, $V_{ref} = 1$ to 5.5.
SID112	A_DNL	Differential non linearity	–1	–	+2.2	LSB	$V_{DDD} = 1.71$ to 5.5, 806 Ksp, $V_{ref} = 1$ to 5.5. $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
			–1	–	+2.3	LSB	$V_{DDD} = 1.71$ to 5.5, 806 Ksp, $V_{ref} = 1$ to 5.5. $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID112A	A_DNL	Differential non linearity	–1	–	+2	LSB	$V_{DDD} = 1.71$ to 3.6, 806 Ksp, $V_{ref} = 1.71$ to $V_{DDD}$ . $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
			–1	–	+2.2	LSB	$V_{DDD} = 1.71$ to 3.6, 806 Ksp, $V_{ref} = 1.71$ to $V_{DDD}$ . $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$
SID112B	A_DNL	Differential non linearity	–1	–	+2.2	LSB	$V_{DDD} = 1.71$ to 5.5, 500 Ksp, $V_{ref} = 1$ to 5.5.
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	$F_{IN} = 10$ kHz.

CSD

**Table 14. CSD Block Specification**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
<b>CSD Specification</b>							
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8-bits) in High range	–	612	–	μA	
SID314A	IDAC1_CRT2	Output current of Idac1(8-bits) in Low range	–	306	–	μA	
SID315	IDAC2_CRT1	Output current of Idac2 (7-bits) in High range	–	304.8	–	μA	
SID315A	IDAC2_CRT2	Output current of Idac2 (7-bits) in Low range	–	152.4	–	μA	

### Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Timer/Counter/PWM

**Table 15. TCPWM Specifications**

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 24 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

### SPI Specifications

**Table 22. Fixed SPI DC Specifications (Guaranteed by Characterization)**

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID163	I <sub>SPI1</sub>	Block current consumption at 1 Mb/s/sec	–	–	360	μA
SID164	I <sub>SPI2</sub>	Block current consumption at 4 Mb/s/sec	–	–	560	μA
SID165	I <sub>SPI3</sub>	Block current consumption at 8 Mb/s/sec	–	–	600	μA

**Table 23. Fixed SPI AC Specifications (Guaranteed by Characterization)**

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID166	F <sub>SPI</sub>	SPI operating frequency (master; 6X oversampling)	–	–	4	MHz

**Table 24. Fixed SPI Master mode AC Specifications (Guaranteed by Characterization)**

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID167	T <sub>DMO</sub>	MOSI valid after S <sub>clock</sub> driving edge	–	–	15	ns
SID168	T <sub>DSI</sub>	MISO valid before S <sub>clock</sub> capturing edge. Full clock, late MISO Sampling used	20	–	–	ns
SID169	T <sub>HMO</sub>	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns

**Table 25. Fixed SPI Slave mode AC Specifications (Guaranteed by Characterization)**

Spec ID	Parameter	Description	Min	Typ	Max	Units
SID170	T <sub>DMI</sub>	MOSI valid before S <sub>clock</sub> capturing edge	40	–	–	ns
SID171	T <sub>DSO</sub>	MISO valid after S <sub>clock</sub> driving edge	–	–	42 + (3 × T <sub>scbclk</sub> )	ns
SID171A	T <sub>DSO_ext</sub>	MISO valid after S <sub>clock</sub> driving edge in Ext. Clock mode	–	–	48	ns
SID172	T <sub>HSO</sub>	Previous MISO data hold time	0	–	–	ns
SID172A	T <sub>SSEL<sub>SCK</sub></sub>	SSEL Valid to first SCK Valid edge	100	–	–	ns



## Memory

**Table 26. Flash DC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V <sub>PE</sub>	Erase and program voltage	1.71	–	5.5	V	

**Table 27. Flash AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T <sub>ROWWRITE</sub> <sup>[3]</sup>	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes. –40 °C ≤ T <sub>A</sub> ≤ 85 °C
			–	–	26	ms	Row (block) = 128 bytes. –40 °C ≤ T <sub>A</sub> ≤ 105 °C
SID175	T <sub>ROWERASE</sub> <sup>[3]</sup>	Row erase time	–	–	13	ms	
SID176	T <sub>ROWPROGRAM</sub> <sup>[3]</sup>	Row program time after erase	–	–	7	ms	–40 °C ≤ T <sub>A</sub> ≤ 85 °C
			–	–	13	ms	–40 °C ≤ T <sub>A</sub> ≤ 105 °C
SID178	T <sub>BULKERASE</sub> <sup>[3]</sup>	Bulk erase time (32 KB)	–	–	35	ms	
SID180	T <sub>DEVPROG</sub> <sup>[3]</sup>	Total device program time	–	–	7	seconds	Guaranteed by characterization
SID181	F <sub>END</sub>	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F <sub>RET</sub>	Flash retention. T <sub>A</sub> ≤ 55 °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. T <sub>A</sub> ≤ 85 °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	F <sub>RETQ</sub>	Flash retention. T <sub>A</sub> ≤ 105 °C, 10K P/E cycles, ≤ three years at T <sub>A</sub> ≥ 85 °C.	10	20	–		Guaranteed by characterization.

## System Resources

*Power-on-Reset (POR) with Brown Out*

**Table 28. Imprecise Power On Reset (PRES)**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	V <sub>RISEIPOR</sub>	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	V <sub>FALLIPOR</sub>	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization
SID187	V <sub>IPORHYST</sub>	Hysteresis	15	–	200	mV	Guaranteed by characterization

**Table 29. Precise Power On Reset (POR)**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	V <sub>FALLPPOR</sub>	BOD trip voltage in active and sleep modes	1.64	–	–	V	Full functionality between 1.71 V and BOD trip voltage is guaranteed by characterization
SID192	V <sub>FALLDPSLP</sub>	BOD trip voltage in Deep Sleep	1.4	–	–	V	Guaranteed by characterization
BID55	Svdd	Maximum power supply ramp rate	–	–	67	kV/sec	

### Note

- It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

### Voltage Monitors

**Table 30. Voltage Monitors DC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID195	V <sub>LVI1</sub>	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	
SID196	V <sub>LVI2</sub>	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	
SID197	V <sub>LVI3</sub>	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	
SID198	V <sub>LVI4</sub>	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	
SID199	V <sub>LVI5</sub>	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	
SID200	V <sub>LVI6</sub>	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	
SID201	V <sub>LVI7</sub>	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	
SID202	V <sub>LVI8</sub>	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	
SID203	V <sub>LVI9</sub>	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	
SID204	V <sub>LVI10</sub>	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	
SID205	V <sub>LVI11</sub>	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	
SID206	V <sub>LVI12</sub>	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	
SID207	V <sub>LVI13</sub>	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	
SID208	V <sub>LVI14</sub>	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	
SID209	V <sub>LVI15</sub>	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	
SID210	V <sub>LVI16</sub>	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	
SID211	LVI_IDD	Block current	–	–	100	μA	Guaranteed by characterization

**Table 31. Voltage Monitors AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID212	T <sub>MONTRIP</sub>	Voltage monitor trip time	–	–	1	μs	Guaranteed by characterization

### SWD Interface

**Table 32. SWD Interface Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F <sub>SWDCLK1</sub>	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F <sub>SWDCLK2</sub>	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T <sub>SWDI_SETUP</sub>	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T <sub>SWDI_HOLD</sub>	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T <sub>SWDO_VALID</sub>	T = 1/f SWDCLK	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T <sub>SWDO_HOLD</sub>	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

### Internal Main Oscillator

**Table 33. IMO DC Specifications (Guaranteed by Design)**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID219	I <sub>IMO2</sub>	IMO operating current at 24 MHz	–	–	325	μA	
SID220	I <sub>IMO3</sub>	IMO operating current at 12 MHz	–	–	225	μA	
SID221	I <sub>IMO4</sub>	IMO operating current at 6 MHz	–	–	180	μA	
SID222	I <sub>IMO5</sub>	IMO operating current at 3 MHz	–	–	150	μA	

**Table 34. IMO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F <sub>IMOTOL1</sub>	Frequency variation from 3 to 24 MHz	–	–	±2	%	+3% if T <sub>A</sub> > 85 °C and IMO frequency < 24 MHz
SID226	T <sub>STARTIMO</sub>	IMO startup time	–	–	12	μs	
SID227	T <sub>JITRMSIMO1</sub>	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	T <sub>JITRMSIMO2</sub>	RMS Jitter at 24 MHz	–	145	–	ps	

### Internal Low-Speed Oscillator

**Table 35. ILO DC Specifications (Guaranteed by Design)**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I <sub>ILO1</sub>	ILO operating current at 32 kHz	–	0.3	1.05	μA	Guaranteed by Characterization
SID233	I <sub>ILOLEAK</sub>	ILO leakage current	–	2	15	nA	Guaranteed by Design

**Table 36. ILO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	T <sub>STARTILO1</sub>	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	T <sub>ILODUTY</sub>	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	F <sub>ILOTRIM1</sub>	32 kHz trimmed frequency	15	32	50	kHz	Max. ILO frequency is 70 kHz if T <sub>A</sub> > 85 °C

**Table 37. External Clock Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	24	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at V <sub>DD/2</sub>	45	–	55	%	Guaranteed by characterization

The field values are listed in Table 40.

**Table 40. Field Values**

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family within architecture	1	4100 Family
		2	4200 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
DE	Package Code	PV	SSOP
F	Temperature Range	A/S	Automotive
GHI	Attributes Code	000-999	Code of feature set in specific family
Z	Fab location change		

## Packaging

**Table 41. Package Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Operating ambient temperature	For A grade devices	–40	25.00	85	°C
T <sub>A</sub>	Operating ambient temperature	For S grade devices	–40	25.00	105	°C
T <sub>J</sub>	Operating junction temperature	For A grade devices	–40	–	100	°C
T <sub>J</sub>	Operating junction temperature	For S grade devices	–40	–	120	°C
T <sub>JA</sub>	Package $\theta_{JA}$ (28-pin SSOP)		–	66.58	–	°C/W
T <sub>JC</sub>	Package $\theta_{JC}$ (28-pin SSOP)		–	46.28	–	°C/W

**Table 42. Solder Reflow Peak Temperature**

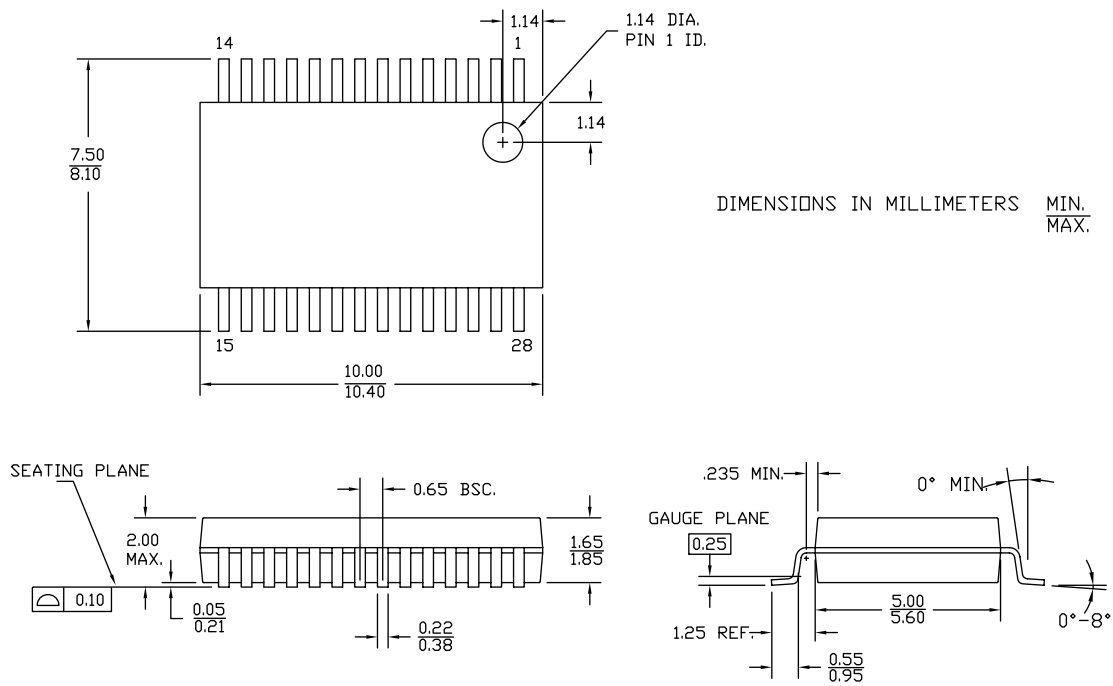
Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
28-pin SSOP	260 °C	30 seconds

**Table 43. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

Package	MSL
28-pin SSOP	MSL 3

PSoC4 CAB Libraries with Schematics Symbols and PCB Footprints are on the Cypress web site at [http://www.cypress.com/cad-resources/psoc-4-cad-libraries?source=search&cat=technical\\_documents](http://www.cypress.com/cad-resources/psoc-4-cad-libraries?source=search&cat=technical_documents)

**Figure 6. 28-pin SSOP (210 Mils) Package Outline**



51-85079 \*F

**Table 44. Acronyms Used in this Document** *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC <sup>®</sup>	Programmable System-on-Chip <sup>™</sup>
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA

**Table 44. Acronyms Used in this Document** *(continued)*

Acronym	Description
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal



## Document Conventions

### Units of Measure

**Table 45. Units of Measure**

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
Ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt