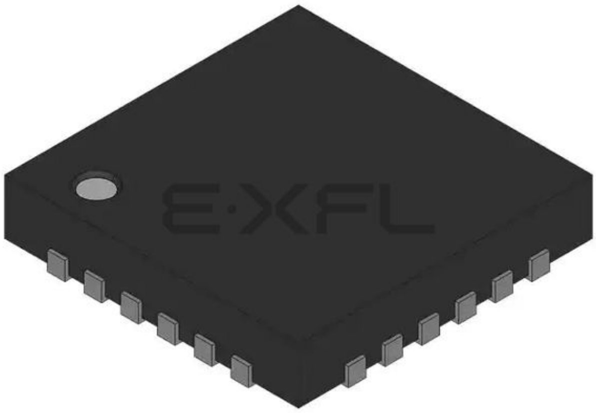


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

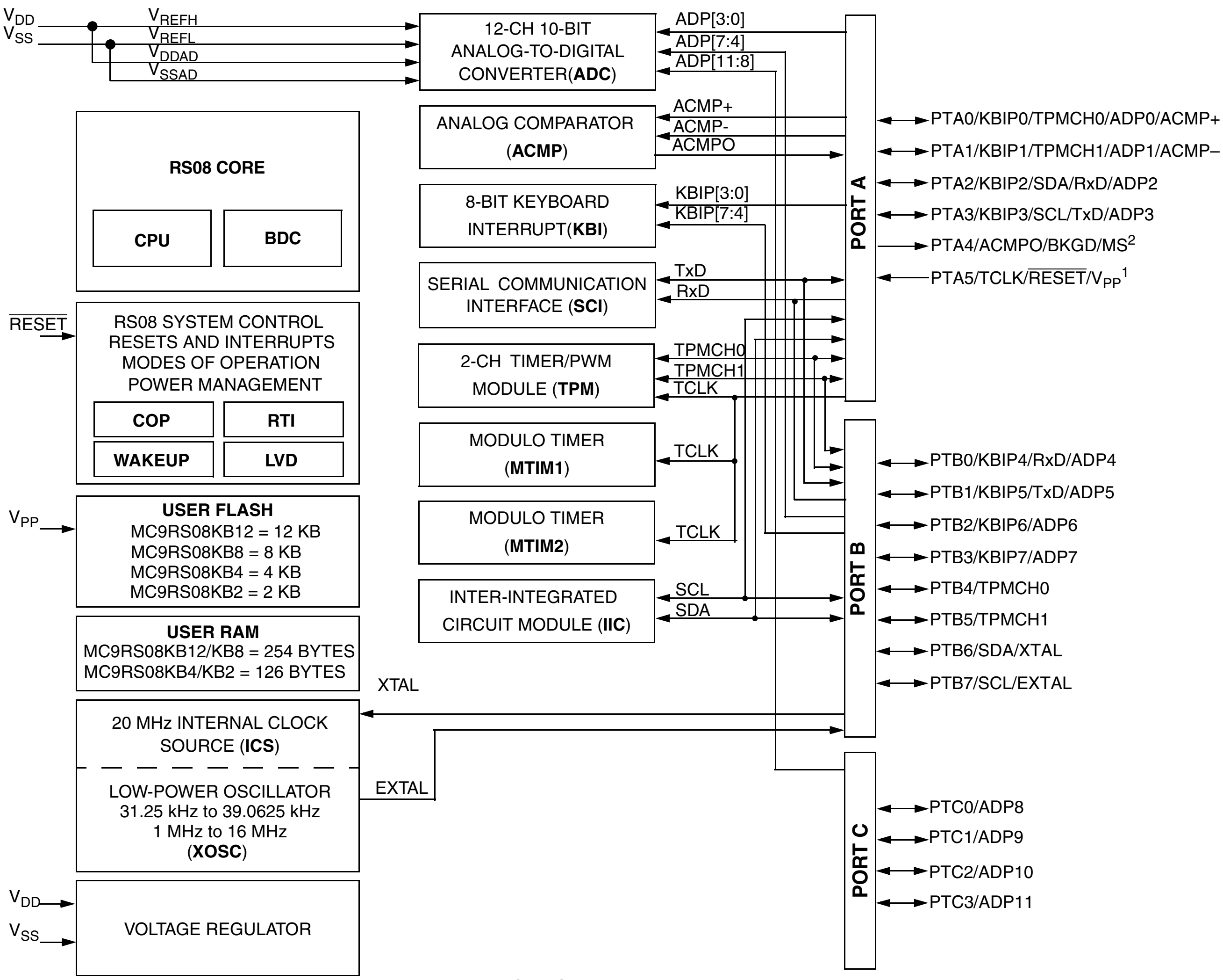
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	254 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN-EP (4x4)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9rs08kb12cfk

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9RS08KB12 MCU.



NOTES:
1. PTA5/TCLK/$\overline{\text{RESET}}$/V_{PP} is an input-only pin when used as port pin
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin

Figure 1. MC9RS08KB12 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08KB12 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number				<-- Lowest **Priority** --> Highest				
24	**20**	**16**	**8**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	3	3	3					V_{DD}
2	—	—	—	NC				
3	4	4	4					V_{SS}
4	5	5	—	PTB7	SCL[1]			EXTAL
5	6	6	—	PTB6	SDA[1]			XTAL
6	7	7	—	PTB5	TPMCH1[2]			
7	8	8	—	PTB4	TPMCH0[2]			
8	9	—	—	PTC3			ADP11	
9	10	—	—	PTC2			ADP10	
10	11	—	—	PTC1			ADP9	
11	12	—	—	PTC0			ADP8	
12	13	9	—	PTB3	KBIP7		ADP7	
13	14	10	—	PTB2	KBIP6		ADP6	
14	15	11	—	PTB1	KBIP5	TxD[3]	ADP5	
15	16	12	—	PTB0	KBIP4	RxD[3]	ADP4	
16	17	13	5	PTA3	KBIP3	SCL[1]	TxD[3]	ADP3
17	18	14	6	PTA2	KBIP2	SDA[1]	RxD[3]	ADP2
18	19	15	7	PTA1	KBIP1	TPMCH1[2]	ADP1	ACMP–
19	20	16	8	PTA0	KBIP0	TPMCH0[2]	ADP0	ACMP+
20	—	—	—	NC				
21	—	—	—	NC				
22	—	—	—	NC				
23	1	1	1	PTA5		TCLK	$\overline{\text{RESET}}$	V_{PP}
24	2	2	2	PTA4	ACMPO	BKGD	MS	

[1] IIC pins can be remapped to PTB6 and PTB7, default reset location is PTA2 and PTA3. It can be configured only once.

[2] TPM pins can be remapped to PTB4 and PTB5, default reset location is PTA0 and PTA1.

[3] SCI pins can be remapped to PTA2 and PTA3, default reset location is PTB0 and PTB1. It can be configured only once.

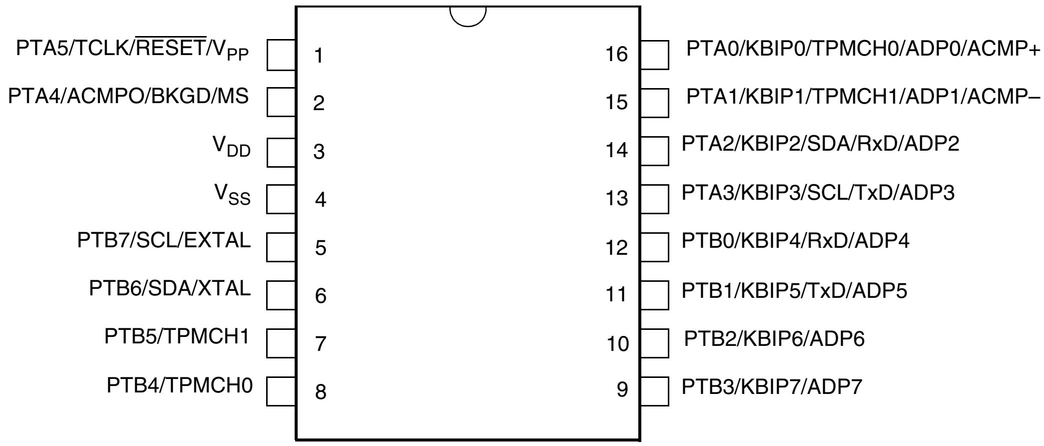


Figure 4. MC9RS08KB12 Series 16-Pin SOIC NB/TSSOP Package

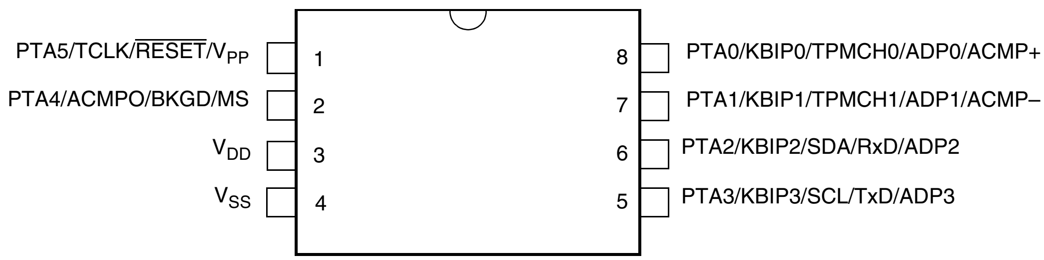


Figure 5. MC9RS08KB12 Series 8-Pin SOIC/DFN Package

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9RS08KB12 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.

Table 2. Parameter Classifications

D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{\text{RESET}}/V_{PP}$ pin which is internally clamped to V_{SS} only.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external VDD load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient)

No.	C	Parameter	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage (run, wait and stop modes.) 0 < f_{Bus} <10 MHz	V_{DD}	1.8	—	5.5	V
2	C	Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	0.8[1]	—	—	V
3	P	Low-voltage detection threshold (V_{DD} falling) (V_{DD} rising)	V_{LVD}	1.80 1.88	1.86 1.94	1.95 2.05	V
4	C	Power on RESET (POR) voltage	V_{POR}[1]	0.9	—	1.7	V
5	C	Input high voltage (V_{DD} > 2.3V) (all digital inputs)	V_{IH}	$0.70 \times V_{DD}$	—	—	V
6	C	Input high voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IH}	$0.85 \times V_{DD}$	—	—	V
7	C	Input low voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IL}	—	—	$0.30 \times V_{DD}$	V
8	C	Input low voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IL}	—	—	$0.30 \times V_{DD}$	V
9	C	Input hysteresis (all digital inputs)	V_{hys}[1]	$0.06 \times V_{DD}$	—	—	V
10	P	Input leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS}, all input only pins	$\|I_{In}\|$	—	0.025	1.0	µA
11	P	High impedance (off-state) leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS}, all input/output	$\|I_{OZ}\|$	—	0.025	1.0	µA
12	P	Internal pullup resistors[2](all port pins)	R_{PU}	20	45	65	kΩ
13	P	Internal pulldown resistors[2](all port pins)	R_{PD}	20	45	65	kΩ
14	C	Output high voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA 1.8 V, I_{Load} = 0.5 mA	V_{OH}	$V_{DD} - 0.8$	— — —	— — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 3 mA 1.8 V, I_{Load} = 2 mA		$V_{DD} - 0.8$	— — —	— — —	
15	C	Maximum total I_{OH} for all port pins	$\|I_{OHT}\|$	—	—	40	mA

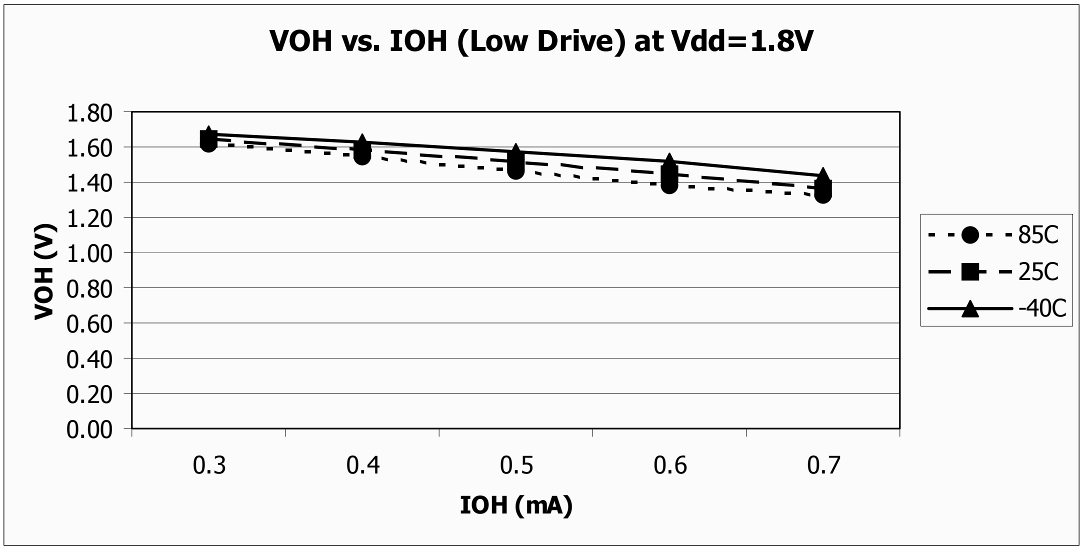


Figure 11. Typical V_{OH} vs. I_{OH}
V_{DD} = 1.8 V (Low Drive)

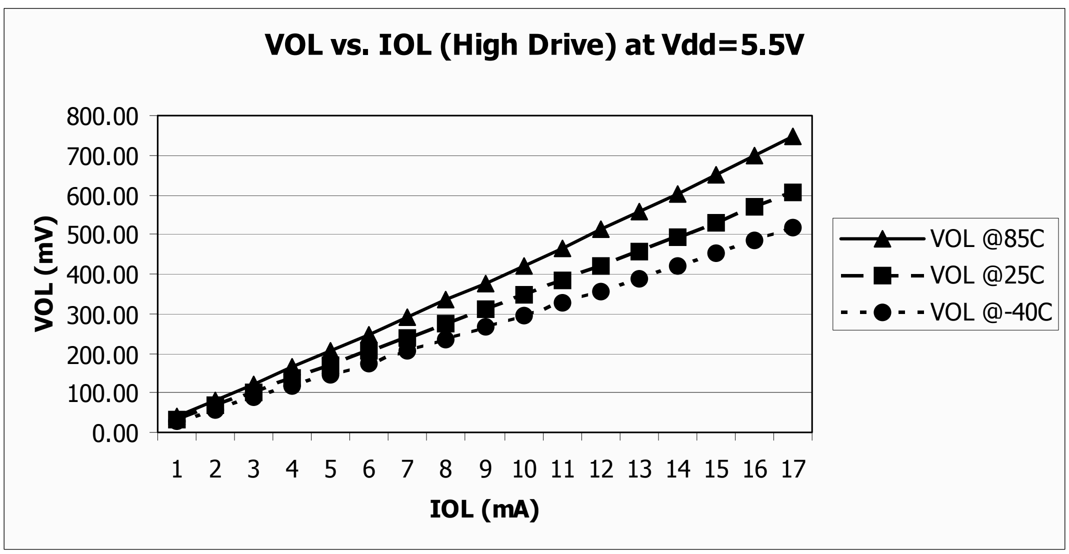


Figure 12. Typical V_{OL} vs. I_{OL}
V_{DD} = 5.5 V (High Drive)

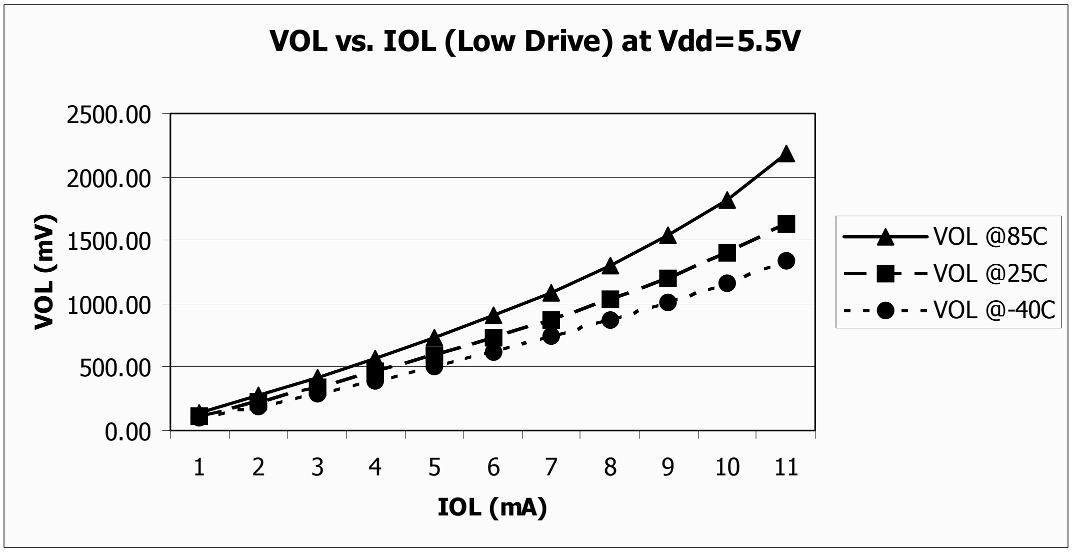


Figure 13. Typical V_{OL} vs. I_{OL}
V_{DD} = 5.5 V (Low Drive)

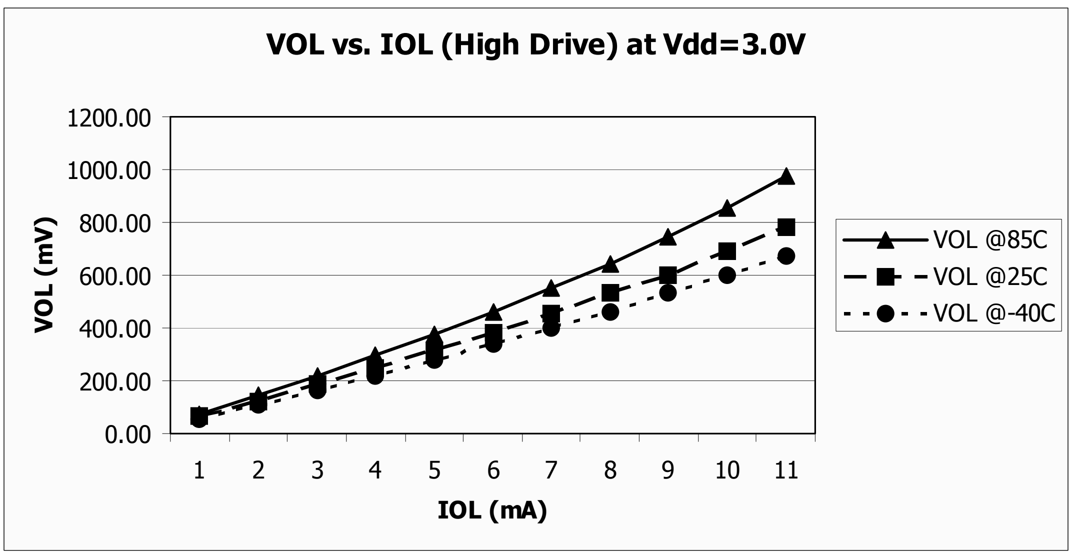


Figure 14. Typical V_{OL} vs. I_{OL}
V_{DD} = 3.0 V (High Drive)

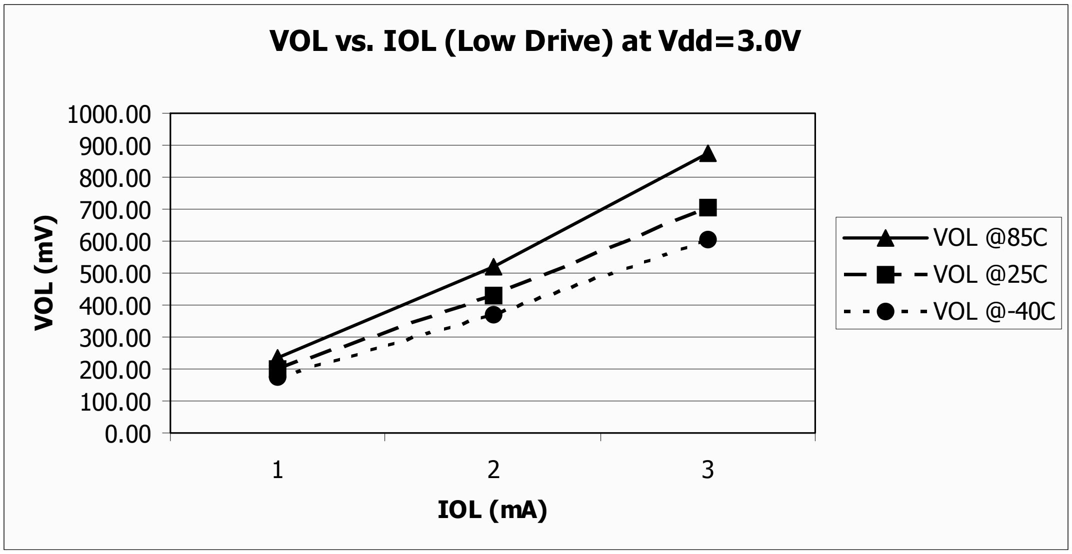


Figure 15. Typical V_{OL} vs. I_{OL}
V_{DD} = 3.0 V (Low Drive)

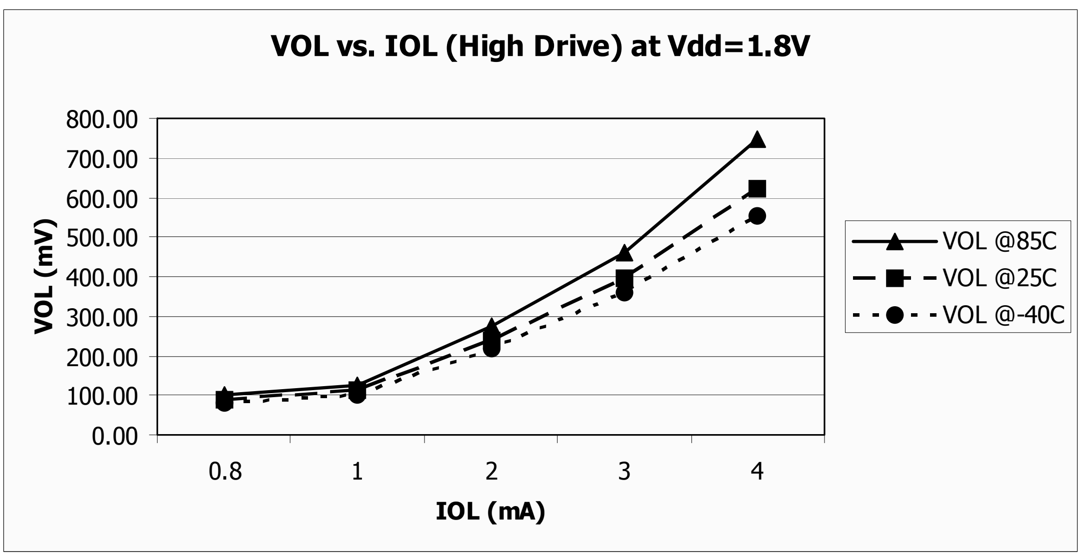


Figure 16. Typical V_{OL} vs. I_{OL}
V_{DD} = 1.8 V (High Drive)

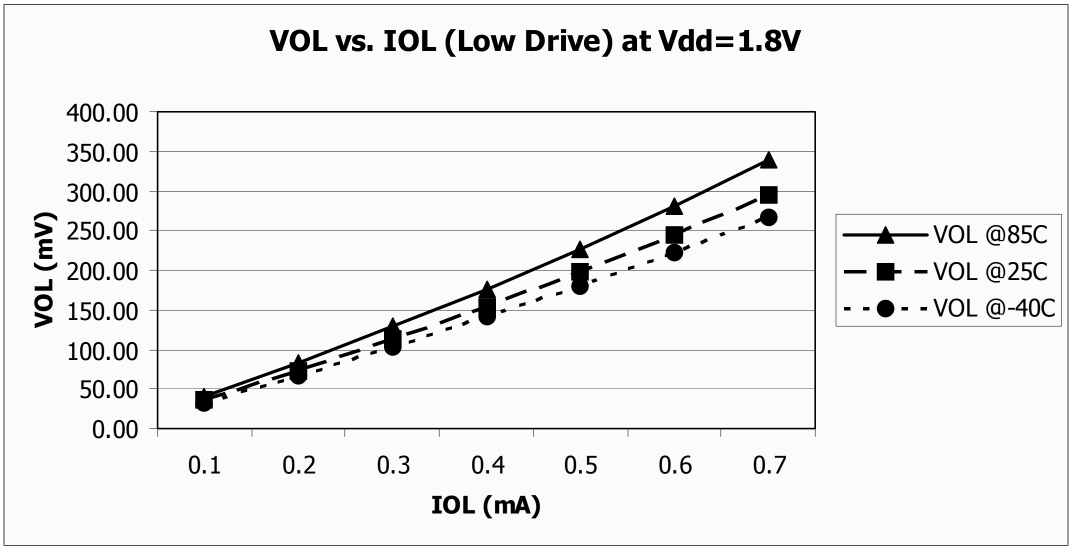


Figure 17. Typical V_{OL} vs. I_{OL}
V_{DD} = 1.8 V (Low Drive)

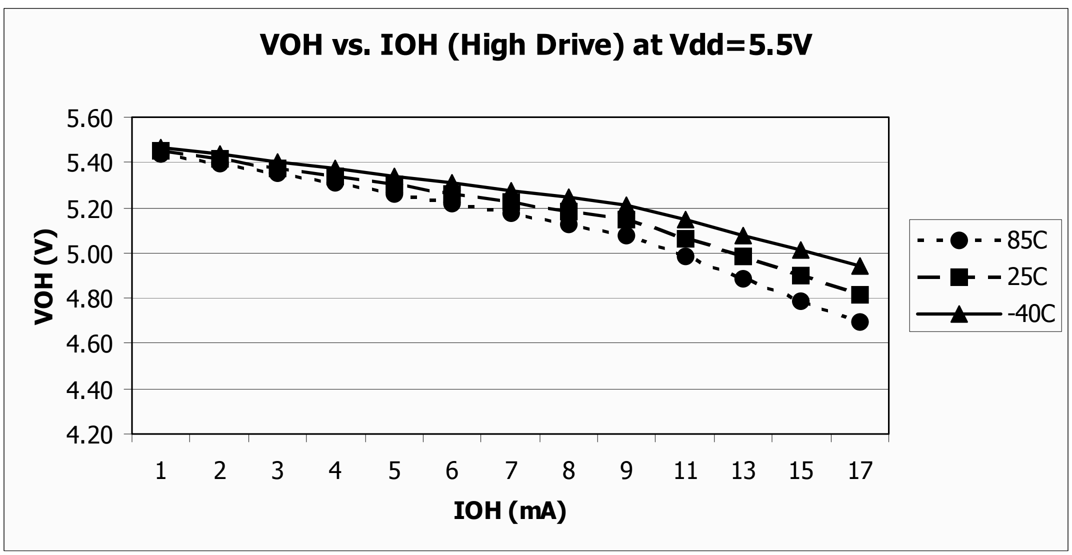


Figure 18. Typical I_{OH} vs. V_{DD}–V_{OH}
V_{DD} = 5.5 V (High Drive)

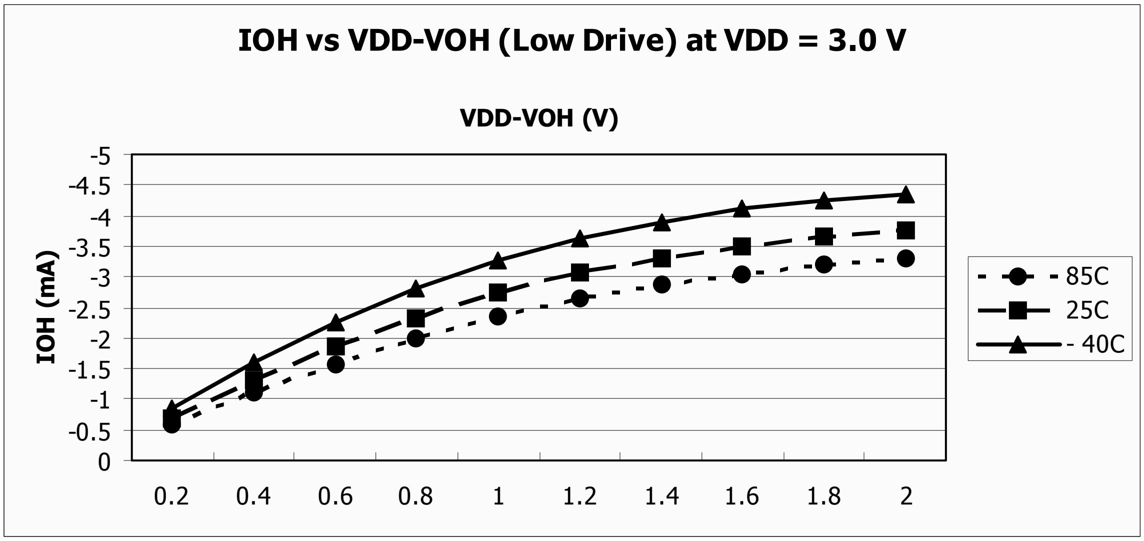


Figure 21. Typical I_{OH} vs. V_{DD}–V_{OH}
V_{DD} = 3 V (Low Drive)

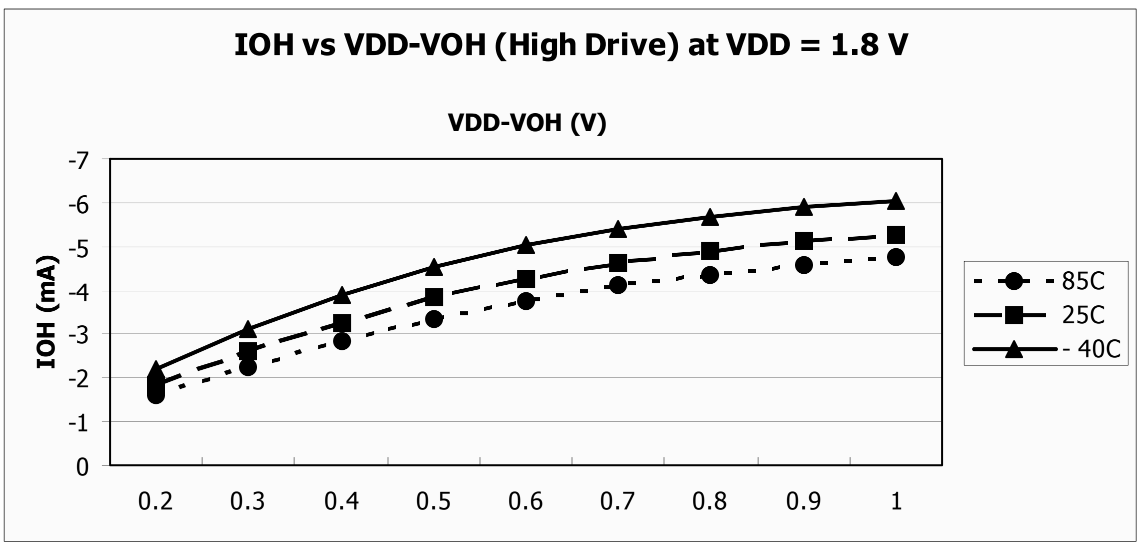


Figure 22. Typical I_{OH} vs. V_{DD}–V_{OH}
V_{DD} = 1.8 V (High Drive)

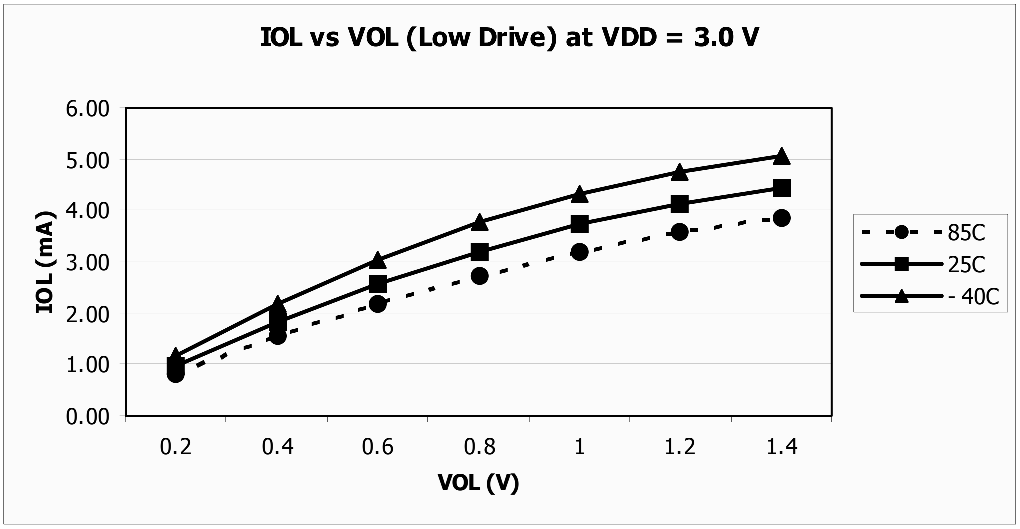


Figure 27. Typical I_{OL} vs. V_{OL}
V_{DD} = 3 V (Low Drive)

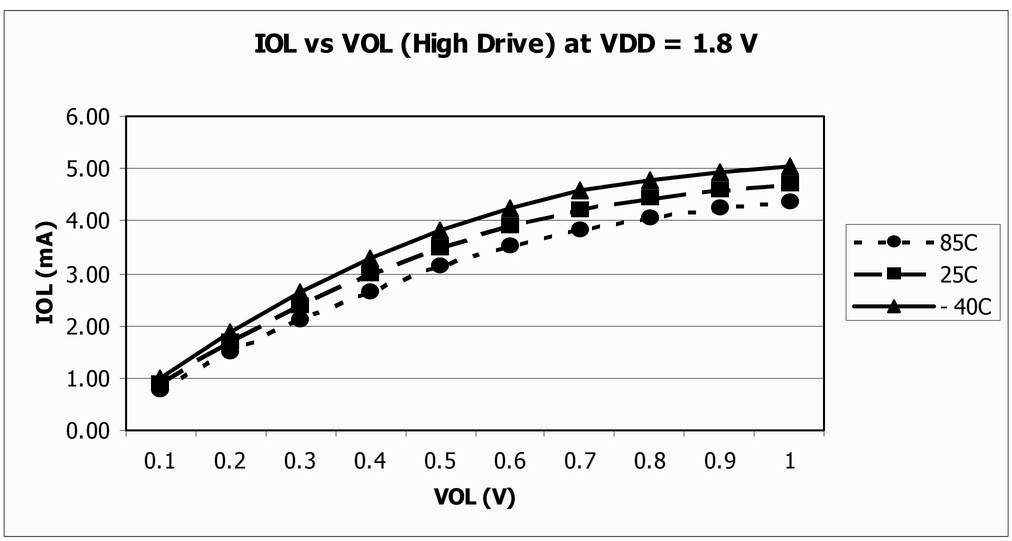


Figure 28. Typical I_{OL} vs. V_{OL}
V_{DD} = 1.8 V (High Drive)

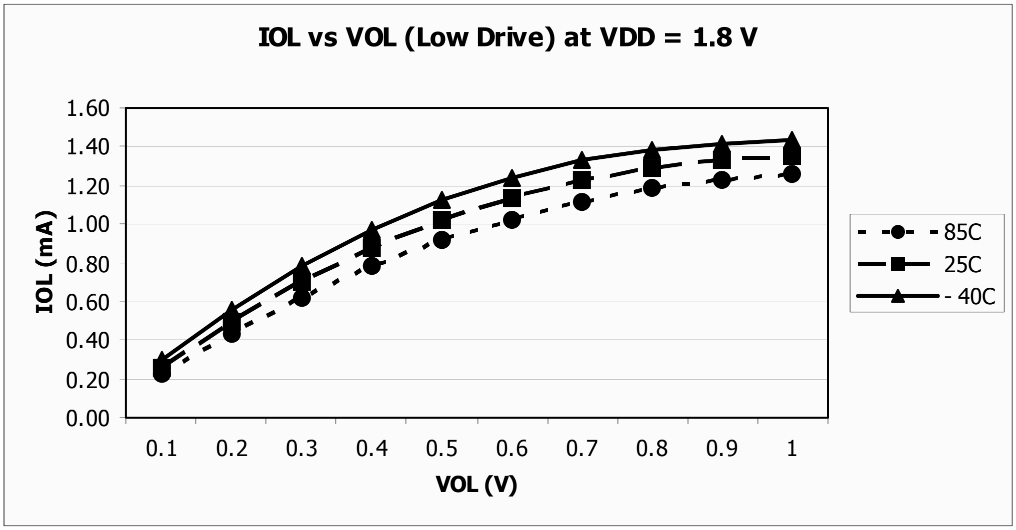


Figure 29. Typical I_{OL} vs. V_{OL}
V_{DD} = 1.8 V (Low Drive)

3.7 Supply Current Characteristics

Table 8. Supply Current Characteristics

N	C	Parameter	Symbol	V_{DD} (V)	Typical	Max[1]	Temp. (°C)	Unit
1	P	Run supply current[2] measured at (f_{Bus} = 10 MHz)	RI_{DD10}	5	3.45 3.48 3.53	7	–40 25 85	mA
2	C			3	3.39 3.42 3.49	—	–40 25 85	
3	C			1.80	2.40 2.42 2.44	—	–40 25 85	
4	C	Run supply current[3] measured at (f_{Bus} = 1.25 MHz)	RI_{DD1}	5	0.93 0.96 0.99	—	–40 25 85	mA
5	T			3	0.91 0.92 0.92	—	–40 25 85	
6	T			1.80	0.66 0.67 0.68	—	–40 25 85	

Table 8. Supply Current Characteristics (continued)

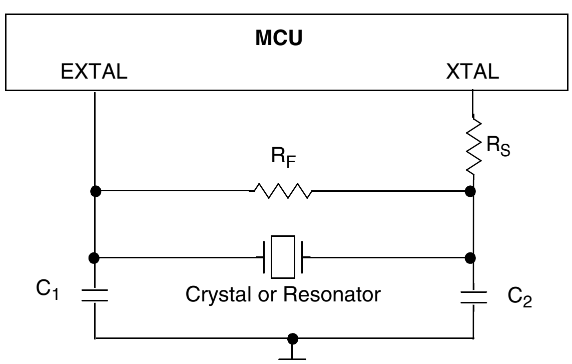
N	C	Parameter	Symbol	V_{DD} (V)	Typical	Max[1]	Temp. (°C)	Unit
7	C	Wait mode supply current[3] measured at (f_{Bus} = 2.00 MHz)	WI_{DD2}	5	841.13 859.98 873.69	—	–40 25 85	µA
8	T			3	840.21 850.60 846.67	—	–40 25 85	
9	T			1.80	630.64 635.10 643.67	—	–40 25 85	
10	C	Wait mode supply current[3] measured at (f_{Bus} = 1.00 MHz)	WI_{DD1}	5	667.86 683.38 688.02	—	–40 25 85	µA
11	T			3	666.34 672.79 669.15	—	–40 25 85	
12	T			1.80	505.39 509.28 502.52	—	–40 25 85	
13	P	Stop mode supply current	SI_{DD}	5	1.15 1.40 7.67	11	–40 25 85	µA
14	C			3	1.05 1.26 4.52	—	–40 25 85	
15	C			1.80	0.39 0.56 4.21	—	–40 25 85	
16	C	ADC adder from stop[3]	—	5	128.86 140.44 154.97	—	–40 25 85	µA
17	T			3	102.98 111.71 118.33	—	–40 25 85	
18	T			1.80	54.77 66.33 74.42	—	–40 25 85	
19	C	ACMP adder from stop (ACME = 1)	—	5	14.43 15.96 16.77	—	–40 25 85	µA
20	T			3	14.37 14.72 14.45	—	–40 25 85	
21	T			1.80	13.05 14.02 12.92	—	–40 25 85	

3.8 External Oscillator (XOSC) Characteristics

Table 9. Oscillator Electrical Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode[2] High range (RANGE = 1, HGO = 1) FBELP mode High range (RANGE = 1, HGO = 0) FBELP mode	 f_{lo} f_{hi} $f_{hi\text{-}hgo}$ $f_{hi\text{-}lp}$	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1, C_2	See crystal or resonator manufacturer's recommendation.			
3	D	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F	 — —	 10 1	 — —	MΩ
4	D	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time[3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[4]	 $t_{CSTL\text{-}LP}$ $t_{CSTL\text{-}HGO}$ $t_{CSTH\text{-}LP}$ $t_{CSTH\text{-}HGO}$	 — — — —	 200 400 5 20	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode[2] FBELP mode	f_{extal}	 0.03125 0	 — —	 5 40	MHz

[1] Typical data was characterized at 5.0 V, 25 °C or is recommended value.
[2] The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
[3] This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.
[4] 4 MHz crystal.



3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

Table 14. 10-Bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
ADC conversion clock Freq.	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC=1)		0.4	—	4.0		

[1] Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

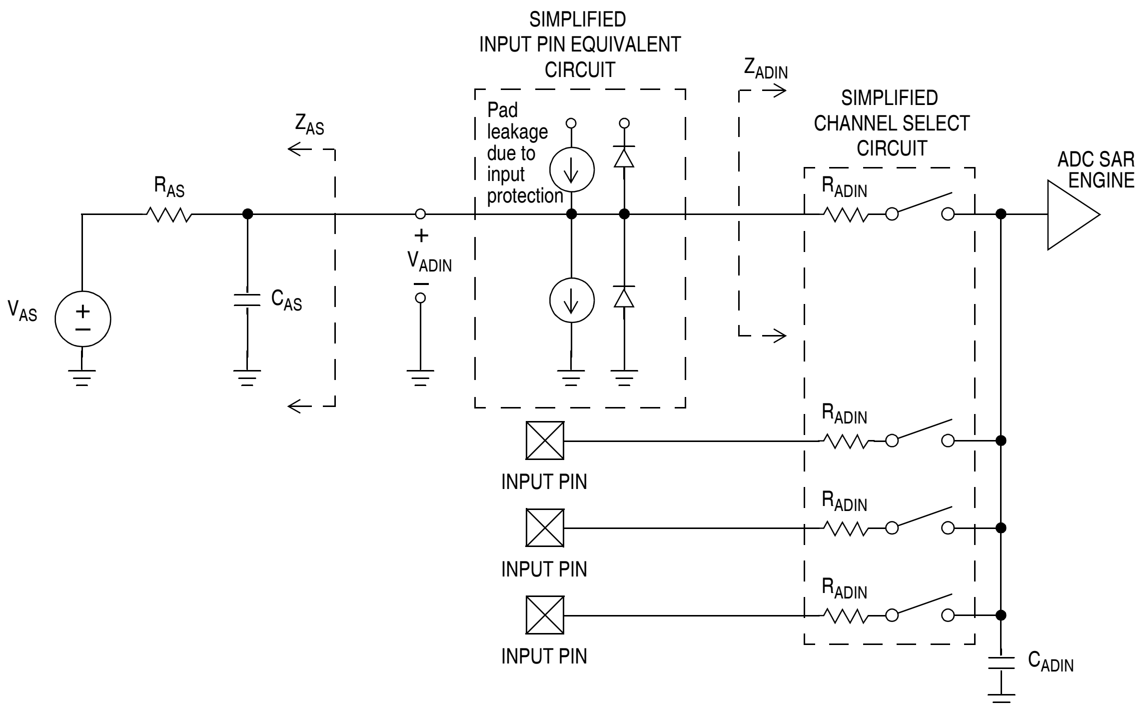


Figure 34. ADC Input Impedance Equivalency Diagram

Table 15. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 2.7 V < V_{DDAD} < 5.5 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	133	—	µA	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	218	—	µA	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	327	—	µA	

Table 16. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 1.8 V < V_{DDAD} < 2.7 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	8-bit mode	I_{DDAD}	—	88	—	μA	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	8-bit mode	I_{DDAD}	—	152	—	μA	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	8-bit mode	I_{DDAD}	—	214	—	μA	
T	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	8-bit mode	I_{DDAD}	—	390	—	μA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	E_{TUE}	—	—	—	LSB[2]	Includes quantization
		8-bit mode		—	±3.5	—		
T	Differential Non-Linearity	10-bit mode	DNL	—	—	—	LSB[2]	
		8-bit mode		—	±1.0	—		
		Monotonicity and No-Missing-Codes guaranteed						
C	Integral Non-Linearity	10-bit mode	INL	—	—	—	LSB[2]	
		8-bit mode		—	±1.5	—		
C	Zero-Scale Error	10-bit mode	E_{ZS}	—	—	—	LSB[2]	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	±1.5	—		
C	Full-Scale Error	10-bit mode	E_{FS}	—	—	—	LSB[2]	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	±1.0	—		
D	Quantization Error	10-bit mode	E_Q	—	—	—	LSB[2]	
		8-bit mode		—	—	±0.5		

3.14 EMC Performance

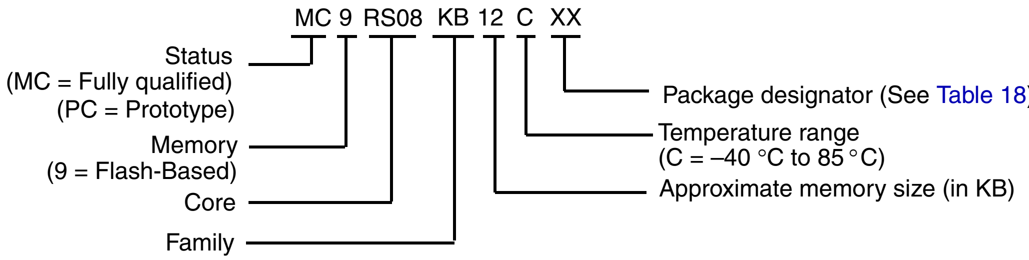
Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

4 Ordering Information

This section contains ordering numbers for MC9RS08KB12 series devices. See below for an example of the device numbering system.



5 Package Information and Mechanical Drawings

Table 18 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9RS08KB12 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 18, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 18) in the "Enter Keyword" search box at the top of the page.

Table 18. Device Numbering System

Device Number	Memory		Package		
	Flash	RAM	Type	Designator	Document No.
MC9RS08KB12 MC9RS08KB8 MC9RS08KB4	12 KB 8 KB 4 KB	254 bytes 254 bytes 126 bytes	24 QFN	FK	98ASA00087D
			20 SOIC WB	WJ	98ASB42343B
			16 SOIC NB	SG	98ASB42566B
			16 TSSOP	TG	98ASH70247A
MC9RS08KB2	2 KB	126 bytes	8 SOIC NB	SC	98ASB42564B
			8 DFN	DC	98ARL10557D

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MC9RS08KB12
Rev. 5
1/2012