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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	254 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9rs08kb12ctg

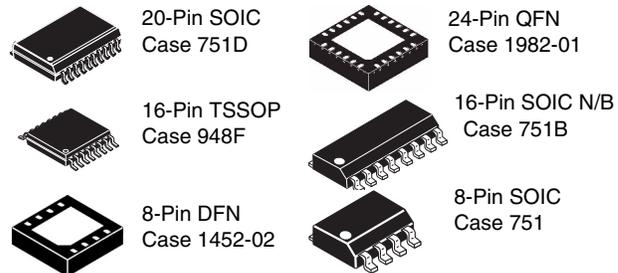
Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D



MC9RS08KB12

MC9RS08KB12 Series

Covers: MC9RS08KB12
MC9RS08KB8
MC9RS08KB4
MC9RS08KB2



- 8-Bit RS08 Central Processor Unit (CPU)
 - Up to 20 MHz CPU at 1.8 V to 5.5 V across temperature range of -40°C to 85°C
 - Subset of HC08 instruction set with added BGND instruction
 - Single Global interrupt vector
- On-Chip Memory
 - Up to 12 KB flash read/program/erase over full operating voltage and temperature, 12 KB/8 KB/4 KB/2 KB flash are optional
 - Up to 254-byte random-access memory (RAM), 254-byte/126-byte RAM are optional
 - Security circuitry to prevent unauthorized access to flash contents
- Power-Saving Modes
 - Wait mode — CPU shuts down; system clocks continue to run; full voltage regulation
 - Stop mode — CPU shuts down; system clocks are stopped; voltage regulator in standby
 - Wakeup from power-saving modes using RTI, KBI, ADC, ACMP, SCI and LVD
- Clock Source Options
 - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 1 MHz to 16 MHz
 - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies up to 10 MHz
- System Protection
 - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal low power oscillator
 - Low-voltage detection with reset or interrupt
 - Illegal opcode detection with reset
 - Illegal address detection with reset
 - Flash-block protection

- Development Support
 - Single-wire background debug interface
 - Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
 - **ADC** — 12-channel, 10-bit resolution; $2.5\ \mu\text{s}$ conversion time; automatic compare function; $1.7\ \text{mV}/^{\circ}\text{C}$ temperature sensor; internal bandgap reference channel; operation in stop; hardware trigger
 - **ACMP** — Analog comparator; full rail-to-rail supply operation; option to compare to fixed internal bandgap reference voltage; can operate in stop mode
 - **TPM** — One 2-channel timer/pulse-width modulator module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
 - **IIC** — Inter-integrated circuit bus module capable of operation up to 100 kbps with maximum bus loading; capable of higher baud rates with reduced loading
 - **SCI** — One serial communications interface module with optional 13-bit break; LIN extensions
 - **MTIM** — Two 8-bit modulo timers; optional clock sources
 - **RTI** — One real-time clock with optional clock sources
 - **KBI** — Keyboard interrupts; up to 8 ports
- Input/Output
 - 18 GPIOs in 24- and 20-pin packages; 14 GPIOs in 16-pin package; 6 GPIOs in 8-pin package; including one output-only pin and one input-only pin
 - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package Options
 - MC9RS08KB12/MC9RS08KB8/MC9RS08KB4
 - 24-pin QFN, 20-pin SOIC, 16-pin SOIC NB or TSSOP
 - MC9RS08KB2
 - 8-pin SOIC or DFN

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	4/13/2009	Updated on shared review comments, added package information.
2	5/22/2009	Completed most of the TBDs, corrected the block diagram.
3	8/31/2009	Completed all the TBDs. Changed V_{LVD} and added R_{PD} in the Table 7 . Changed SI_{DD} , ADC adder from stop, RTI adder from stop with 1 kHz clock source enabled and LVI adder from stop at 5 V in the Table 8 .
4	6/23/2011	Split the 10-Bit ADC Characteristics to Table 15 and Table 16 for the V_{DDAD} ranges. Corrected the note 4 in the Table 8 .
5	1/30/2012	Added 24-pin QFN package.

Related Documentation

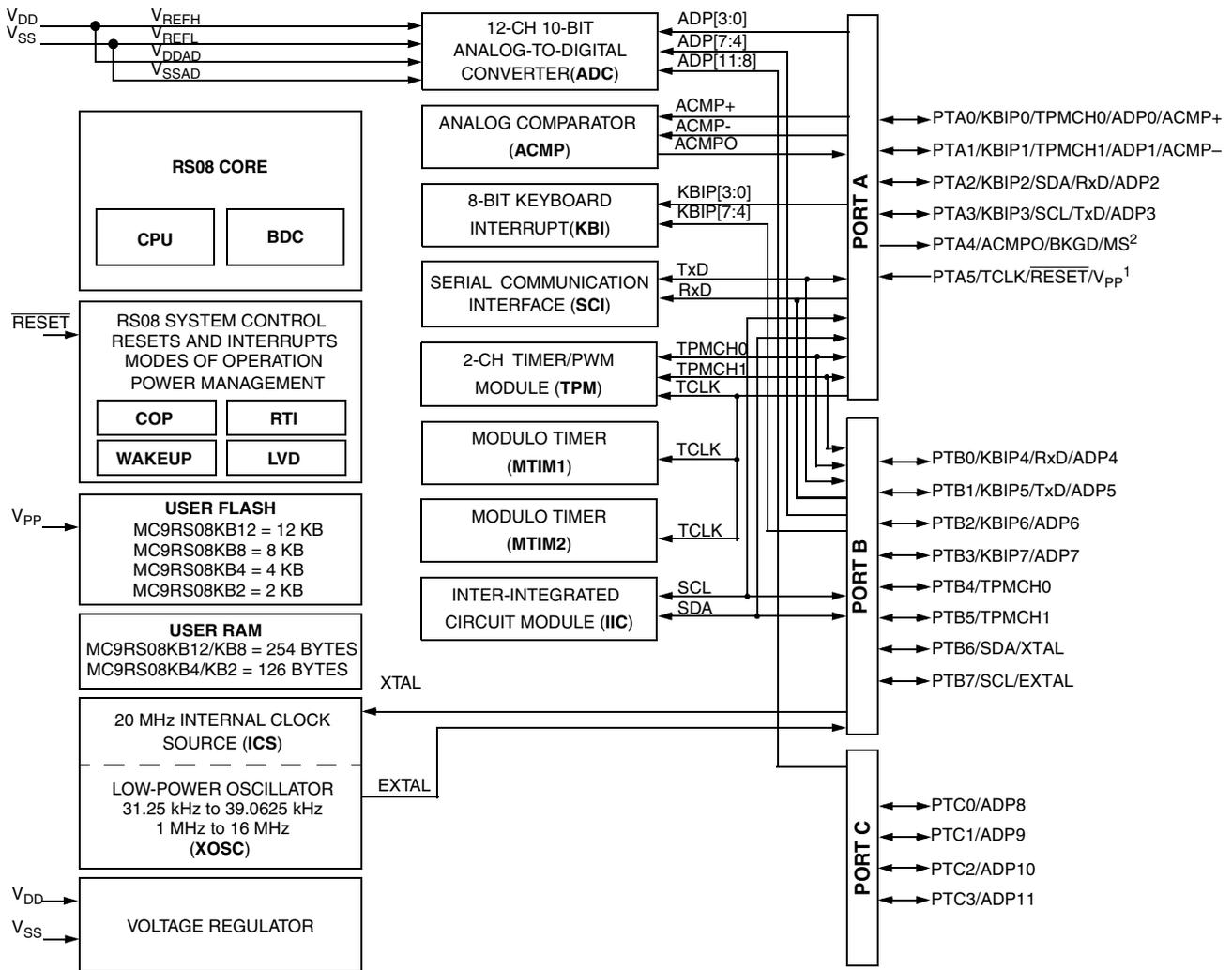
Find the most current versions of all documents at: <http://www.freescale.com>

Reference Manual (MC9RS08KB12RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, [Figure 1](#), shows the structure of the MC9RS08KB12 MCU.



NOTES:

1. PTA5/TCLK/RESET/V_{PP} is an input-only pin when used as port pin
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin

Figure 1. MC9RS08KB12 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08KB12 series.

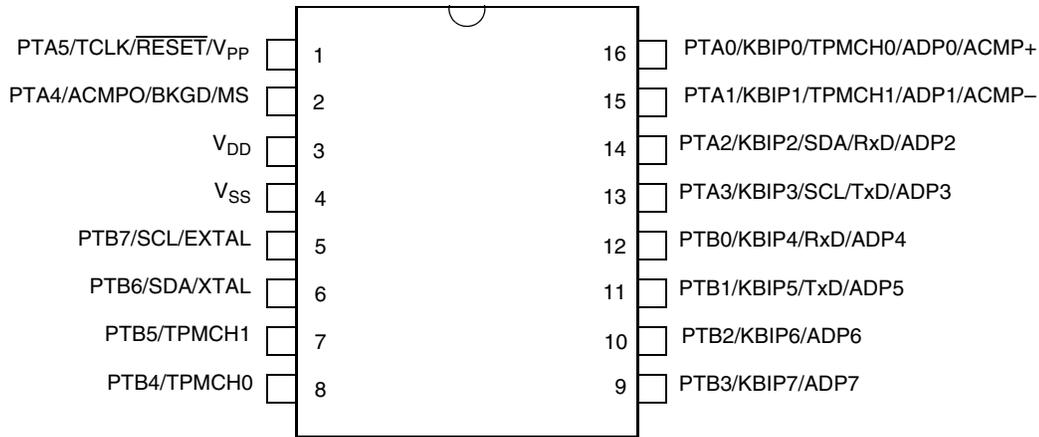


Figure 4. MC9RS08KB12 Series 16-Pin SOIC NB/TSSOP Package

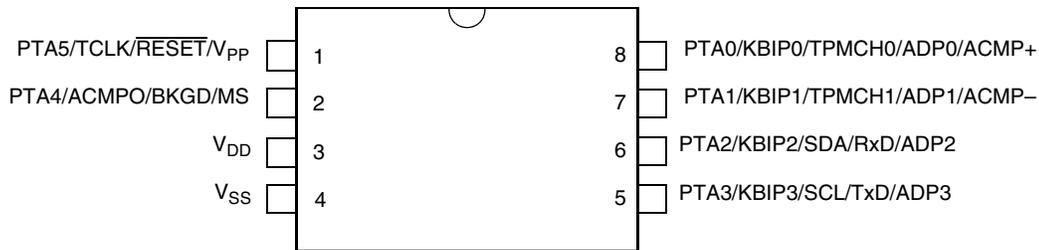


Figure 5. MC9RS08KB12 Series 8-Pin SOIC/DFN Package

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9RS08KB12 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.

Electrical Characteristics

unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to 85	°C
Maximum junction temperature	T_{JMAX}	150	°C
Thermal resistance 24-pin QFN	θ_{JA}	113	°C/W
Thermal resistance 20-pin SOIC	θ_{JA}	83	°C/W
Thermal resistance 16-pin SOIC NB	θ_{JA}	103	°C/W
Thermal resistance 16-pin TSSOP	θ_{JA}	29	°C/W
Thermal resistance 8-pin SOIC	θ_{JA}	150	°C/W
Thermal resistance 8-pin DFN	θ_{JA}	110	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C /W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts chip internal power

$P_{I/O}$ = Power dissipation on input and output pins user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving [Equation 1](#) and [Equation 2](#) for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from [Equation 3](#) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving [Equation 1](#) and [Equation 2](#) iteratively for any value of T_A .

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge.

Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating ¹	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Charge device model (CDM)	V_{CDM}	± 500	—	V
3	Latch-up current at $T_A = 85^\circ\text{C}$	I_{LAT}	± 100	—	mA

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = -40 to 85°C Ambient)

No.	C	Parameter	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage (run, wait and stop modes.) $0 < f_{BUS} < 10$ MHz	V_{DD}	1.8	—	5.5	V
2	C	Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	0.8^1	—	—	V
3	P	Low-voltage detection threshold (V_{DD} falling) (V_{DD} rising)	V_{LVD}	1.80 1.88	1.86 1.94	1.95 2.05	V
4	C	Power on RESET (POR) voltage	V_{POR}^1	0.9	—	1.7	V
5	C	Input high voltage ($V_{DD} > 2.3\text{V}$) (all digital inputs)	V_{IH}	$0.70 \times V_{DD}$	—	—	V
6	C	Input high voltage ($1.8\text{V} \leq V_{DD} \leq 2.3\text{V}$) (all digital inputs)	V_{IH}	$0.85 \times V_{DD}$	—	—	V
7	C	Input low voltage ($V_{DD} > 2.3\text{V}$) (all digital inputs)	V_{IL}	—	—	$0.30 \times V_{DD}$	V
8	C	Input low voltage ($1.8\text{V} \leq V_{DD} \leq 2.3\text{V}$) (all digital inputs)	V_{IL}	—	—	$0.30 \times V_{DD}$	V
9	C	Input hysteresis (all digital inputs)	V_{hys}^1	$0.06 \times V_{DD}$	—	—	V
10	P	Input leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS} , all input only pins	I_{InI}	—	0.025	1.0	μA
11	P	High impedance (off-state) leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS} , all input/output	I_{IOZ}	—	0.025	1.0	μA
12	P	Internal pullup resistors ² (all port pins)	R_{PU}	20	45	65	k Ω
13	P	Internal pulldown resistors ² (all port pins)	R_{PD}	20	45	65	k Ω
14	C	Output high voltage — Low drive (PTxDSn = 0) 5 V, $I_{Load} = 2$ mA 3 V, $I_{Load} = 1$ mA 1.8 V, $I_{Load} = 0.5$ mA	V_{OH}	$V_{DD} - 0.8$	—	—	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, $I_{Load} = 5$ mA 3 V, $I_{Load} = 3$ mA 1.8 V, $I_{Load} = 2$ mA			$V_{DD} - 0.8$	—	
15	C	Maximum total IOH for all port pins	I_{OHT}	—	—	40	mA

Table 7. DC Characteristics (Temperature Range = -40 to 85°C Ambient) (continued)

No.	C	Parameter	Symbol	Min	Typical	Max	Unit
16	C	Output low voltage — Low drive (PTxDSn = 0) 5 V, $I_{Load} = 2$ mA 3 V, $I_{Load} = 1$ mA 1.8 V, $I_{Load} = 0.5$ mA	V_{OL}	—	—	0.8	V
		Output low voltage — High drive (PTxDSn = 1) 5 V, $I_{Load} = 5$ mA 3 V, $I_{Load} = 3$ mA 1.8 V, $I_{Load} = 2$ mA		—	—		
17	C	Maximum total IOI for all port pins	I_{OLT}	—	—	40	mA
18	C	DC injection current ^{3, 4, 5, 6} $V_{In} < V_{SS}$, $V_{In} > V_{DD}$ Single pin limit		—	—	0.2	mA
		Total MCU limit, includes sum of all stressed pins		—	—	0.8	
19	C	Input capacitance (all non-supply pins)	C_{In}	—	—	7	pF

¹ This parameter is characterized and not tested on each device.

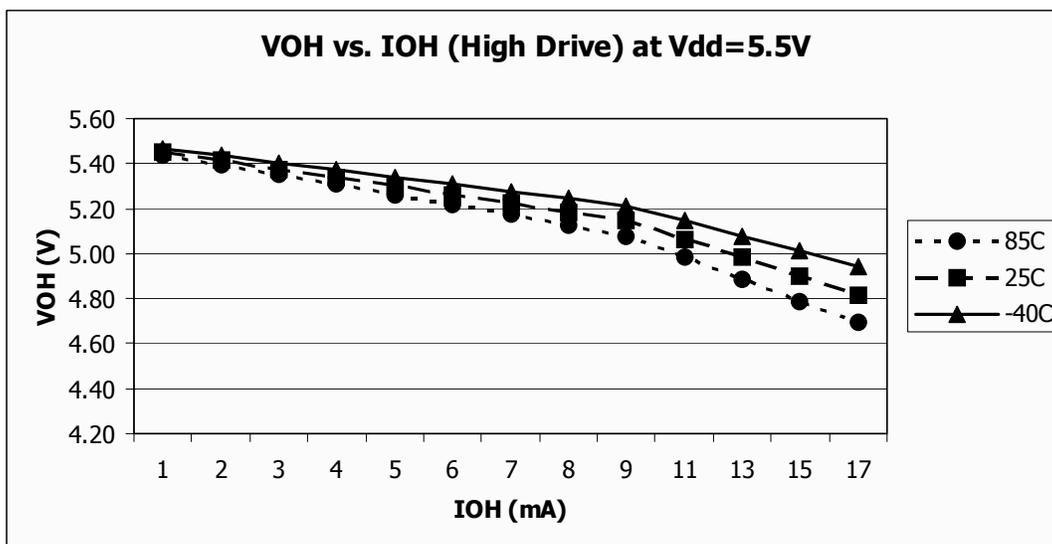
² Measurement condition for pull resistors: $V_{In} = V_{SS}$ for pullup and $V_{In} = V_{DD}$ for pulldown.

³ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the \overline{RESET}/V_{PP} which is internally clamped to V_{SS} only.

⁴ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁵ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁶ This parameter is characterized and not tested on each device.



**Figure 6. Typical V_{OH} vs. I_{OH}
 $V_{DD} = 5.5$ V (High Drive)**

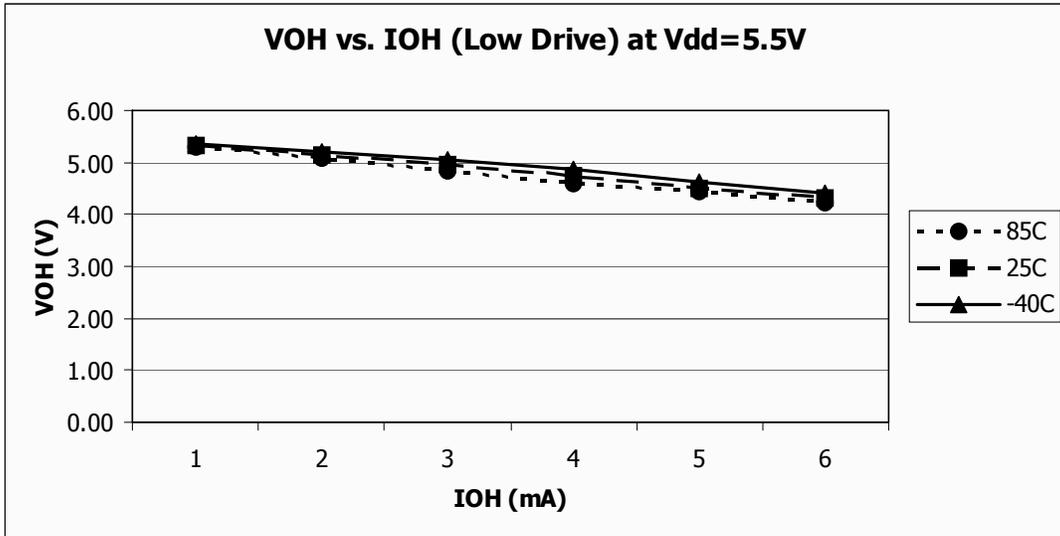


Figure 7. Typical V_{OH} vs. I_{OH}
 $V_{DD} = 5.5V$ (Low Drive)

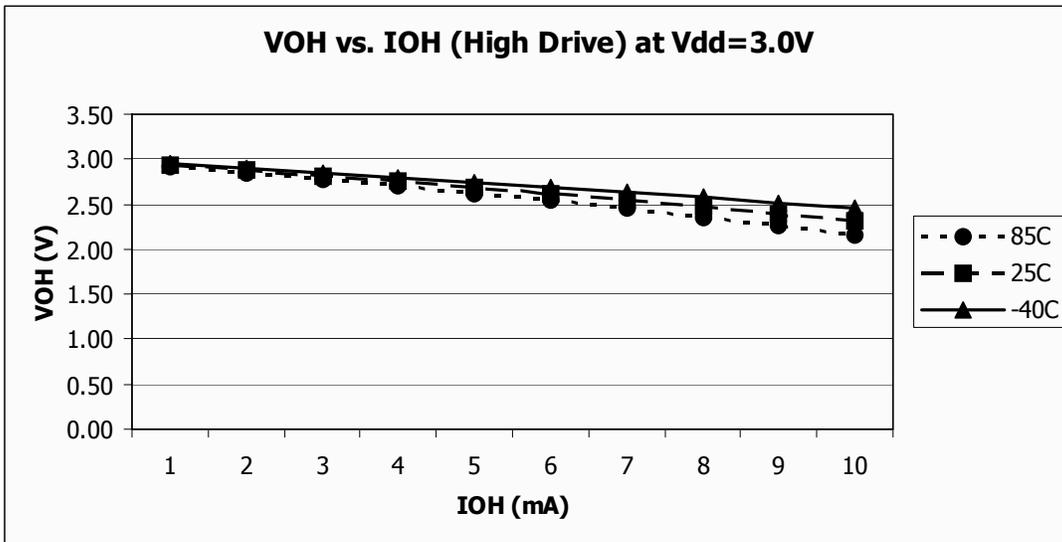


Figure 8. Typical V_{OH} vs. I_{OH}
 $V_{DD} = 3.0V$ (High Drive)

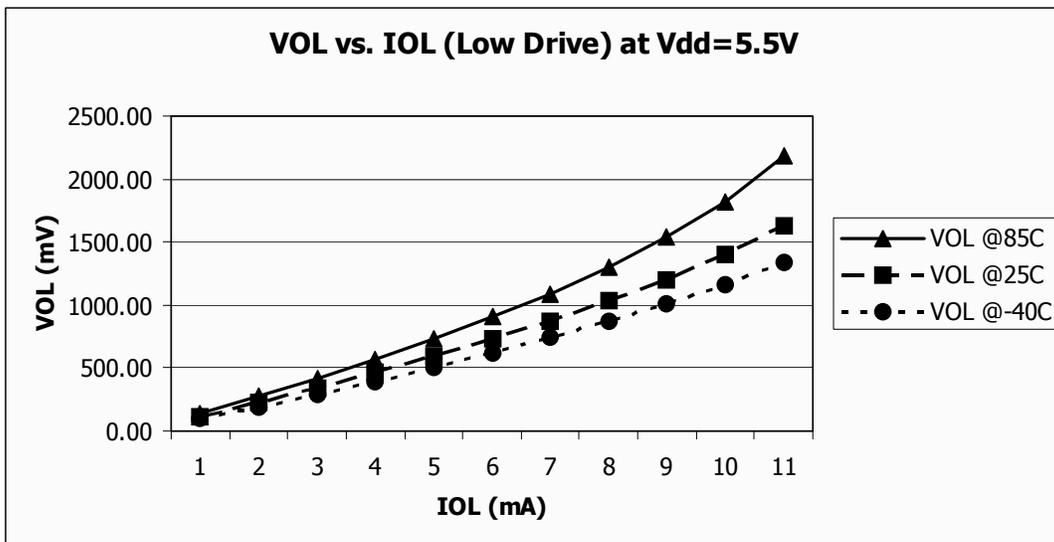


Figure 13. Typical V_{OL} vs. I_{OL}
 $V_{DD} = 5.5\text{ V}$ (Low Drive)

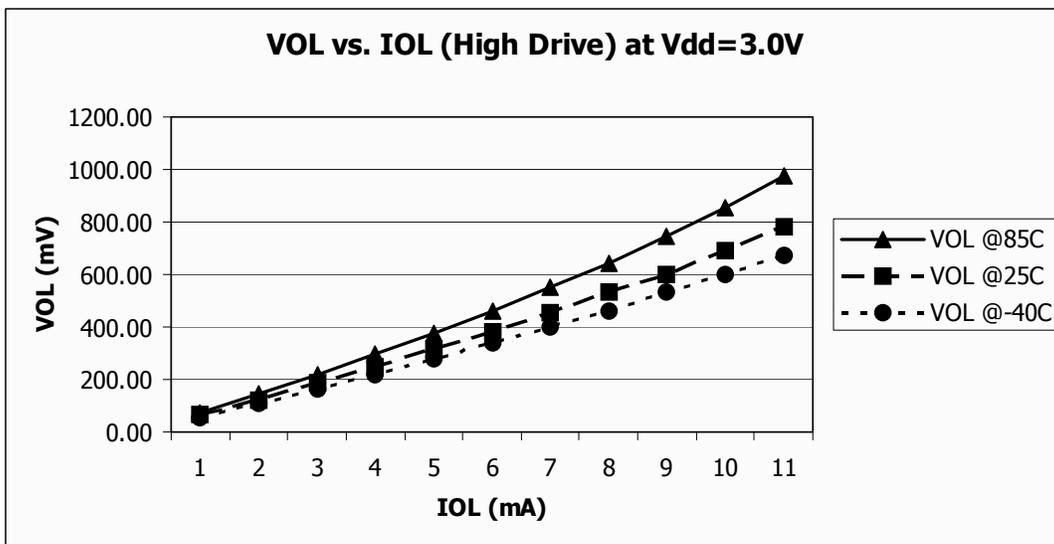


Figure 14. Typical V_{OL} vs. I_{OL}
 $V_{DD} = 3.0\text{ V}$ (High Drive)

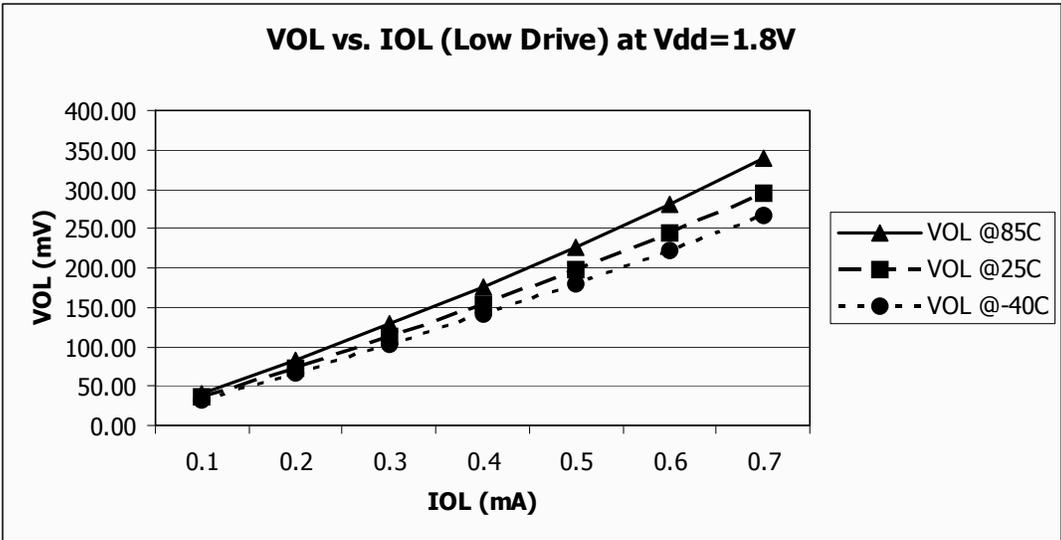


Figure 17. Typical V_{OL} vs. I_{OL}
 $V_{DD} = 1.8\text{ V}$ (Low Drive)

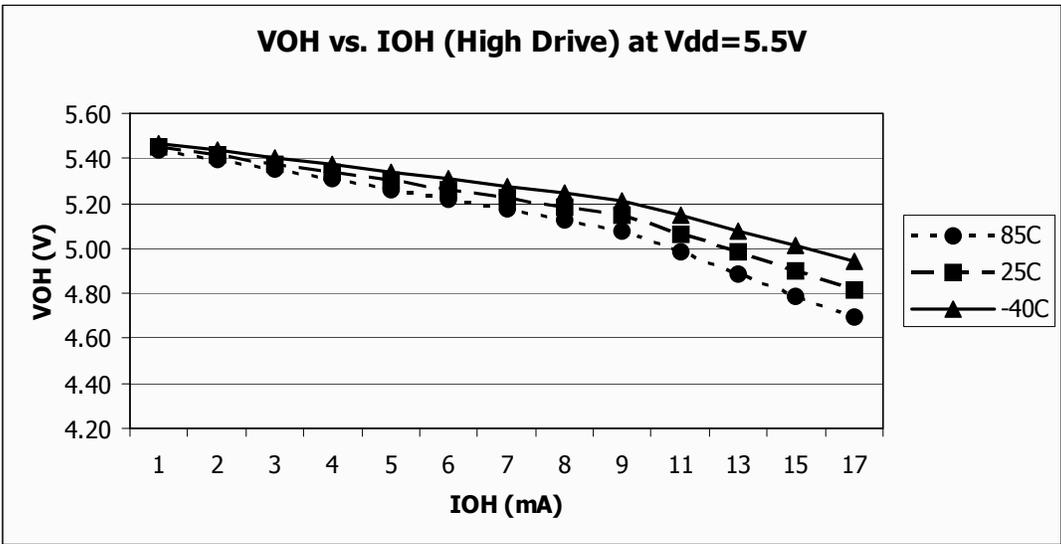


Figure 18. Typical I_{OH} vs. $V_{DD}-V_{OH}$
 $V_{DD} = 5.5\text{ V}$ (High Drive)

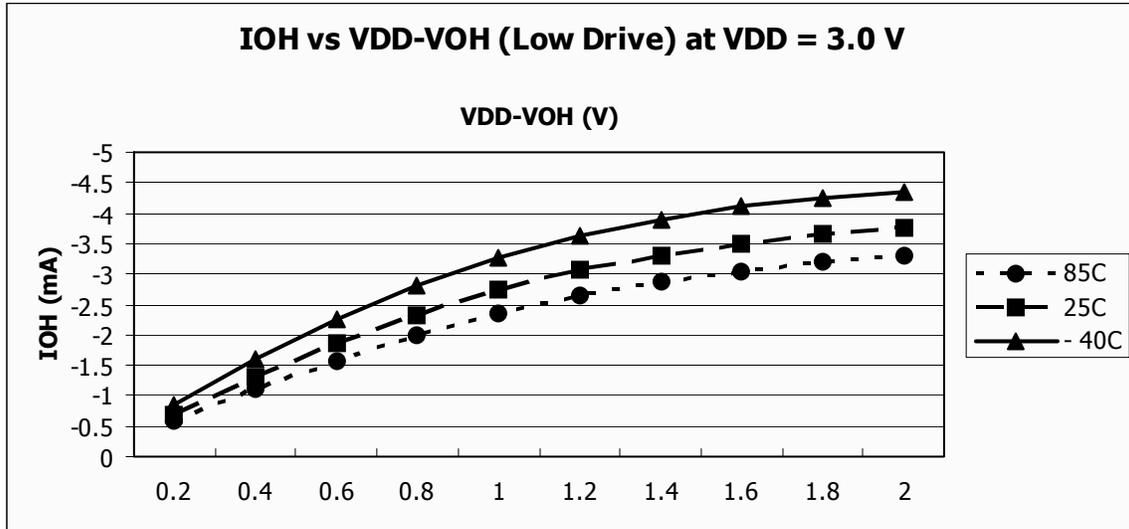


Figure 21. Typical I_{OH} vs. V_{DD}-V_{OH}
V_{DD} = 3 V (Low Drive)

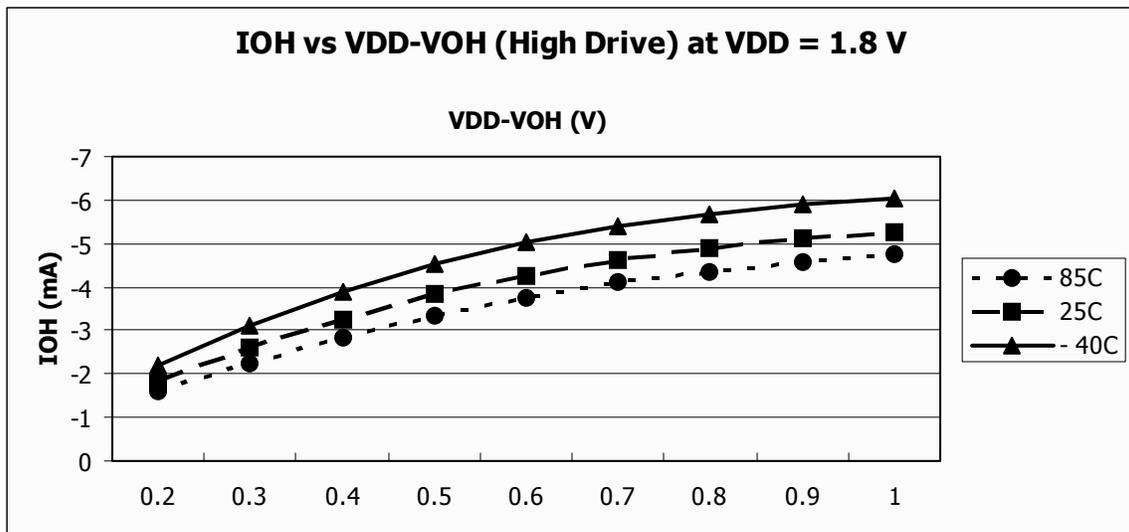


Figure 22. Typical I_{OH} vs. V_{DD}-V_{OH}
V_{DD} = 1.8 V (High Drive)

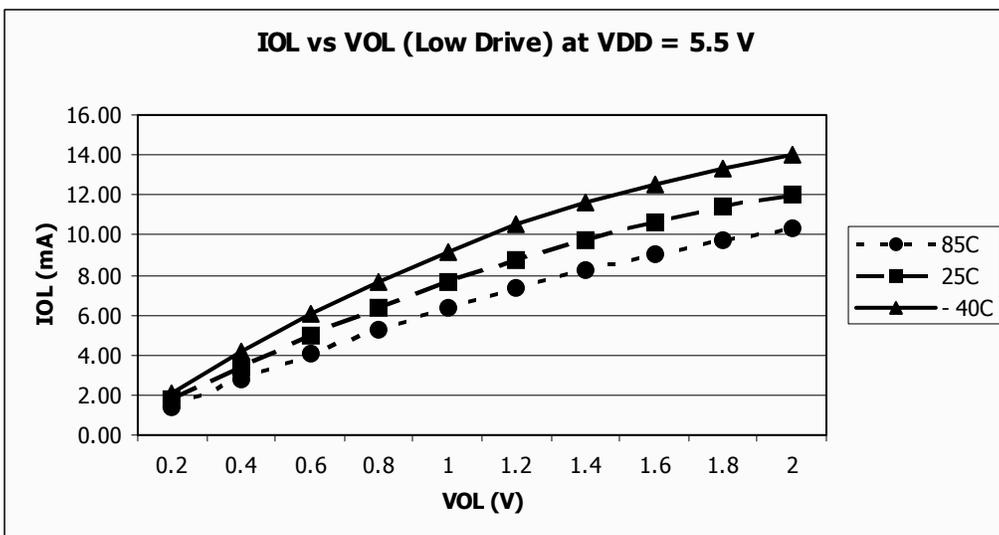


Figure 25. Typical I_{OL} vs. V_{OL}
 $V_{DD} = 5.5$ V (Low Drive)

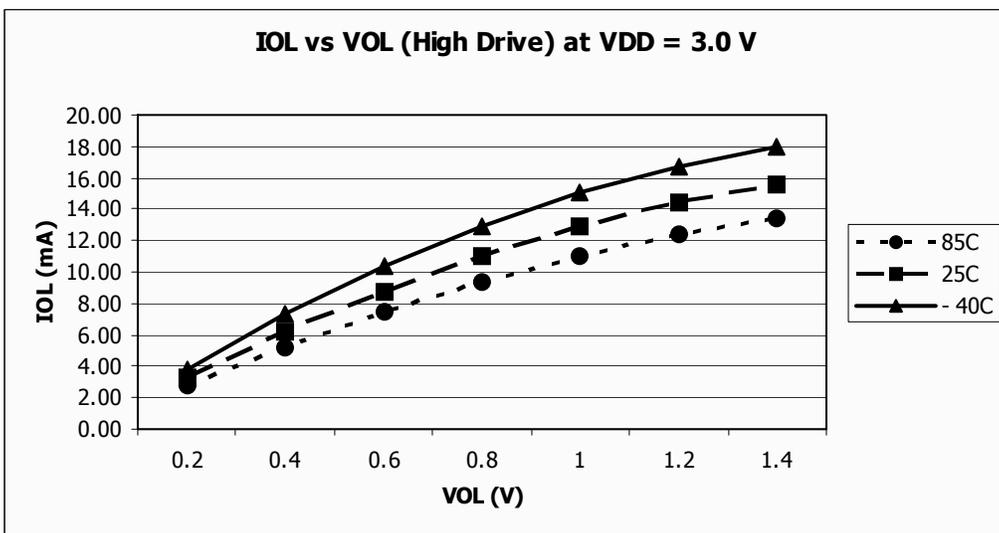


Figure 26. Typical I_{OL} vs. V_{OL}
 $V_{DD} = 3$ V (High Drive)

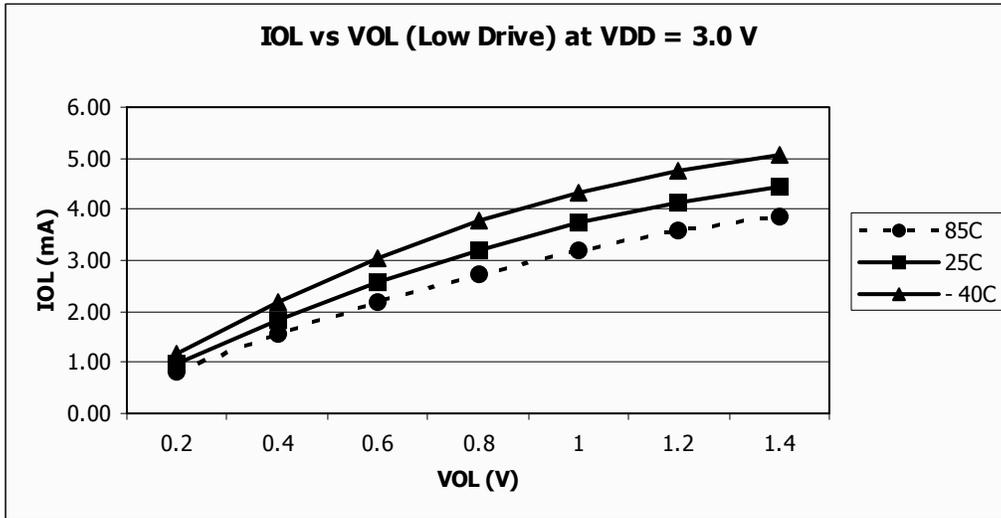


Figure 27. Typical I_{OL} vs. V_{OL}
 $V_{DD} = 3$ V (Low Drive)

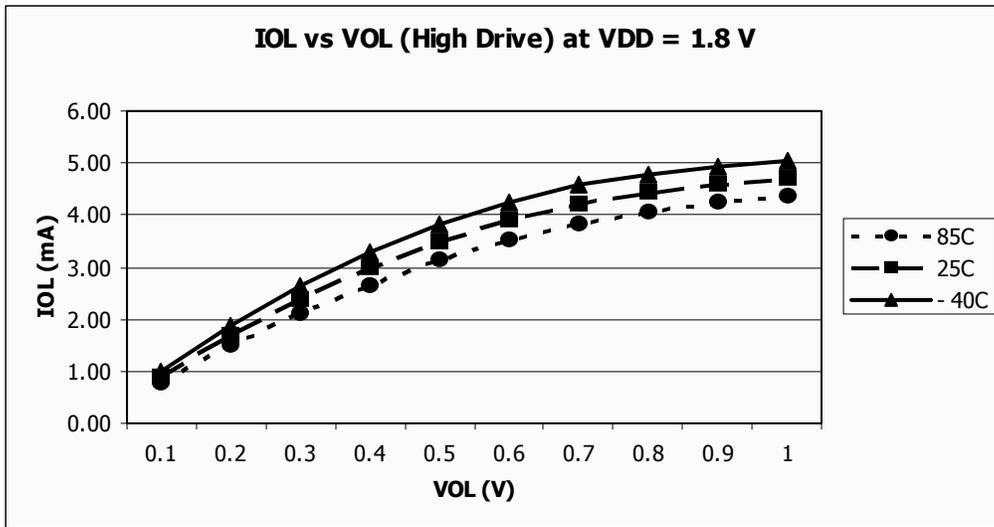


Figure 28. Typical I_{OL} vs. V_{OL}
 $V_{DD} = 1.8$ V (High Drive)

3.9.1 Control Timing

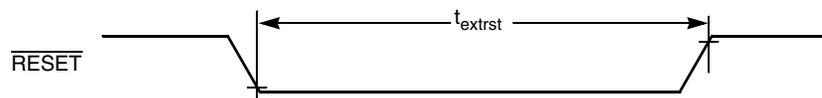
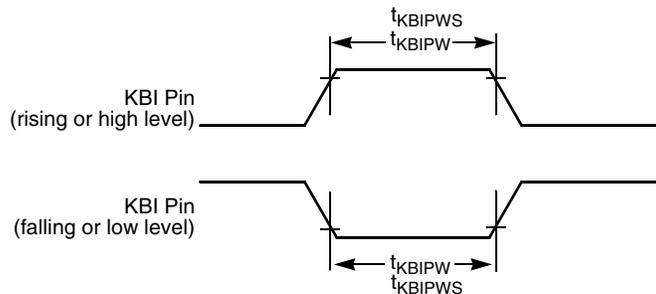
Table 10. Control Timing

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	0	—	10	MHz
2	D	Real time interrupt internal oscillator period	t_{RTI}	700	1000	1300	μ s
3	D	External \overline{RESET} pulse width ¹	t_{extrst}	150	—	—	ns
4	D	KBI pulse width ²	t_{KBIPW}	$1.5 t_{cyc}$	—	—	ns
5	D	KBI pulse width in stop ¹	t_{KBIPWS}	100	—	—	ns
6	D	Port rise and fall time (load = 50 pF) ³	t_{Rise}, t_{Fall}	—	11	—	ns
		Slew rate control disabled (PTxSE = 0)			35	—	
		Slew rate control enabled (PTxSE = 1)					

¹ This is the shortest pulse guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

² This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

³ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$.


Figure 30. Reset Timing

Figure 31. KBI Pulse Width

3.9.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

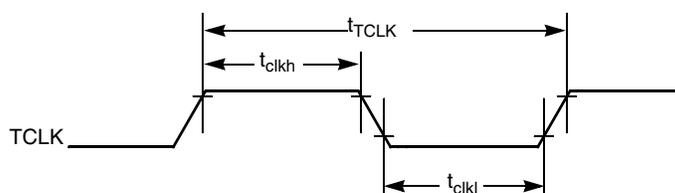


Figure 32. Timer External Clock

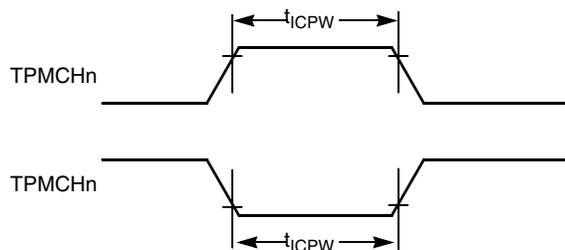


Figure 33. Timer Input Capture Pulse

3.10 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.80	—	5.5	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	μA
3	D	Analog input voltage ¹	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
4	C	Analog input offset voltage ¹	V_{AIO}	—	20	40	mV
5	C	Analog Comparator hysteresis ¹	V_H	3.0	9.0	15.0	mV
6	C	Analog source impedance ¹	R_{AS}	—	—	10	$k\Omega$
7	P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
8	C	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	μs

Table 14. 10-Bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
ADC conversion clock Freq.	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC=1)		0.4	—	4.0		

¹ Typical values assume $V_{DDAD} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

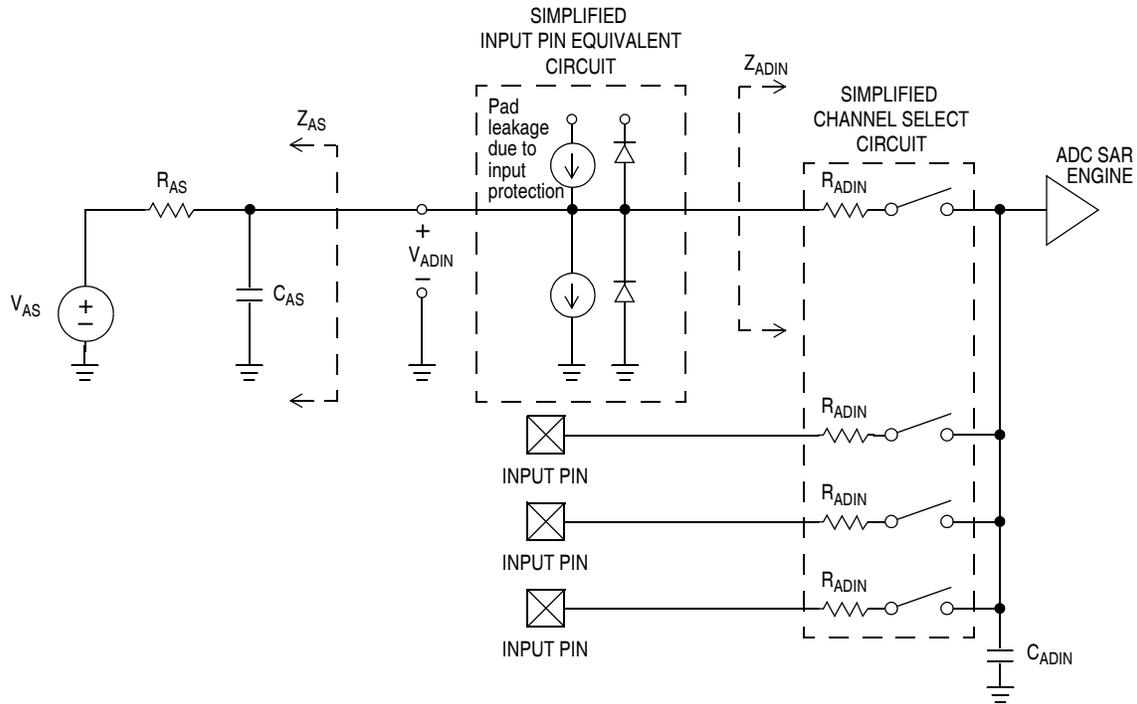


Figure 34. ADC Input Impedance Equivalency Diagram

Table 15. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 2.7 V < V_{DDAD} < 5.5 V)

C	Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	133	—	μ A	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	218	—	μ A	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	327	—	μ A	

Table 15. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, $2.7\text{ V} < V_{DDAD} < 5.5\text{ V}$)

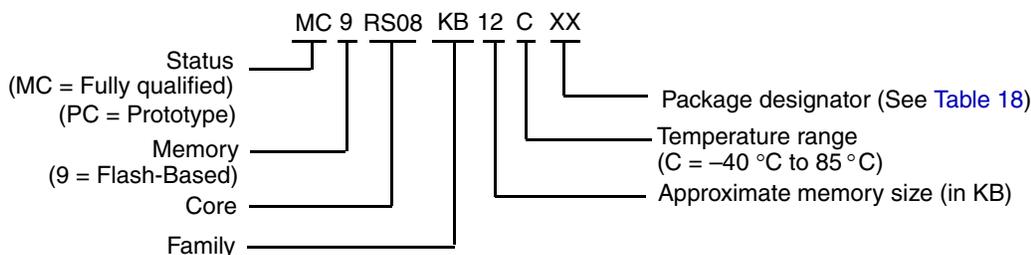
C	Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
C	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	0.582	1	mA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	E_{TUE}	—	± 1.5	± 3.5	LSB ²	Includes quantization
		8-bit mode		—	± 0.7	± 1.5		
T	Differential Non-Linearity	10-bit mode	DNL	—	± 0.5	± 1.0	LSB ²	
		8-bit mode		—	± 0.3	± 0.5		
Monotonicity and No-Missing-Codes guaranteed								
C	Integral Non-Linearity	10-bit mode	INL	—	± 0.5	± 1.0	LSB ²	
		8-bit mode		—	± 0.3	± 0.5		
P	Zero-Scale Error	10-bit mode	E_{ZS}	—	± 1.5	± 2.5	LSB ²	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	± 0.5	± 0.7		
P	Full-Scale Error	10-bit mode	E_{FS}	—	± 1	± 1.5	LSB ²	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	± 0.5	± 0.5		
D	Quantization Error	10-bit mode	E_Q	—	—	± 0.5	LSB ²	
		8-bit mode		—	—	± 0.5		
D	Input Leakage Error	10-bit mode	E_{IL}	—	± 0.2	± 2.5	LSB ²	Pad leakage ^{2*} R_{AS}
		8-bit mode		—	± 0.1	± 1		

¹ Typical values assume $V_{DDAD} = 5.0\text{ V}$, $\text{Temp} = 25\text{ }^\circ\text{C}$, $f_{ADCK} = 1.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

² Based on input pad leakage current. Refer to pad electricals.

4 Ordering Information

This section contains ordering numbers for MC9RS08KB12 series devices. See below for an example of the device numbering system.



5 Package Information and Mechanical Drawings

Table 18 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9RS08KB12 Series Product Summary pages at <http://www.freescale.com>.

To view the latest drawing, either:

- Click on the appropriate link in Table 18, or
- Open a browser to the Freescale® website (<http://www.freescale.com>), and enter the appropriate document number (from Table 18) in the “Enter Keyword” search box at the top of the page.

Table 18. Device Numbering System

Device Number	Memory		Package		
	Flash	RAM	Type	Designator	Document No.
MC9RS08KB12 MC9RS08KB8 MC9RS08KB4	12 KB	254 bytes	24 QFN	FK	98ASA00087D
	8 KB	254 bytes	20 SOIC WB	WJ	98ASB42343B
	4 KB	126 bytes	16 SOIC NB	SG	98ASB42566B
			16 TSSOP	TG	98ASH70247A
MC9RS08KB2	2 KB	126 bytes	8 SOIC NB	SC	98ASB42564B
			8 DFN	DC	98ARL10557D

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