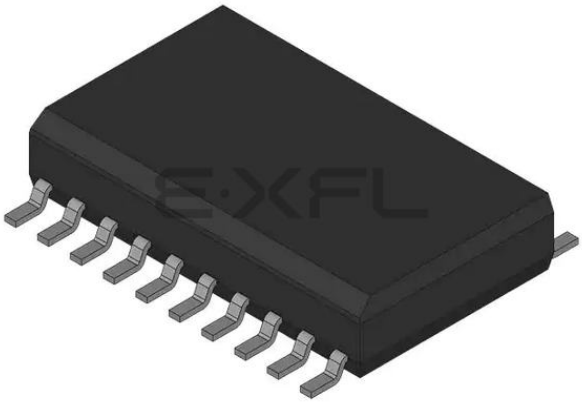

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	254 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9rs08kb12cwj

Freescale Semiconductor
Data Sheet: Technical Data

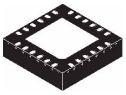
Document Number: MC9RS08KB12
Rev. 5, 1/2012

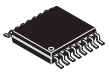
MC9RS08KB12

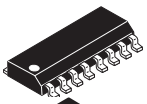
MC9RS08KB12 Series

Covers:MC9RS08KB12
MC9RS08KB8
MC9RS08KB4
MC9RS08KB2

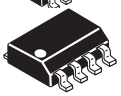

20-Pin SOIC
Case 751D


24-Pin QFN
Case 1982-01


16-Pin TSSOP
Case 948F


16-Pin SOIC N/B
Case 751B


8-Pin DFN
Case 1452-02


8-Pin SOIC
Case 751

- 8-Bit RS08 Central Processor Unit (CPU)
  - Up to 20 MHz CPU at 1.8 V to 5.5 V across temperature range of –40 °C to 85 °C
  - Subset of HC08 instruction set with added BGND instruction
  - Single Global interrupt vector
- On-Chip Memory
  - Up to 12 KB flash read/program/erase over full operating voltage and temperature, 12 KB/8 KB/4 KB/2 KB flash are optional
  - Up to 254-byte random-access memory (RAM), 254-byte/126-byte RAM are optional
  - Security circuitry to prevent unauthorized access to flash contents
- Power-Saving Modes
  - Wait mode — CPU shuts down; system clocks continue to run; full voltage regulation
  - Stop mode — CPU shuts down; system clocks are stopped; voltage regulator in standby
  - Wakeup from power-saving modes using RTI, KBI, ADC, ACMP, SCI and LVD
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies up to 10 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal low power oscillator
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash-block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
  - **ADC** — 12-channel, 10-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop; hardware trigger
  - **ACMP** — Analog comparator; full rail-to-rail supply operation; option to compare to fixed internal bandgap reference voltage; can operate in stop mode
  - **TPM** — One 2-channel timer/pulse-width modulator module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - **IIC** — Inter-integrated circuit bus module capable of operation up to 100 kbps with maximum bus loading; capable of higher baud rates with reduced loading
  - **SCI** — One serial communications interface module with optional 13-bit break; LIN extensions
  - **MTIM** — Two 8-bit modulo timers; optional clock sources
  - **RTI** — One real-time clock with optional clock sources
  - **KBI** — Keyboard interrupts; up to 8 ports
- Input/Output
  - 18 GPIOs in 24- and 20-pin packages; 14 GPIOs in 16-pin package; 6 GPIOs in 8-pin package; including one output-only pin and one input-only pin
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package Options
  - MC9RS08KB12/MC9RS08KB8/MC9RS08KB4
    - 24-pin QFN, 20-pin SOIC, 16-pin SOIC NB or TSSOP
  - MC9RS08KB2
    - 8-pin SOIC or DFN

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	4/13/2009	Updated on shared review comments, added package information.
2	5/22/2009	Completed most of the TBDs, corrected the block diagram.
3	8/31/2009	Completed all the TBDs. Changed V_{LVD} and added R_{PD} in the Table 7. Changed SI_{DD}, ADC adder from stop, RTI adder from stop with 1 kHz clock source enabled and LVI adder from stop at 5 V in the Table 8.
4	6/23/2011	Split the 10-Bit ADC Characteristics to Table 15 and Table 16 for the V_{DDAD} ranges. Corrected the note 4 in the Table 8.
5	1/30/2012	Added 24-pin QFN package.

Related Documentation

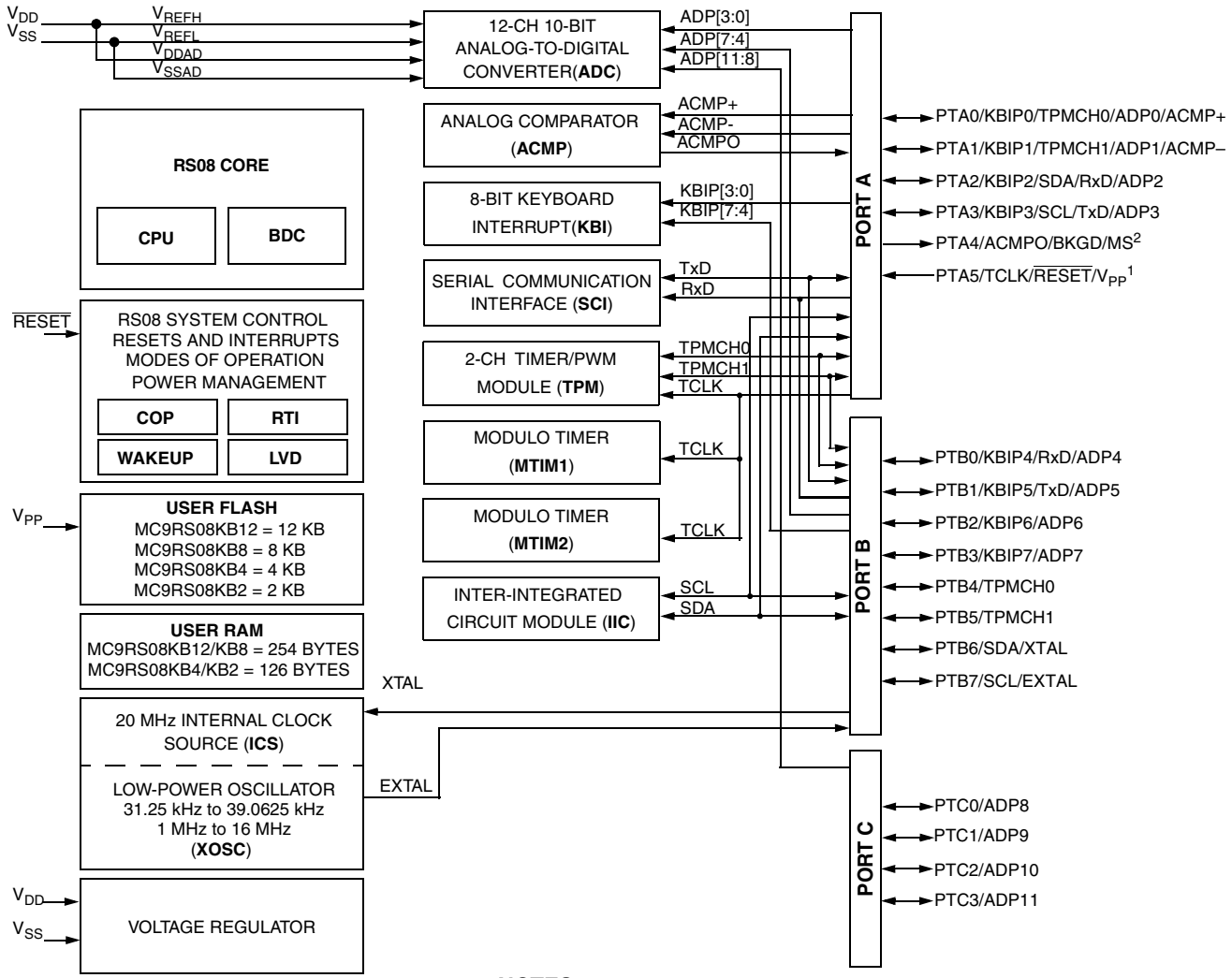
Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9RS08KB12RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9RS08KB12 MCU.



NOTES:

1. PTA5/TCLK/$\overline{\text{RESET}}$/V_{PP} is an input-only pin when used as port pin
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin

Figure 1. MC9RS08KB12 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08KB12 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number				<-- Lowest **Priority** --> Highest				
24	**20**	**16**	**8**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	3	3	3					V_{DD}
2	—	—	—	NC				
3	4	4	4					V_{SS}
4	5	5	—	PTB7	SCL[1]			EXTAL
5	6	6	—	PTB6	SDA[1]			XTAL
6	7	7	—	PTB5	TPMCH1[2]			
7	8	8	—	PTB4	TPMCH0[2]			
8	9	—	—	PTC3			ADP11	
9	10	—	—	PTC2			ADP10	
10	11	—	—	PTC1			ADP9	
11	12	—	—	PTC0			ADP8	
12	13	9	—	PTB3	KBIP7		ADP7	
13	14	10	—	PTB2	KBIP6		ADP6	
14	15	11	—	PTB1	KBIP5	TxD[3]	ADP5	
15	16	12	—	PTB0	KBIP4	RxD[3]	ADP4	
16	17	13	5	PTA3	KBIP3	SCL[1]	TxD[3]	ADP3
17	18	14	6	PTA2	KBIP2	SDA[1]	RxD[3]	ADP2
18	19	15	7	PTA1	KBIP1	TPMCH1[2]	ADP1	ACMP–
19	20	16	8	PTA0	KBIP0	TPMCH0[2]	ADP0	ACMP+
20	—	—	—	NC				
21	—	—	—	NC				
22	—	—	—	NC				
23	1	1	1	PTA5		TCLK	$\overline{\text{RESET}}$	V_{PP}
24	2	2	2	PTA4	ACMPO	BKGD	MS	

1 IIC pins can be remapped to PTB6 and PTB7, default reset location is PTA2 and PTA3. It can be configured only once.

2 TPM pins can be remapped to PTB4 and PTB5, default reset location is PTA0 and PTA1.

3 SCI pins can be remapped to PTA2 and PTA3, default reset location is PTB0 and PTB1. It can be configured only once.

Table 2. Parameter Classifications

D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{\text{RESET}}/V_{PP}$ pin which is internally clamped to V_{SS} only.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of

During the device qualification ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-Up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	1	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient)

No.	C	Parameter	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage (run, wait and stop modes.) 0 < f_{Bus} <10 MHz	V_{DD}	1.8	—	5.5	V
2	C	Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	0.8[1]	—	—	V
3	P	Low-voltage detection threshold (V_{DD} falling) (V_{DD} rising)	V_{LVD}	1.80 1.88	1.86 1.94	1.95 2.05	V
4	C	Power on RESET (POR) voltage	V_{POR}[1]	0.9	—	1.7	V
5	C	Input high voltage (V_{DD} > 2.3V) (all digital inputs)	V_{IH}	0.70 × V_{DD}	—	—	V
6	C	Input high voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IH}	0.85 × V_{DD}	—	—	V
7	C	Input low voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IL}	—	—	0.30 × V_{DD}	V
8	C	Input low voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IL}	—	—	0.30 × V_{DD}	V
9	C	Input hysteresis (all digital inputs)	V_{hys}[1]	0.06 × V_{DD}	—	—	V
10	P	Input leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input only pins	|I_{In}|	—	0.025	1.0	µA
11	P	High impedance (off-state) leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input/output	|I_{OZ}|	—	0.025	1.0	µA
12	P	Internal pullup resistors[2](all port pins)	R_{PU}	20	45	65	kΩ
13	P	Internal pulldown resistors[2](all port pins)	R_{PD}	20	45	65	kΩ
14	C	Output high voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA 1.8 V, I_{Load} = 0.5 mA	V_{OH}	V_{DD} – 0.8	— — —	— — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 3 mA 1.8 V, I_{Load} = 2 mA		V_{DD} – 0.8	— — —	— — —	
15	C	Maximum total I_{OH} for all port pins	|I_{OHT}|	—	—	40	mA

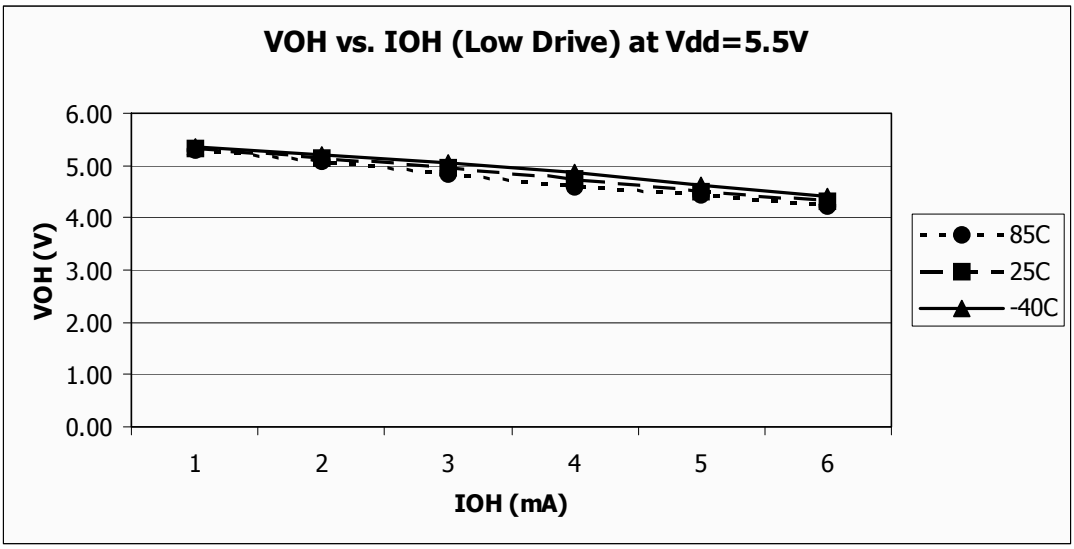


Figure 7. Typical V_{OH} vs. I_{OH}
V_{DD} = 5.5 V (Low Drive)

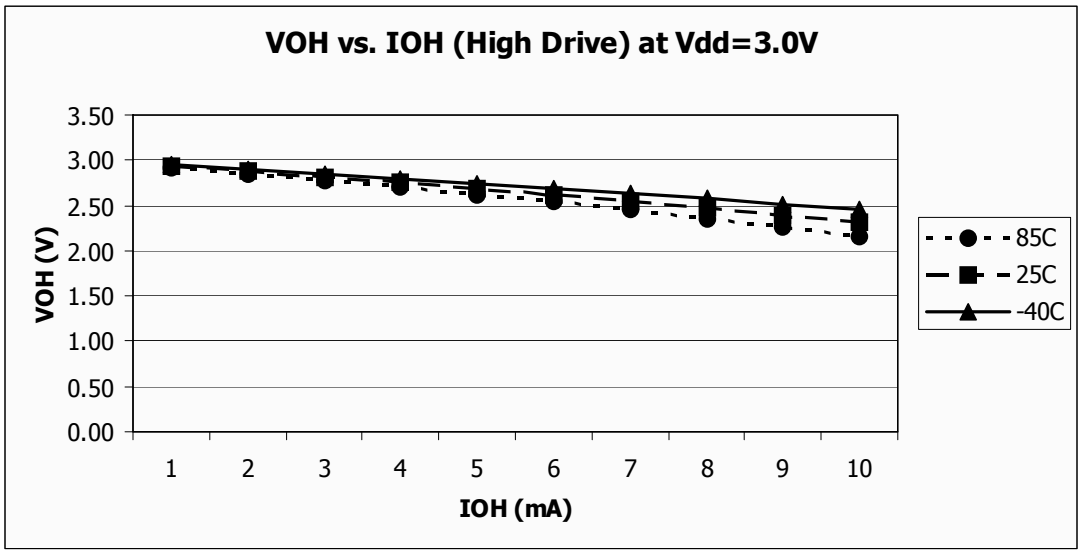


Figure 8. Typical V_{OH} vs. I_{OH}
V_{DD} = 3.0 V (High Drive)

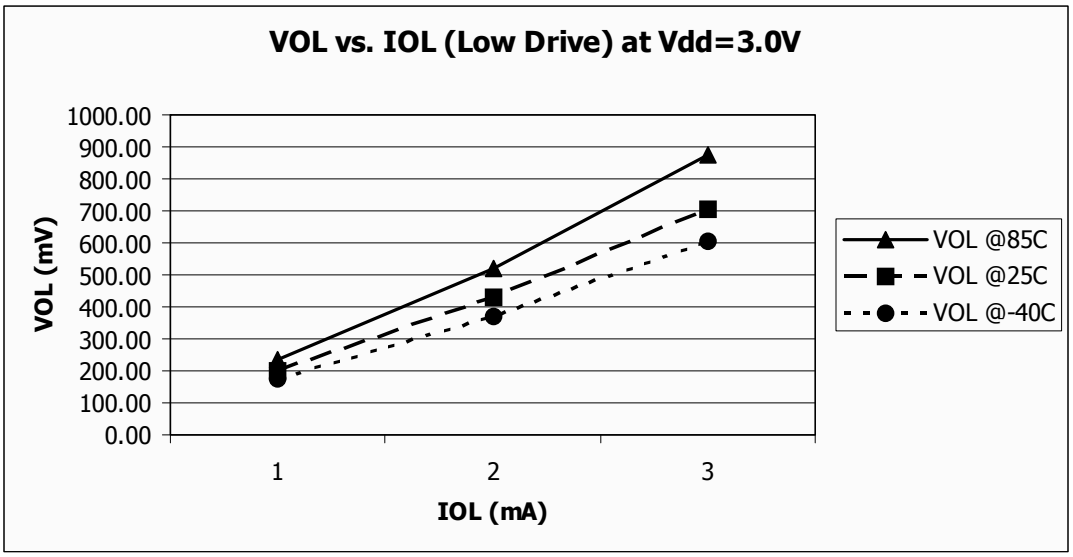


Figure 15. Typical V_{OL} vs. I_{OL}
V_{DD} = 3.0 V (Low Drive)

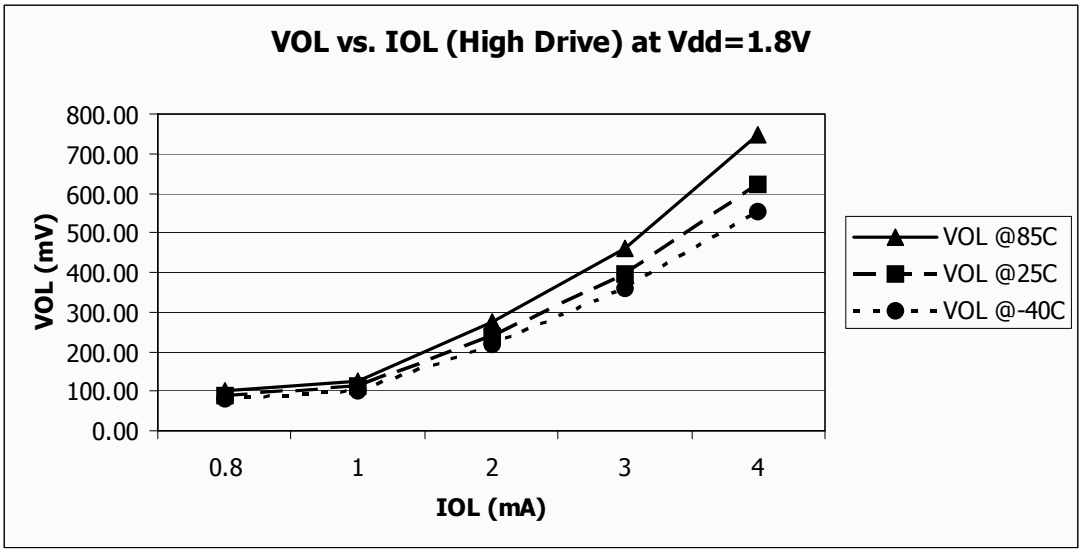


Figure 16. Typical V_{OL} vs. I_{OL}
V_{DD} = 1.8 V (High Drive)

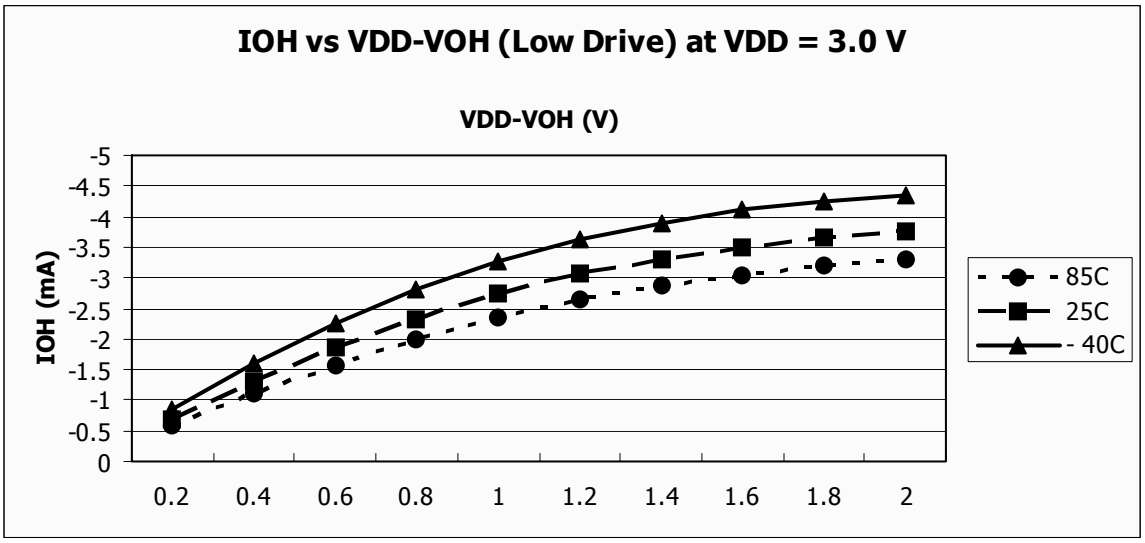


Figure 21. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 3 V (Low Drive)

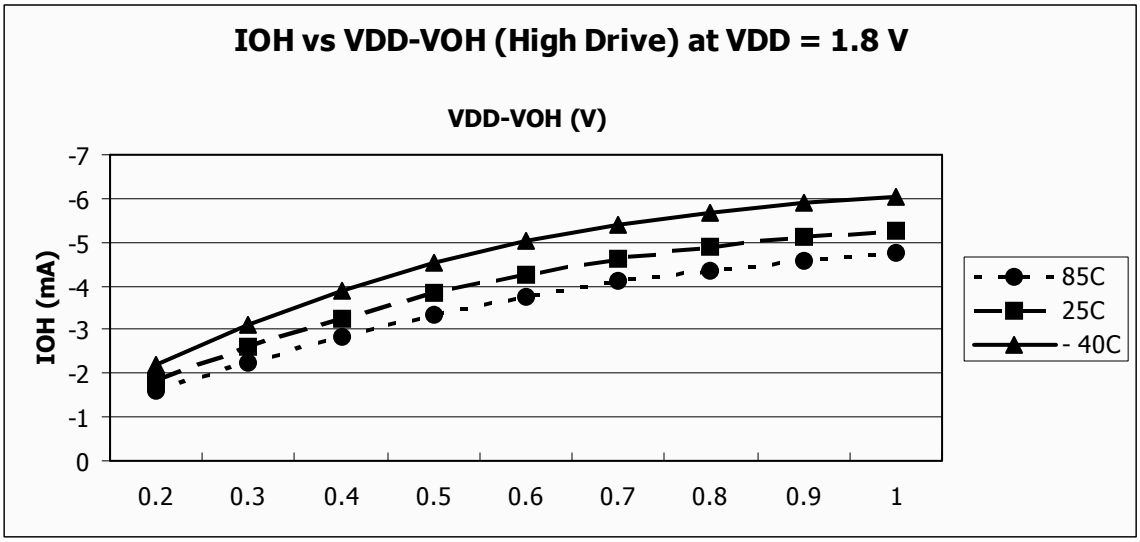


Figure 22. Typical I_{OH} vs. V_{DD}–V_{OH} V_{DD} = 1.8 V (High Drive)

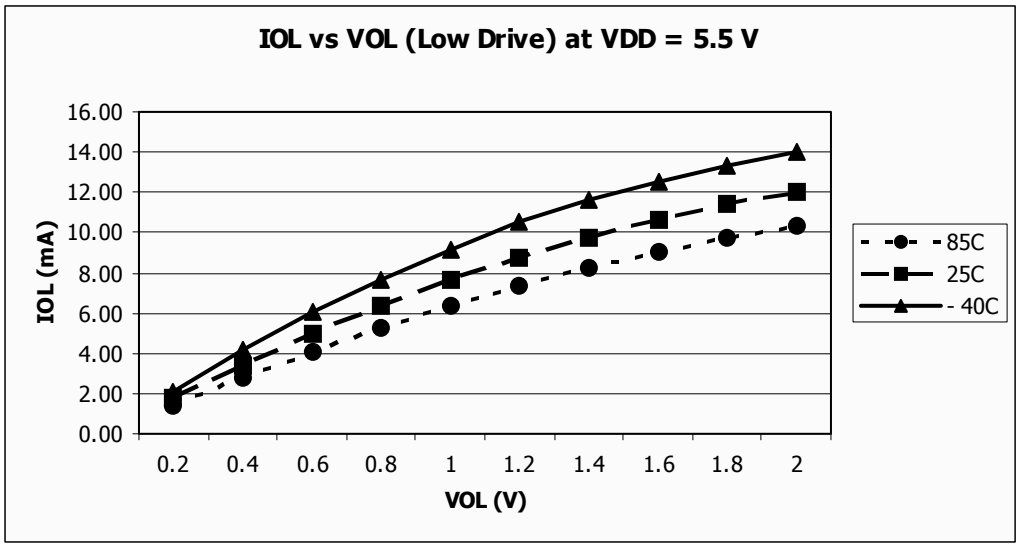


Figure 25. Typical I_{OL} vs. V_{OL}
V_{DD} = 5.5 V (Low Drive)

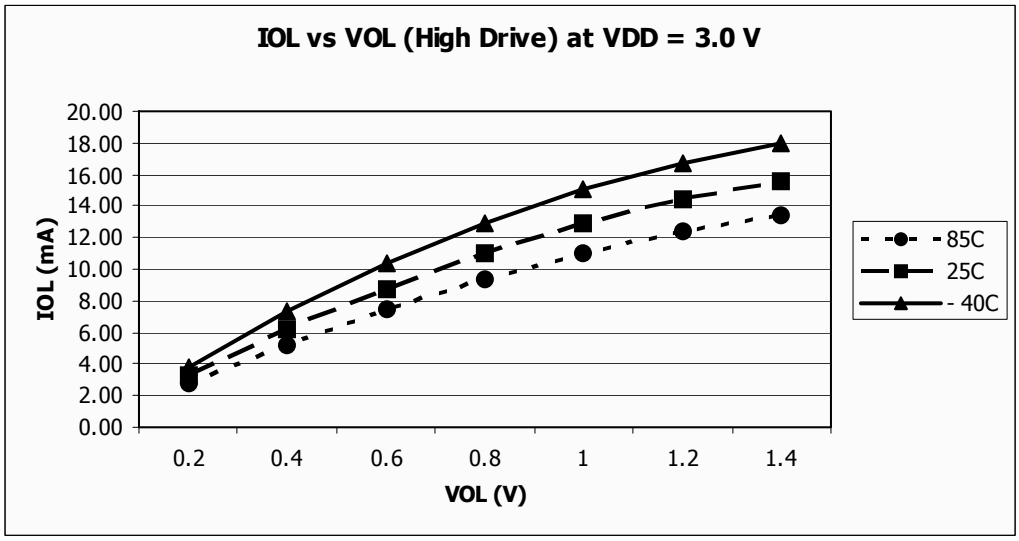


Figure 26. Typical I_{OL} vs. V_{OL}
V_{DD} = 3 V (High Drive)

Table 8. Supply Current Characteristics (continued)

N	C	Parameter	Symbol	V_{DD} (V)	Typical	Max[1]	Temp. (°C)	Unit
7	C	Wait mode supply current[3] measured at (f_{Bus} = 2.00 MHz)	WI_{DD2}	5	841.13 859.98 873.69	—	–40 25 85	µA
8	T			3	840.21 850.60 846.67	—	–40 25 85	
9	T			1.80	630.64 635.10 643.67	—	–40 25 85	
10	C	Wait mode supply current[3] measured at (f_{Bus} = 1.00 MHz)	WI_{DD1}	5	667.86 683.38 688.02	—	–40 25 85	µA
11	T			3	666.34 672.79 669.15	—	–40 25 85	
12	T			1.80	505.39 509.28 502.52	—	–40 25 85	
13	P	Stop mode supply current	SI_{DD}	5	1.15 1.40 7.67	11	–40 25 85	µA
14	C			3	1.05 1.26 4.52	—	–40 25 85	
15	C			1.80	0.39 0.56 4.21	—	–40 25 85	
16	C	ADC adder from stop[3]	—	5	128.86 140.44 154.97	—	–40 25 85	µA
17	T			3	102.98 111.71 118.33	—	–40 25 85	
18	T			1.80	54.77 66.33 74.42	—	–40 25 85	
19	C	ACMP adder from stop (ACME = 1)	—	5	14.43 15.96 16.77	—	–40 25 85	µA
20	T			3	14.37 14.72 14.45	—	–40 25 85	
21	T			1.80	13.05 14.02 12.92	—	–40 25 85	

Table 8. Supply Current Characteristics (continued)

N	C	Parameter	Symbol	V_{DD} (V)	Typical	Max[1]	Temp. (°C)	Unit
22	C	RTI adder from stop with 1 kHz clock source enabled[4]	—	5	0.10 0.10 0.17	—	–40 25 85	µA
23	T			3	0.02 0.06 0.02	—	–40 25 85	
24	T			1.80	0.40 0.45 0.20	—	–40 25 85	
25	T	RTI adder from stop with 32.768KHz external clock source reference enabled	—	5	0.70 1.08 1.94	—	–40 25 85	µA
26	T			3	0.56 0.56 0.62	—	–40 25 85	
27	T			1.80	0.70 0.86 0.50	—	–40 25 85	
28	C	LVI adder from stop (LVDE = 1 and LVDSE = 1)	—	5	58.93 68.27 76.60	—	–40 25 85	µA
29	T			3	58.89 61.98 63.45	—	–40 25 85	
30	T			1.80	52.84 54.52 52.49	—	–40 25 85	

1 Maximum value is measured at the nominal V_{DD} voltage times 10% tolerance. Values given here are preliminary estimates prior to completing characterization.

2 Not include any DC loads on port pins.

3 Required asynchronous ADC clock and LVD to be enabled.

4 Most customers are expected to find that auto-wakeup from stop can be used instead of the higher current wait mode. Wait mode typical is 672.79 µA at 3 V and 509.28 µA at 1.8 V with f_{Bus} = 1 MHz.

Table 12. Analog Comparator Electrical Specifications (continued)

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
9	P	Analog Comparator bandgap reference voltage	V_{BG}	1.1	1.208	1.3	V

1 These data are characterized but not production tested.

3.11 Internal Clock Source Characteristics

Table 13. Internal Clock Source Specifications

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	C	Average internal reference frequency — untrimmed	f_{int_ut}	25	31.25	41.66	kHz
2	P	Average internal reference frequency — trimmed	f_{int_t}	31.25	32.768	39.0625	kHz
3	C	DCO output frequency range — untrimmed	f_{dco_ut}	12.8	16	21.33	MHz
4	P	DCO output frequency range — trimmed	f_{dco_t}	16	16.77	20	MHz
5	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco\_res\_t}$	—	—	0.2	$\%f_{dco}$
6	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	—	2	$\%f_{dco}$
7	C	FLL acquisition time[2,3]	$t_{acquire}$	—	—	1	ms
8	C	Stop recovery time (FLL wakeup to previous acquired frequency) IREFSTEN = 0 IREFSTEN = 1	t_wakeup	—	 100 86	—	µs

1 Data in typical column was characterized at 3.0 V and 5.0 V, 25 °C or is typical recommended value.

2 This parameter is characterized and not tested on each device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBILP) to FLL enabled (FEI, FBI).

3.12 ADC Characteristics

Table 14. 10-Bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	1.8	—	5.5	V	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	
Analog source resistance	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ	External to MCU
	8-bit mode (all valid f_{ADCK})		—	—	10		

Table 15. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 2.7 V < V_{DDAD} < 5.5 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
C	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	0.582	1	mA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	E_{TUE}	—	±1.5	±3.5	LSB[2]	Includes quantization
		8-bit mode		—	±0.7	±1.5		
T	Differential Non-Linearity	10-bit mode	DNL	—	±0.5	±1.0	LSB[2]	
		8-bit mode		—	±0.3	±0.5		
		Monotonicity and No-Missing-Codes guaranteed						
C	Integral Non-Linearity	10-bit mode	INL	—	±0.5	±1.0	LSB[2]	
		8-bit mode		—	±0.3	±0.5		
P	Zero-Scale Error	10-bit mode	E_{ZS}	—	±1.5	±2.5	LSB[2]	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	±0.5	±0.7		
P	Full-Scale Error	10-bit mode	E_{FS}	—	±1	±1.5	LSB[2]	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	±0.5	±0.5		
D	Quantization Error	10-bit mode	E_Q	—	—	±0.5	LSB[2]	
		8-bit mode		—	—	±0.5		
D	Input Leakage Error	10-bit mode	E_{IL}	—	±0.2	±2.5	LSB[2]	Pad leakage[2] * R_{AS}
		8-bit mode		—	±0.1	±1		

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 Based on input pad leakage current. Refer to pad electricals.

Table 16. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 1.8 V < V_{DDAD} < 2.7 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	8-bit mode	I_{DDAD}	—	88	—	μA	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	8-bit mode	I_{DDAD}	—	152	—	μA	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	8-bit mode	I_{DDAD}	—	214	—	μA	
T	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	8-bit mode	I_{DDAD}	—	390	—	μA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	E_{TUE}	—	—	—	LSB[2]	Includes quantization
		8-bit mode		—	±3.5	—		
T	Differential Non-Linearity	10-bit mode	DNL	—	—	—	LSB[2]	
		8-bit mode		—	±1.0	—		
		Monotonicity and No-Missing-Codes guaranteed						
C	Integral Non-Linearity	10-bit mode	INL	—	—	—	LSB[2]	
		8-bit mode		—	±1.5	—		
C	Zero-Scale Error	10-bit mode	E_{ZS}	—	—	—	LSB[2]	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	±1.5	—		
C	Full-Scale Error	10-bit mode	E_{FS}	—	—	—	LSB[2]	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	±1.0	—		
D	Quantization Error	10-bit mode	E_Q	—	—	—	LSB[2]	
		8-bit mode		—	—	±0.5		

Table 16. 10-Bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}, 1.8 V < V_{DDAD} < 2.7 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
D	Input Leakage Error	10-bit mode	E_{IL}	—	—	—	LSB[2]	Pad leakage[2] * R_{AS}
		8-bit mode		—	±0.1	±1		

1 Typical values assume V_{DDAD} = 1.8 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

Table 17. Flash Characteristics

No.	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	D	Supply voltage for program/erase	V_{DD}	2.7	—	5.5	V
2	D	Program/Erase voltage	V_{PP}	11.8	12	12.2	V
3	C	V_{PP} current Program Mass erase	 I_{VPP_prog} I_{VPP_erase}	 — —	 — —	 200 100	 µA µA
4	D	Supply voltage for read operation 0 < f_{Bus} < 10 MHz	V_{Read}	1.8	—	5.5	V
5	P	Byte program time	t_{prog}	20	—	40	µs
6	P	Mass erase time	t_{me}	500	—	—	ms
7	C	Cumulative program HV time[2]	t_{hv}	—	—	8	ms
8	C	Total cumulative HV time (total of t_{me} & t_{hv} applied to device)	t_{hv_total}	—	—	2	hours
9	D	HVEN to program setup time	t_{pgs}	10	—	—	µs
10	D	PGM/MASS to HVEN setup time	t_{nvs}	5	—	—	µs
11	D	HVEN hold time for PGM	t_{nvh}	5	—	—	µs
12	D	HVEN hold time for MASS	t_{nvh1}	100	—	—	µs
13	D	V_{PP} to PGM/MASS setup time	t_{vps}	20	—	—	ns
14	D	HVEN to V_{PP} hold time	t_{vph}	20	—	—	ns
15	D	V_{PP} rise time[3]	t_{vrs}	200	—	—	ns
16	D	Recovery time	t_{rcv}	1	—	—	µs
17	D	Program/erase endurance T_L to T_H = –40 °C to 85 °C	—	1000	—	—	cycles
18	C	Data retention	t_{D_ret}	15	—	—	years

1 Typicals are measured at 25 °C.

2 t_{hv} is the cumulative high voltage programming time to the same row before next erase. Same address can not be programmed more than twice before next erase.

3 Fast V_{PP} rise time may potentially trigger the ESD protection structure, which may result in over current flowing into the pad and cause permanent damage to the pad. External filtering for the V_{PP} power source is recommended. An example V_{PP} filter is shown in Figure 35.

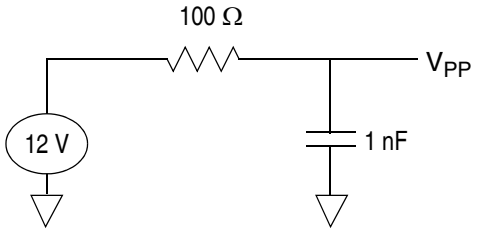
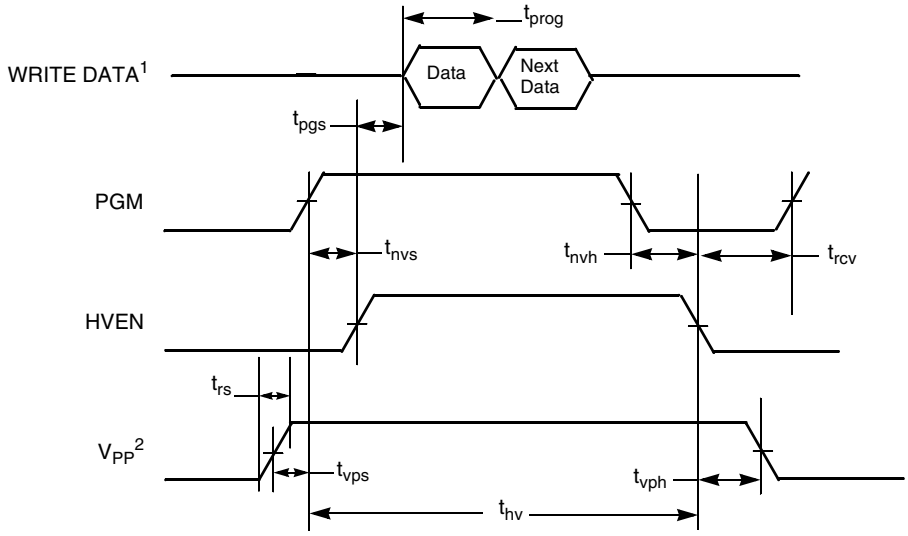


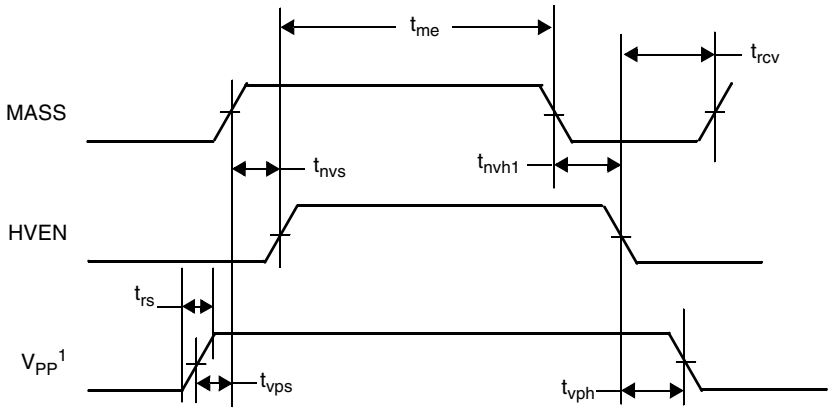
Figure 35. Example V_{PP} Filtering



1 Next Data applies if programming multiple bytes in a single row, refer to *MC9RS08KB12 Series Reference Manual*.

2 V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 36. Flash Program Timing



1 V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 37. Flash Mass Erase Timing

3.14 EMC Performance

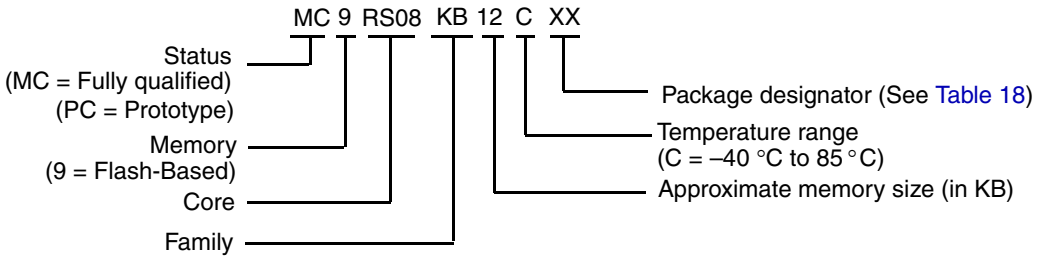
Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

4 Ordering Information

This section contains ordering numbers for MC9RS08KB12 series devices. See below for an example of the device numbering system.



5 Package Information and Mechanical Drawings

Table 18 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9RS08KB12 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 18, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 18) in the "Enter Keyword" search box at the top of the page.

Table 18. Device Numbering System

Device Number	Memory		Package		
	Flash	RAM	Type	Designator	Document No.
MC9RS08KB12 **MC9RS08KB8** **MC9RS08KB4**	12 KB 8 KB 4 KB	254 bytes 254 bytes 126 bytes	24 QFN	FK	98ASA00087D
			20 SOIC WB	WJ	98ASB42343B
			16 SOIC NB	SG	98ASB42566B
			16 TSSOP	TG	98ASH70247A
MC9RS08KB2	2 KB	126 bytes	8 SOIC NB	SC	98ASB42564B
			8 DFN	DC	98ARL10557D