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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

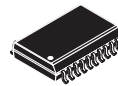|	
Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	126 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9rs08kb4cwj

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

Addendum for New QFN Package Migration, Rev. 0

Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9RS08KB12
Rev. 5, 1/2012

✔RoHS

MC9RS08KB12

MC9RS08KB12 Series

Covers: MC9RS08KB12
MC9RS08KB8
MC9RS08KB4
MC9RS08KB2

- 8-Bit RS08 Central Processor Unit (CPU)
  - Up to 20 MHz CPU at 1.8 V to 5.5 V across temperature range of –40 °C to 85 °C
  - Subset of HC08 instruction set with added BGND instruction
  - Single Global interrupt vector
- On-Chip Memory
  - Up to 12 KB flash read/program/erase over full operating voltage and temperature, 12 KB/8 KB/4 KB/2 KB flash are optional
  - Up to 254-byte random-access memory (RAM), 254-byte/126-byte RAM are optional
  - Security circuitry to prevent unauthorized access to flash contents
- Power-Saving Modes
  - Wait mode — CPU shuts down; system clocks continue to run; full voltage regulation
  - Stop mode — CPU shuts down; system clocks are stopped; voltage regulator in standby
  - Wakeup from power-saving modes using RTI, KBI, ADC, ACMP, SCI and LVD
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies up to 10 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal low power oscillator
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset
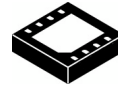 - Illegal address detection with reset
  - Flash-block protection

20-Pin SOIC
Case 751D

24-Pin QFN
Case 1982-01
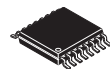
16-Pin TSSOP
Case 948F

16-Pin SOIC N/B
Case 751B

8-Pin DFN
Case 1452-02

8-Pin SOIC
Case 751

- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
  - **ADC** — 12-channel, 10-bit resolution; 2.5 μs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop; hardware trigger
  - **ACMP** — Analog comparator; full rail-to-rail supply operation; option to compare to fixed internal bandgap reference voltage; can operate in stop mode
  - **TPM** — One 2-channel timer/pulse-width modulator module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - **IIC** — Inter-integrated circuit bus module capable of operation up to 100 kbps with maximum bus loading; capable of higher baud rates with reduced loading
  - **SCI** — One serial communications interface module with optional 13-bit break; LIN extensions
  - **MTIM** — Two 8-bit modulo timers; optional clock sources
  - **RTI** — One real-time clock with optional clock sources
  - **KBI** — Keyboard interrupts; up to 8 ports
- Input/Output
  - 18 GPIOs in 24- and 20-pin packages; 14 GPIOs in 16-pin package; 6 GPIOs in 8-pin package; including one output-only pin and one input-only pin
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package Options
  - MC9RS08KB12/MC9RS08KB8/MC9RS08KB4
    - 24-pin QFN, 20-pin SOIC, 16-pin SOIC NB or TSSOP
  - MC9RS08KB2
    - 8-pin SOIC or DFN

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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Table 1. Pin Availability by Package Pin-Count

Pin Number					<-- Lowest **Priority** --> Highest			
24	**20**	**16**	**8**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	3	3	3					V_{DD}
2	—	—	—	NC				
3	4	4	4					V_{SS}
4	5	5	—	PTB7	SCL[1]			EXTAL
5	6	6	—	PTB6	SDA[1]			XTAL
6	7	7	—	PTB5	TPMCH1[2]			
7	8	8	—	PTB4	TPMCH0[2]			
8	9	—	—	PTC3			ADP11	
9	10	—	—	PTC2			ADP10	
10	11	—	—	PTC1			ADP9	
11	12	—	—	PTC0			ADP8	
12	13	9	—	PTB3	KBIP7		ADP7	
13	14	10	—	PTB2	KBIP6		ADP6	
14	15	11	—	PTB1	KBIP5	TxD[3]	ADP5	
15	16	12	—	PTB0	KBIP4	RxD[3]	ADP4	
16	17	13	5	PTA3	KBIP3	SCL[1]	TxD[3]	ADP3
17	18	14	6	PTA2	KBIP2	SDA[1]	RxD[3]	ADP2
18	19	15	7	PTA1	KBIP1	TPMCH1[2]	ADP1	ACMP−
19	20	16	8	PTA0	KBIP0	TPMCH0[2]	ADP0	ACMP+
20	—	—	—	NC				
21	—	—	—	NC				
22	—	—	—	NC				
23	1	1	1	PTA5		TCLK	$\overline{\text{RESET}}$	V_{PP}
24	2	2	2	PTA4	ACMPO	BKGD	MS	

[1] IIC pins can be remapped to PTB6 and PTB7, default reset location is PTA2 and PTA3. It can be configured only once.

[2] TPM pins can be remapped to PTB4 and PTB5, default reset location is PTA0 and PTA1.

[3] SCI pins can be remapped to PTA2 and PTA3, default reset location is PTB0 and PTB1. It can be configured only once.

Table 2. Parameter Classifications

D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

3.3   Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	−0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	−55 to 150	°C

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{RESET}$/V_{PP} pin which is internally clamped to V_{SS} only.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external VDD load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.4   Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of

unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H −40 to 85	°C
Maximum junction temperature	T_{JMAX}	150	°C
Thermal resistance 24-pin QFN	θ_{JA}	113	°C/W
Thermal resistance 20-pin SOIC	θ_{JA}	83	°C/W
Thermal resistance 16-pin SOIC NB	θ_{JA}	103	°C/W
Thermal resistance 16-pin TSSOP	θ_{JA}	29	°C/W
Thermal resistance 8-pin SOIC	θ_{JA}	150	°C/W
Thermal resistance 8-pin DFN	θ_{JA}	110	°C/W

The average chip-junction temperature (TJ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C /W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts chip internal power

$P_{I/O}$ = Power dissipation on input and output pins user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between PD and TJ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (PD)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5   ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

During the device qualification ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-Up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	1	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at $T_A = 85\ °C$	I_{LAT}	±100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient)

No.	C	Parameter	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage (run, wait and stop modes.) $0 < f_{Bus} <10$ MHz	V_{DD}	1.8	—	5.5	V
2	C	Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	0.8[1]	—	—	V
3	P	Low-voltage detection threshold (V_{DD} falling) (V_{DD} rising)	V_{LVD}	1.80 1.88	1.86 1.94	1.95 2.05	V
4	C	Power on RESET (POR) voltage	V_{POR}[1]	0.9	—	1.7	V
5	C	Input high voltage ($V_{DD} > 2.3$V) (all digital inputs)	V_{IH}	$0.70 \times V_{DD}$	—	—	V
6	C	Input high voltage (1.8 V $\leq V_{DD} \leq$ 2.3 V) (all digital inputs)	V_{IH}	$0.85 \times V_{DD}$	—	—	V
7	C	Input low voltage ($V_{DD} > 2.3$ V) (all digital inputs)	V_{IL}	—	—	$0.30 \times V_{DD}$	V
8	C	Input low voltage (1.8 V $\leq V_{DD} \leq$ 2.3 V) (all digital inputs)	V_{IL}	—	—	$0.30 \times V_{DD}$	V
9	C	Input hysteresis (all digital inputs)	V_{hys}[1]	$0.06 \times V_{DD}$	—	—	V
10	P	Input leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS}, all input only pins	$|I_{In}|$	—	0.025	1.0	µA
11	P	High impedance (off-state) leakage current (per pin) $V_{In} = V_{DD}$ or V_{SS}, all input/output	$|I_{ozl}|$	—	0.025	1.0	µA
12	P	Internal pullup resistors[2] (all port pins)	R_{PU}	20	45	65	kΩ
13	P	Internal pulldown resistors[2] (all port pins)	R_{PD}	20	45	65	kΩ
14	C	Output high voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA 1.8 V, I_{Load} = 0.5 mA Output high voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 3 mA 1.8 V, I_{Load} = 2 mA	V_{OH}	$V_{DD} - 0.8$ — — $V_{DD} - 0.8$ — —	— — — — — —	— — — — — —	V
15	C	Maximum total IOH for all port pins	$|I_{OHT}|$	—	—	40	mA
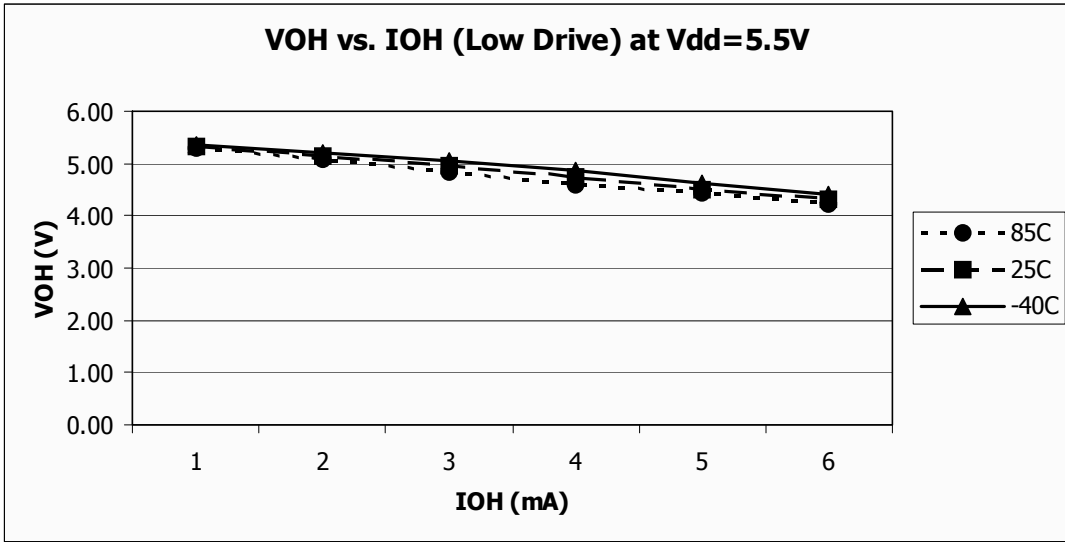
Figure 7. Typical V$_{OH}$ vs. I$_{OH}$
V$_{DD}$ = 5.5 V (Low Drive)
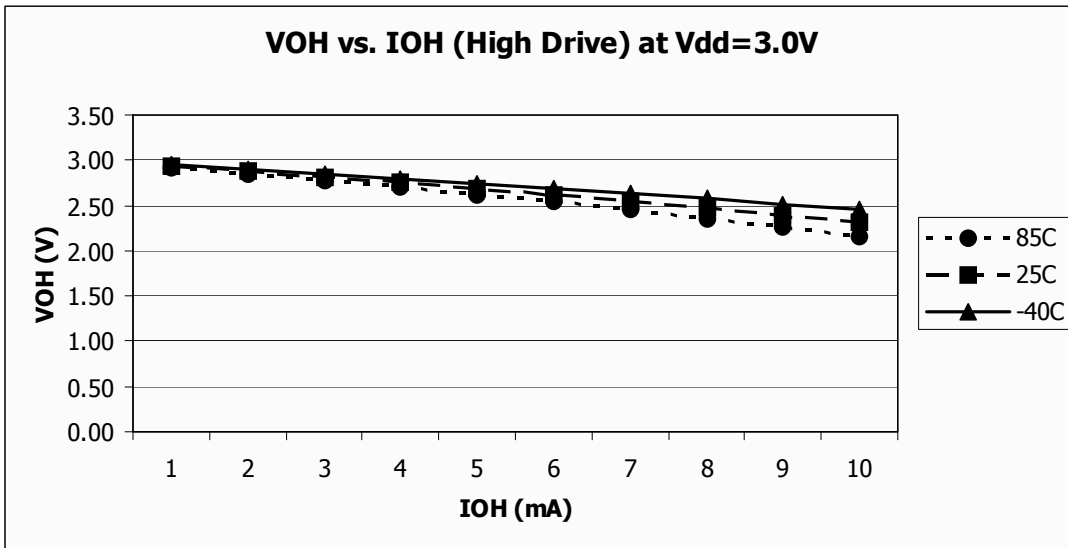
Figure 8. Typical V$_{OH}$ vs. I$_{OH}$
V$_{DD}$ = 3.0 V (High Drive)

VOH vs. IOH (Low Drive) at Vdd=3.0V
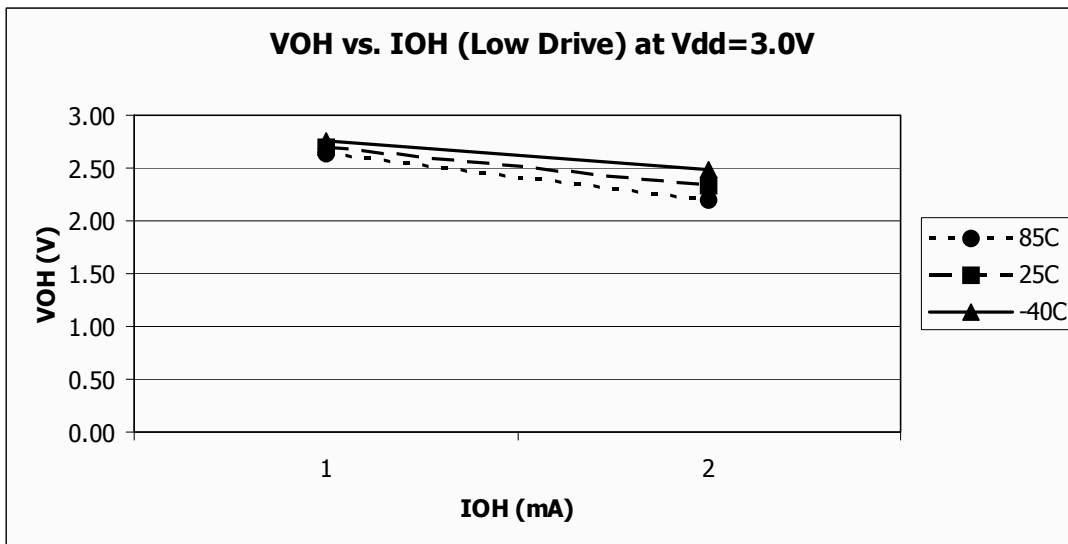
Figure 9. Typical V_{OH} vs. I_{OH}
V_{DD} = 3.0 V (Low Drive)

VOH vs. IOH (High Drive) at Vdd=1.8V
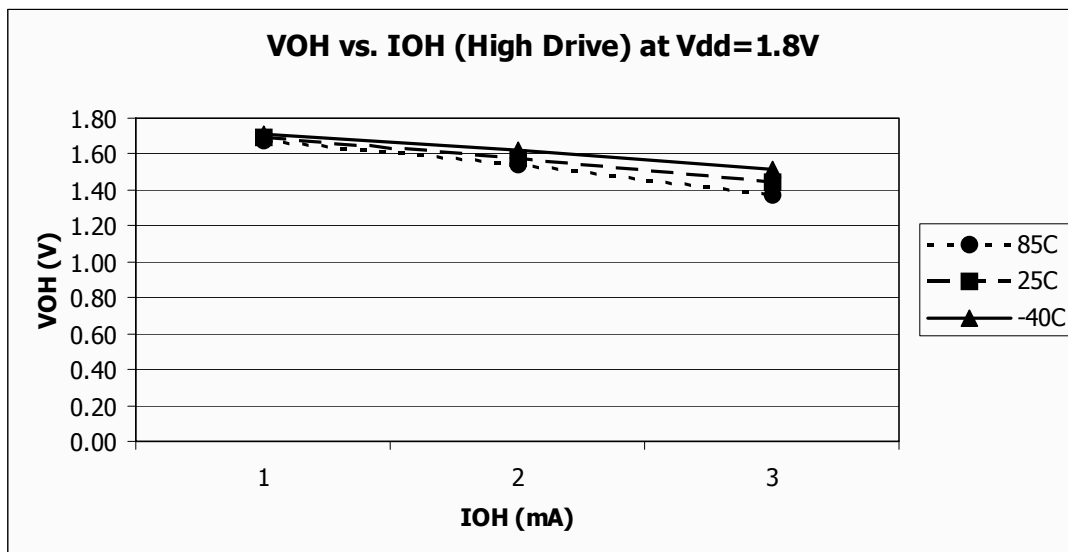
Figure 10. Typical V_{OH} vs. I_{OH}
V_{DD} = 1.8 V (High Drive)

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VOH vs. IOH (Low Drive) at Vdd=1.8V

- ● - 85C
- ■ - 25C
- ▲ - -40C

X-axis: IOH (mA) — 0.3, 0.4, 0.5, 0.6, 0.7
Y-axis: VOH (V) — 0.00, 0.20, 0.40, 0.60, 0.80, 1.00, 1.20, 1.40, 1.60, 1.80
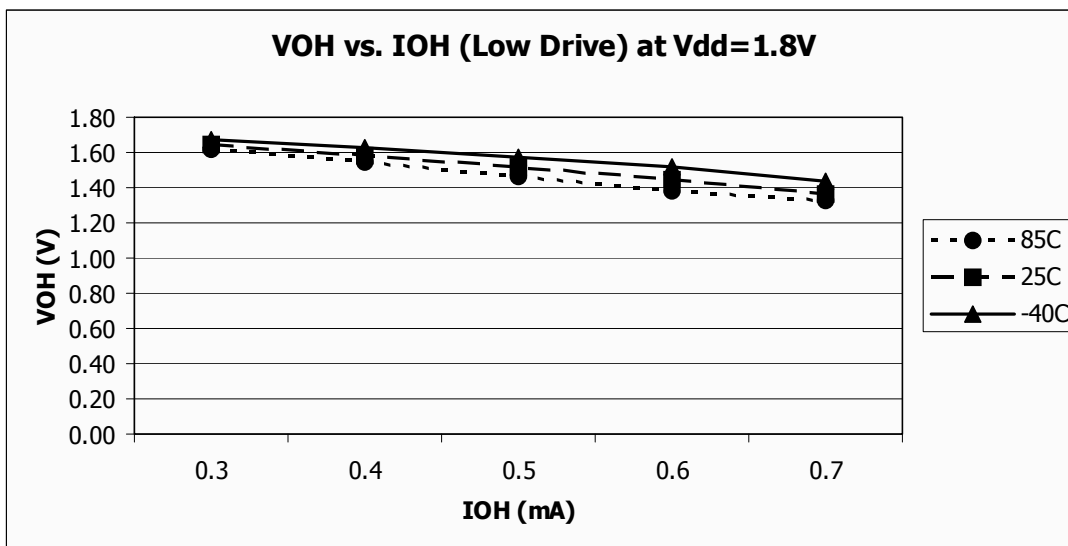
Figure 11. Typical V$_{OH}$ vs. I$_{OH}$
V$_{DD}$ = 1.8 V (Low Drive)

VOL vs. IOL (High Drive) at Vdd=5.5V

- ▲ VOL @85C
- ■ VOL @25C
- ● VOL @-40C

X-axis: IOL (mA) — 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
Y-axis: VOL (mV) — 0.00, 100.00, 200.00, 300.00, 400.00, 500.00, 600.00, 700.00, 800.00
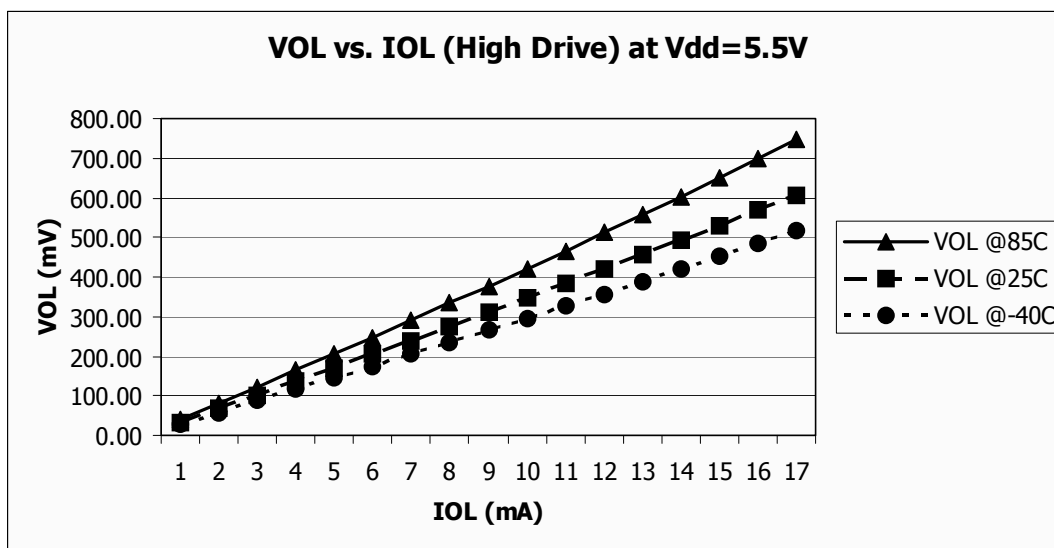
Figure 12. Typical V$_{OL}$ vs. I$_{OL}$
V$_{DD}$ = 5.5 V (High Drive)
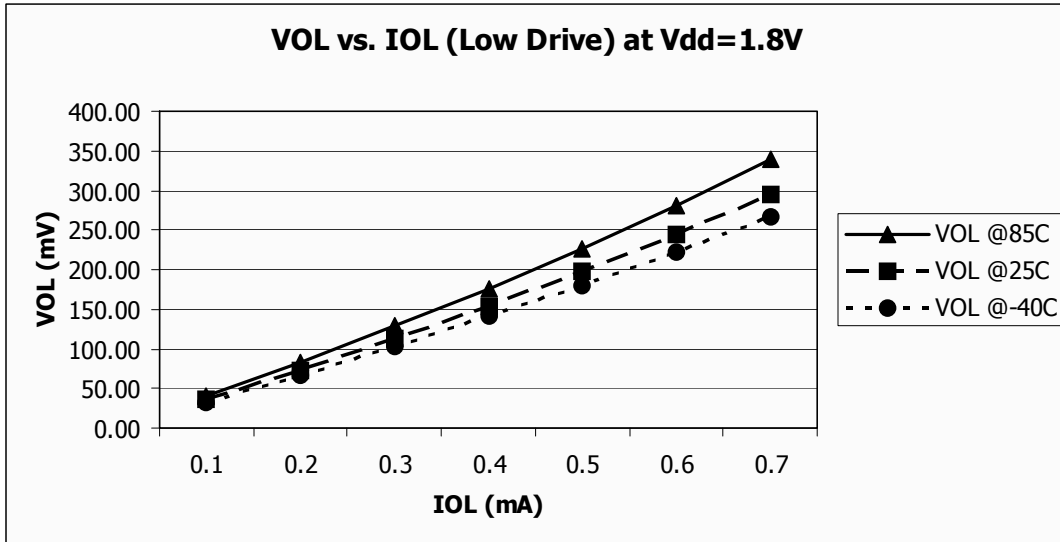
Figure 17. Typical V_{OL} vs. I_{OL}
V_{DD} = 1.8 V (Low Drive)
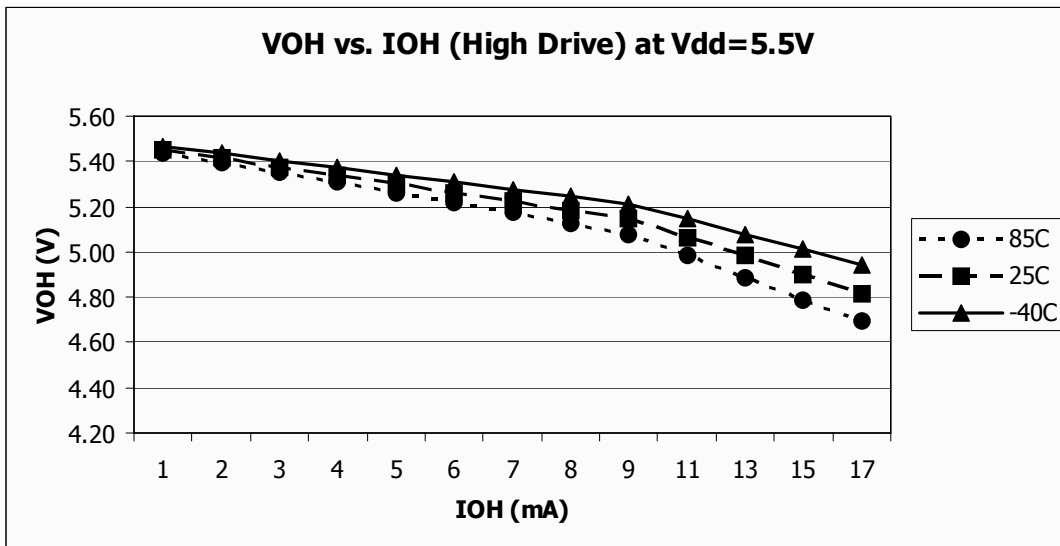
Figure 18. Typical I_{OH} vs. V_{DD}–V_{OH}
V_{DD} = 5.5 V (High Drive)

IOH vs VDD-VOH (Low Drive) at VDD = 3.0 V
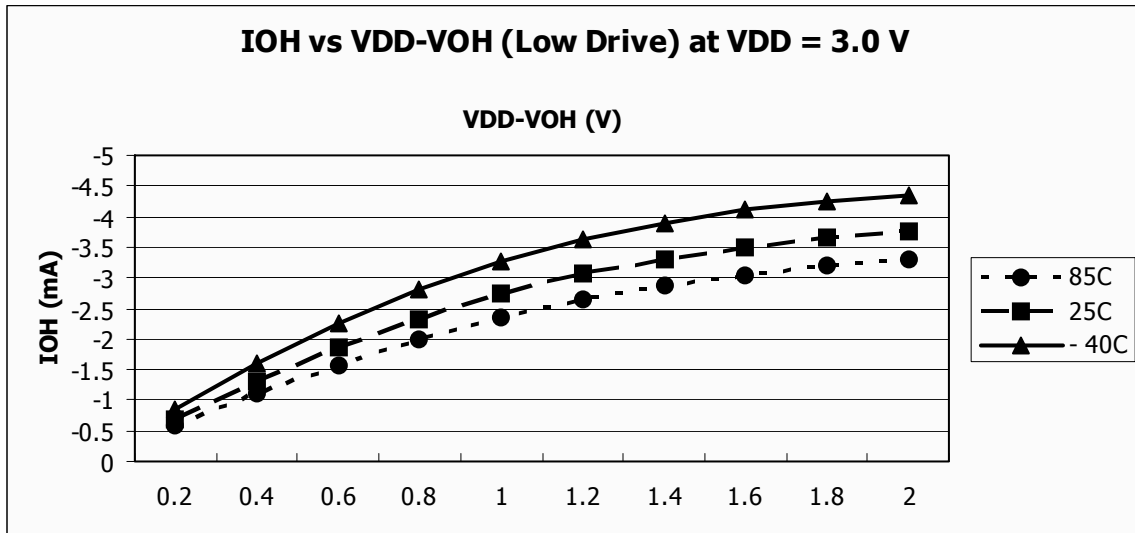
Figure 21. Typical I_{OH} vs. V_{DD}–V_{OH}
V_{DD} = 3 V (Low Drive)

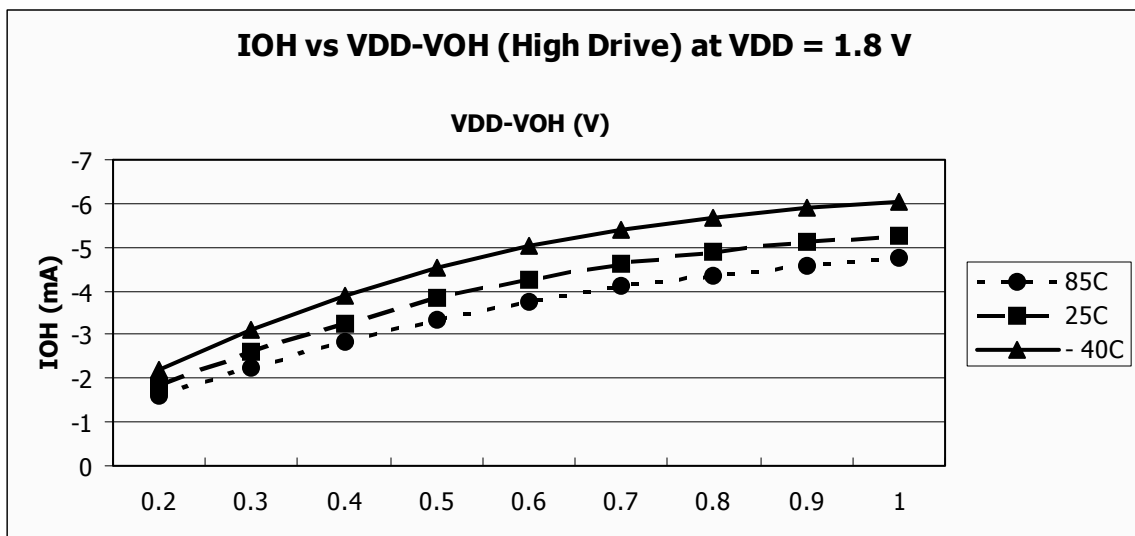**IOH vs VDD-VOH (High Drive) at VDD = 1.8 V**

Figure 22. Typical I_{OH} vs. V_{DD}–V_{OH}
V_{DD} = 1.8 V (High Drive)
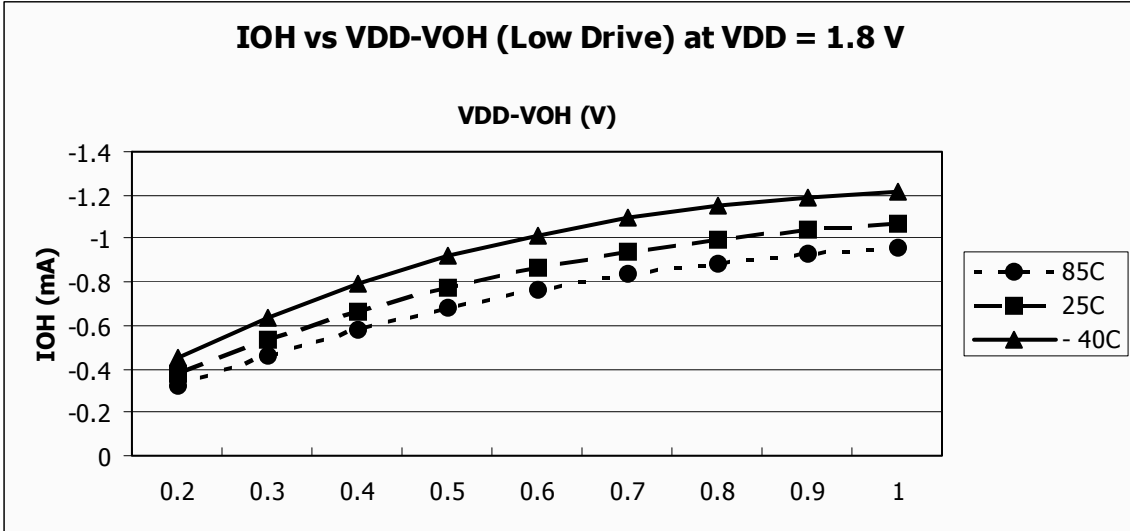
Figure 23. Typical I$_{OH}$ vs. V$_{DD}$–V$_{OH}$
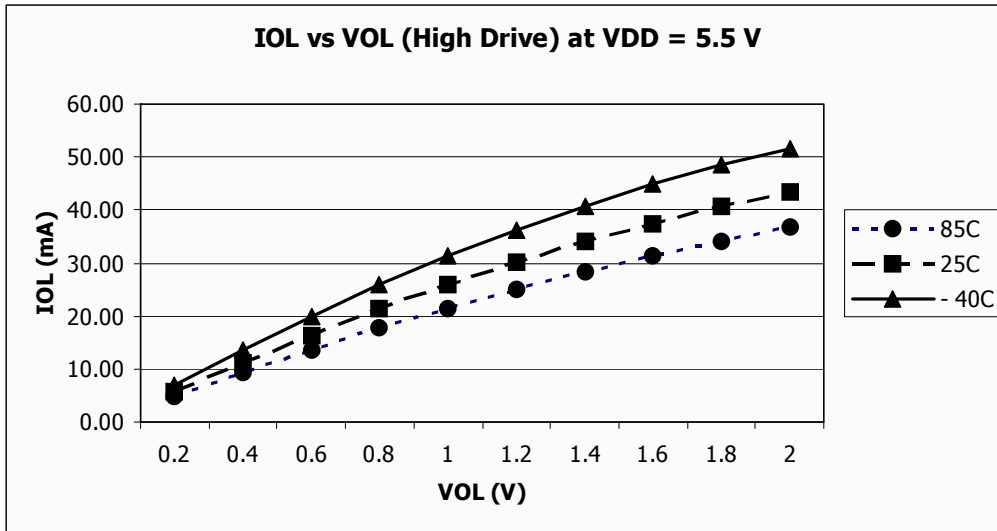**V$_{DD}$ = 1.8 V (Low Drive)**

Figure 24. Typical I$_{OL}$ vs. V$_{OL}$
V$_{DD}$ = 5.5 V (High Drive)

MC9RS08KB12 Series MCU Data Sheet, Rev. 5

3.9.1 Control Timing

Table 10. Control Timing

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	0	—	10	MHz
2	D	Real time interrupt internal oscillator period	t_{RTI}	700	1000	1300	μs
3	D	External $\overline{RESET}$ pulse width[1]	t_{extrst}	150	—	—	ns
4	D	KBI pulse width[2]	t_{KBIPW}	1.5 t_{cyc}	—	—	ns
5	D	KBI pulse width in stop[1]	t_{KBIPWS}	100	—	—	ns
6	D	Port rise and fall time (load = 50 pF)[3] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	11 35	— —	ns

[1] This is the shortest pulse guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

[2] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

[3] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.
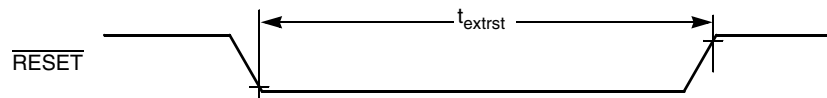
Figure 30. Reset Timing
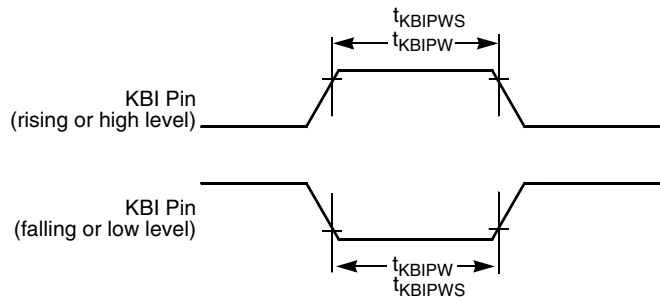
Figure 31. KBI Pulse Width

3.9.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}
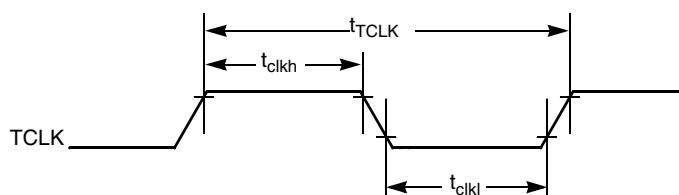
Figure 32. Timer External Clock
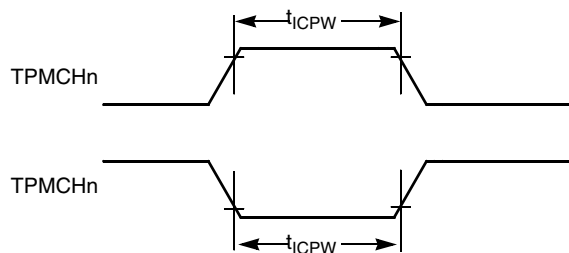
Figure 33. Timer Input Capture Pulse

3.10 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.80	—	5.5	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	μA
3	D	Analog input voltage[1]	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
4	C	Analog input offset voltage[1]	V_{AIO}	—	20	40	mV
5	C	Analog Comparator hysteresis[1]	V_H	3.0	9.0	15.0	mV
6	C	Analog source impedance[1]	R_{AS}	—	—	10	$k\Omega$
7	P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
8	C	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	μs

Table 14. 10-Bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
ADC conversion clock Freq.	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC=1)		0.4	—	4.0		

[1] Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
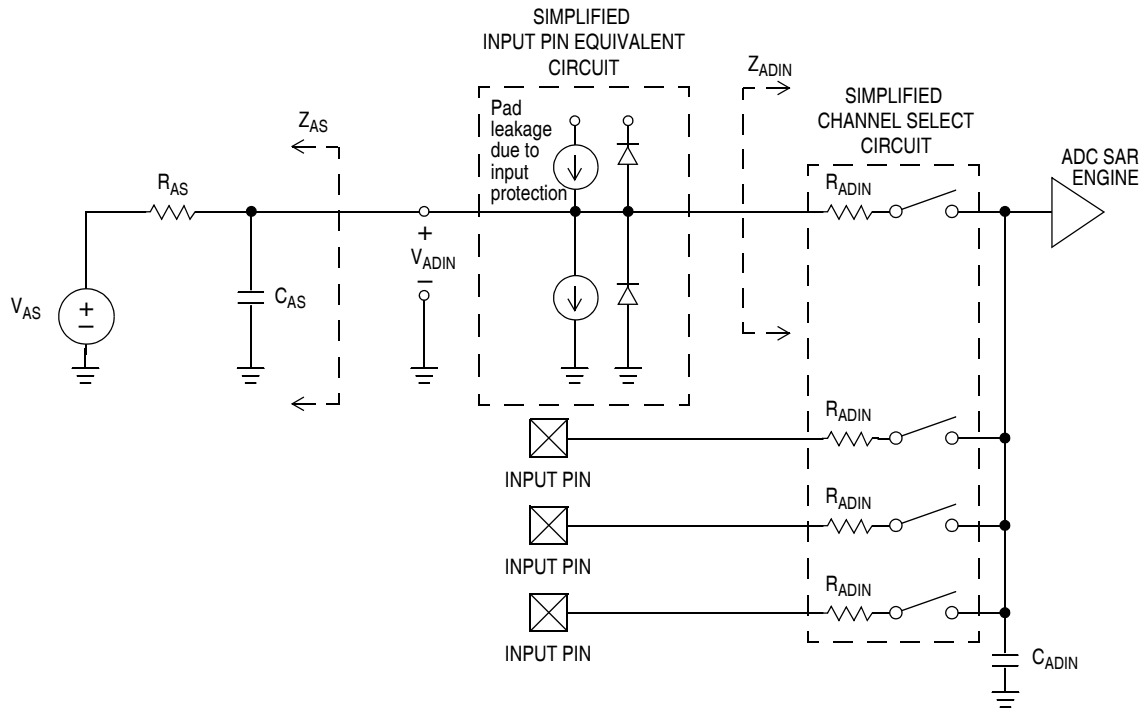
Figure 34. ADC Input Impedance Equivalency Diagram

Table 15. 10-Bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}, 2.7 V < V_{DDAD} < 5.5 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	133	—	µA	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	218	—	µA	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	327	—	µA	

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Table 15. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 2.7 V < V_{DDAD} < 5.5 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
C	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	0.582	1	mA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = 1/f_{ADACK}
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	E_{TUE}	—	±1.5	±3.5	LSB[2]	Includes quantization
		8-bit mode		—	±0.7	±1.5		
T	Differential Non-Linearity	10-bit mode	DNL	—	±0.5	±1.0	LSB[2]	
		8-bit mode		—	±0.3	±0.5		
		Monotonicity and No-Missing-Codes guaranteed						
C	Integral Non-Linearity	10-bit mode	INL	—	±0.5	±1.0	LSB[2]	
		8-bit mode		—	±0.3	±0.5		
P	Zero-Scale Error	10-bit mode	E_{ZS}	—	±1.5	±2.5	LSB[2]	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	±0.5	±0.7		
P	Full-Scale Error	10-bit mode	E_{FS}	—	±1	±1.5	LSB[2]	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	±0.5	±0.5		
D	Quantization Error	10-bit mode	E_Q	—	—	±0.5	LSB[2]	
		8-bit mode		—	—	±0.5		
D	Input Leakage Error	10-bit mode	E_{IL}	—	±0.2	±2.5	LSB[2]	Pad leakage[2] * R_{AS}
		8-bit mode		—	±0.1	±1		

[1] Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] Based on input pad leakage current. Refer to pad electricals.

Table 16. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 1.8 V < V_{DDAD} < 2.7 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	8-bit mode	I_{DDAD}	—	88	—	µA	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	8-bit mode	I_{DDAD}	—	152	—	µA	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	8-bit mode	I_{DDAD}	—	214	—	µA	
T	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	8-bit mode	I_{DDAD}	—	390	—	µA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	E_{TUE}	—	—	—	LSB^2	Includes quantization
		8-bit mode		—	±3.5	—		
T	Differential Non-Linearity	10-bit mode	DNL	—	—	—	LSB^2	
		8-bit mode		—	±1.0	—		
		Monotonicity and No-Missing-Codes guaranteed						
C	Integral Non-Linearity	10-bit mode	INL	—	—	—	LSB^2	
		8-bit mode		—	±1.5	—		
C	Zero-Scale Error	10-bit mode	E_{ZS}	—	—	—	LSB^2	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	±1.5	—		
C	Full-Scale Error	10-bit mode	E_{FS}	—	—	—	LSB^2	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	±1.0	—		
D	Quantization Error	10-bit mode	E_Q	—	—	—	LSB^2	
		8-bit mode		—	—	±0.5		

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Table 16. 10-Bit ADC Characteristics (V$_{REFH}$ = V$_{DDAD}$, V$_{REFL}$ = V$_{SSAD}$, 1.8 V < V$_{DDAD}$ < 2.7 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
D	Input Leakage Error	10-bit mode	E$_{IL}$	—	—	—	LSB[2]	Pad leakage[2] * R$_{AS}$
		8-bit mode		—	±0.1	±1		

[1] Typical values assume V$_{DDAD}$ = 1.8 V, Temp = 25 °C, f$_{ADCK}$ = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

Table 17. Flash Characteristics

No.	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	D	Supply voltage for program/erase	V$_{DD}$	2.7	—	5.5	V
2	D	Program/Erase voltage	V$_{PP}$	11.8	12	12.2	V
3	C	V$_{PP}$ current Program Mass erase	I$_{VPP\_prog}$ I$_{VPP\_erase}$	— —	— —	200 100	μA μA
4	D	Supply voltage for read operation 0 < f$_{Bus}$ < 10 MHz	V$_{Read}$	1.8	—	5.5	V
5	P	Byte program time	t$_{prog}$	20	—	40	μs
6	P	Mass erase time	t$_{me}$	500	—	—	ms
7	C	Cumulative program HV time[2]	t$_{hv}$	—	—	8	ms
8	C	Total cumulative HV time (total of t$_{me}$ & t$_{hv}$ applied to device)	t$_{hv\_total}$	—	—	2	hours
9	D	HVEN to program setup time	t$_{pgs}$	10	—	—	μs
10	D	PGM/MASS to HVEN setup time	t$_{nvs}$	5	—	—	μs
11	D	HVEN hold time for PGM	t$_{nvh}$	5	—	—	μs
12	D	HVEN hold time for MASS	t$_{nvh1}$	100	—	—	μs
13	D	V$_{PP}$ to PGM/MASS setup time	t$_{vps}$	20	—	—	ns
14	D	HVEN to V$_{PP}$ hold time	t$_{vph}$	20	—	—	ns
15	D	V$_{PP}$ rise time[3]	t$_{vrs}$	200	—	—	ns
16	D	Recovery time	t$_{rcv}$	1	—	—	μs
17	D	Program/erase endurance T$_L$ to T$_H$ = −40 °C to 85 °C	—	1000	—	—	cycles
18	C	Data retention	t$_{D\_ret}$	15	—	—	years

[1] Typicals are measured at 25 °C.

[2] t$_{hv}$ is the cumulative high voltage programming time to the same row before next erase. Same address can not be programmed more than twice before next erase.

[3] Fast V$_{PP}$ rise time may potentially trigger the ESD protection structure, which may result in over current flowing into the pad and cause permanent damage to the pad. External filtering for the V$_{PP}$ power source is recommended. An example V$_{PP}$ filter is shown in Figure 35.

3.14　EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.14.1　Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).