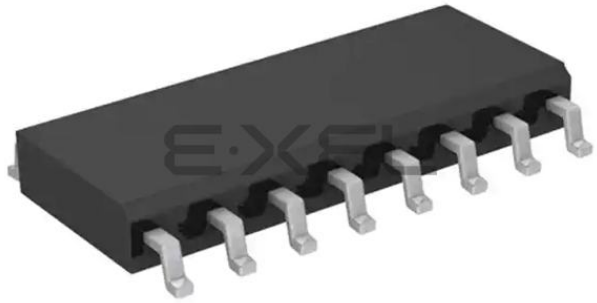

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	254 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9rs08kb8csg

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

Freescale Semiconductor
Data Sheet: Technical Data

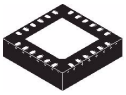
Document Number: MC9RS08KB12
Rev. 5, 1/2012

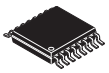
MC9RS08KB12

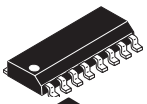
MC9RS08KB12 Series

Covers:MC9RS08KB12
MC9RS08KB8
MC9RS08KB4
MC9RS08KB2

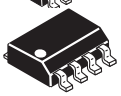

20-Pin SOIC
Case 751D


24-Pin QFN
Case 1982-01


16-Pin TSSOP
Case 948F


16-Pin SOIC N/B
Case 751B


8-Pin DFN
Case 1452-02


8-Pin SOIC
Case 751

- 8-Bit RS08 Central Processor Unit (CPU)
  - Up to 20 MHz CPU at 1.8 V to 5.5 V across temperature range of –40 °C to 85 °C
  - Subset of HC08 instruction set with added BGND instruction
  - Single Global interrupt vector
- On-Chip Memory
  - Up to 12 KB flash read/program/erase over full operating voltage and temperature, 12 KB/8 KB/4 KB/2 KB flash are optional
  - Up to 254-byte random-access memory (RAM), 254-byte/126-byte RAM are optional
  - Security circuitry to prevent unauthorized access to flash contents
- Power-Saving Modes
  - Wait mode — CPU shuts down; system clocks continue to run; full voltage regulation
  - Stop mode — CPU shuts down; system clocks are stopped; voltage regulator in standby
  - Wakeup from power-saving modes using RTI, KBI, ADC, ACMP, SCI and LVD
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies up to 10 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal low power oscillator
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash-block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
  - **ADC** — 12-channel, 10-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop; hardware trigger
  - **ACMP** — Analog comparator; full rail-to-rail supply operation; option to compare to fixed internal bandgap reference voltage; can operate in stop mode
  - **TPM** — One 2-channel timer/pulse-width modulator module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - **IIC** — Inter-integrated circuit bus module capable of operation up to 100 kbps with maximum bus loading; capable of higher baud rates with reduced loading
  - **SCI** — One serial communications interface module with optional 13-bit break; LIN extensions
  - **MTIM** — Two 8-bit modulo timers; optional clock sources
  - **RTI** — One real-time clock with optional clock sources
  - **KBI** — Keyboard interrupts; up to 8 ports
- Input/Output
  - 18 GPIOs in 24- and 20-pin packages; 14 GPIOs in 16-pin package; 6 GPIOs in 8-pin package; including one output-only pin and one input-only pin
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins
- Package Options
  - MC9RS08KB12/MC9RS08KB8/MC9RS08KB4
    - 24-pin QFN, 20-pin SOIC, 16-pin SOIC NB or TSSOP
  - MC9RS08KB2
    - 8-pin SOIC or DFN

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	4/13/2009	Updated on shared review comments, added package information.
2	5/22/2009	Completed most of the TBDs, corrected the block diagram.
3	8/31/2009	Completed all the TBDs. Changed V_{LVD} and added R_{PD} in the Table 7. Changed SI_{DD}, ADC adder from stop, RTI adder from stop with 1 kHz clock source enabled and LVI adder from stop at 5 V in the Table 8.
4	6/23/2011	Split the 10-Bit ADC Characteristics to Table 15 and Table 16 for the V_{DDAD} ranges. Corrected the note 4 in the Table 8.
5	1/30/2012	Added 24-pin QFN package.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9RS08KB12RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

Table 1. Pin Availability by Package Pin-Count

Pin Number				<-- Lowest **Priority** --> Highest				
24	**20**	**16**	**8**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	3	3	3					V_{DD}
2	—	—	—	NC				
3	4	4	4					V_{SS}
4	5	5	—	PTB7	SCL[1]			EXTAL
5	6	6	—	PTB6	SDA[1]			XTAL
6	7	7	—	PTB5	TPMCH1[2]			
7	8	8	—	PTB4	TPMCH0[2]			
8	9	—	—	PTC3			ADP11	
9	10	—	—	PTC2			ADP10	
10	11	—	—	PTC1			ADP9	
11	12	—	—	PTC0			ADP8	
12	13	9	—	PTB3	KBIP7		ADP7	
13	14	10	—	PTB2	KBIP6		ADP6	
14	15	11	—	PTB1	KBIP5	TxD[3]	ADP5	
15	16	12	—	PTB0	KBIP4	RxD[3]	ADP4	
16	17	13	5	PTA3	KBIP3	SCL[1]	TxD[3]	ADP3
17	18	14	6	PTA2	KBIP2	SDA[1]	RxD[3]	ADP2
18	19	15	7	PTA1	KBIP1	TPMCH1[2]	ADP1	ACMP–
19	20	16	8	PTA0	KBIP0	TPMCH0[2]	ADP0	ACMP+
20	—	—	—	NC				
21	—	—	—	NC				
22	—	—	—	NC				
23	1	1	1	PTA5		TCLK	$\overline{\text{RESET}}$	V_{PP}
24	2	2	2	PTA4	ACMPO	BKGD	MS	

1 IIC pins can be remapped to PTB6 and PTB7, default reset location is PTA2 and PTA3. It can be configured only once.

2 TPM pins can be remapped to PTB4 and PTB5, default reset location is PTA0 and PTA1.

3 SCI pins can be remapped to PTA2 and PTA3, default reset location is PTB0 and PTB1. It can be configured only once.

unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_{JMAX}	150	°C
Thermal resistance 24-pin QFN	θ_{JA}	113	°C/W
Thermal resistance 20-pin SOIC	θ_{JA}	83	°C/W
Thermal resistance 16-pin SOIC NB	θ_{JA}	103	°C/W
Thermal resistance 16-pin TSSOP	θ_{JA}	29	°C/W
Thermal resistance 8-pin SOIC	θ_{JA}	150	°C/W
Thermal resistance 8-pin DFN	θ_{JA}	110	°C/W

The average chip-junction temperature (TJ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C /W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts chip internal power

$P_{I/O}$ = Power dissipation on input and output pins user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between PD and TJ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (PD)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

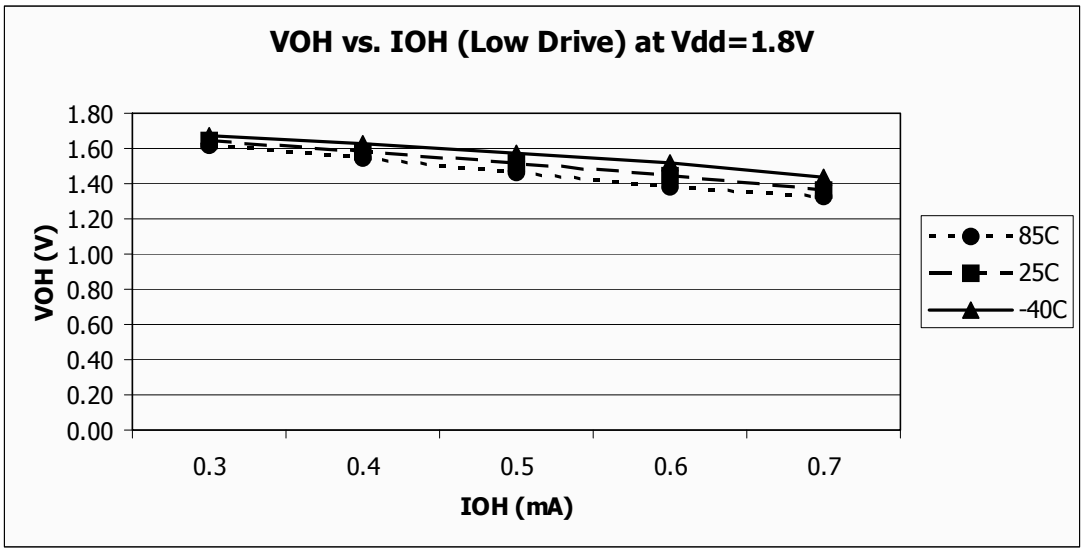


Figure 11. Typical V_{OH} vs. I_{OH}
V_{DD} = 1.8 V (Low Drive)

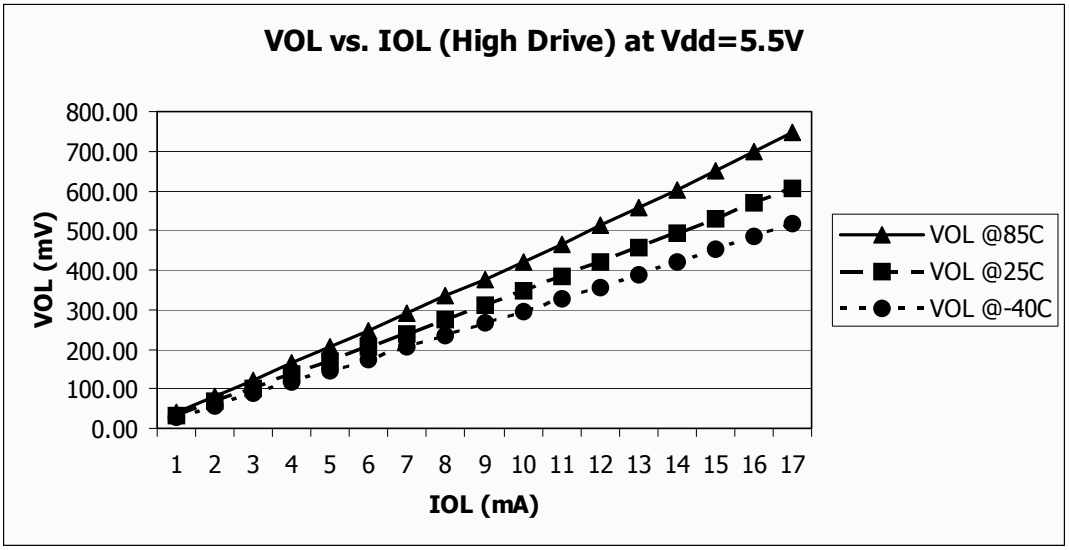


Figure 12. Typical V_{OL} vs. I_{OL}
V_{DD} = 5.5 V (High Drive)

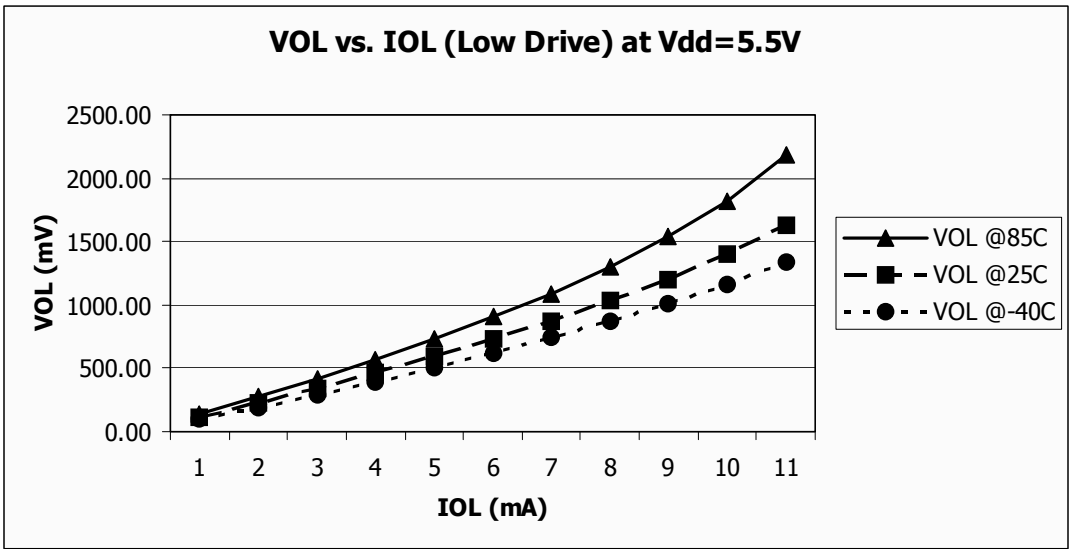


Figure 13. Typical V_{OL} vs. I_{OL}
V_{DD} = 5.5 V (Low Drive)

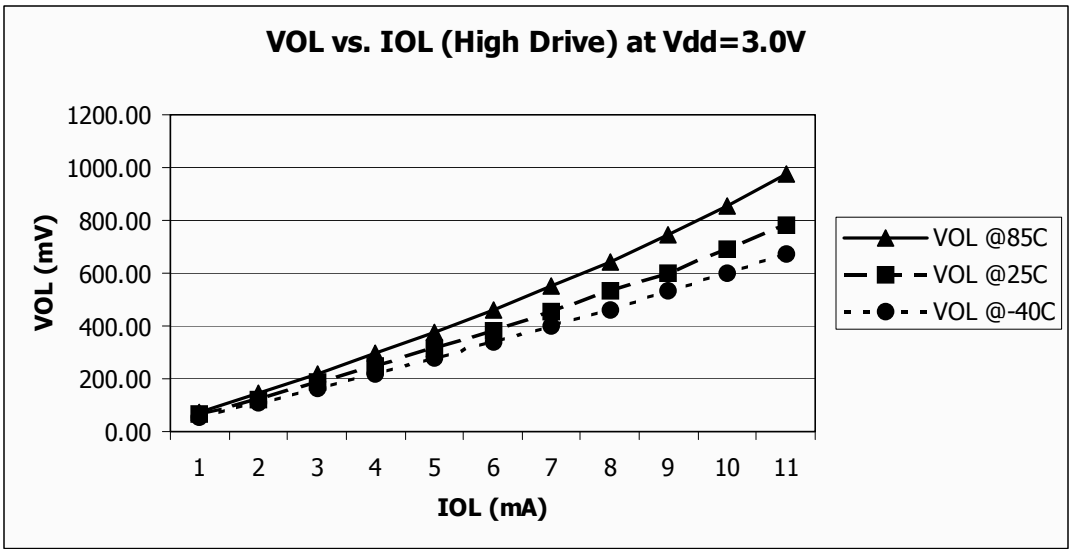


Figure 14. Typical V_{OL} vs. I_{OL}
V_{DD} = 3.0 V (High Drive)

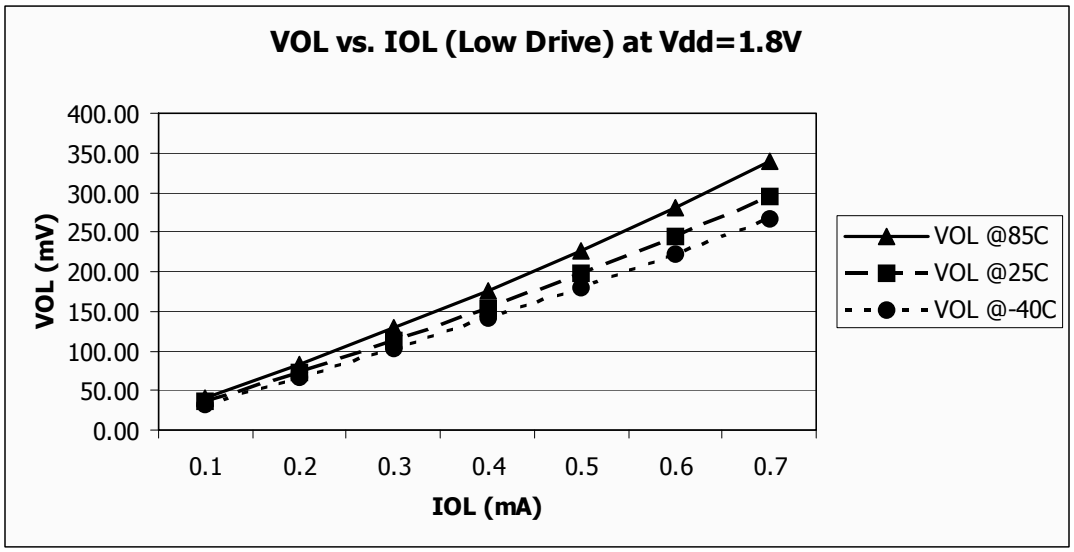


Figure 17. Typical V_{OL} vs. I_{OL}
V_{DD} = 1.8 V (Low Drive)

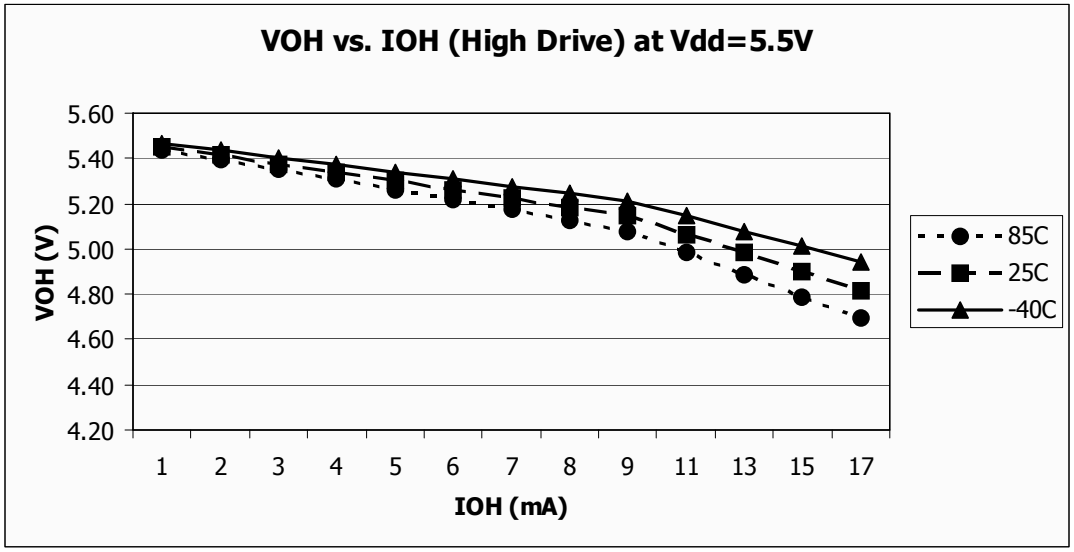


Figure 18. Typical I_{OH} vs. V_{DD}–V_{OH}
V_{DD} = 5.5 V (High Drive)

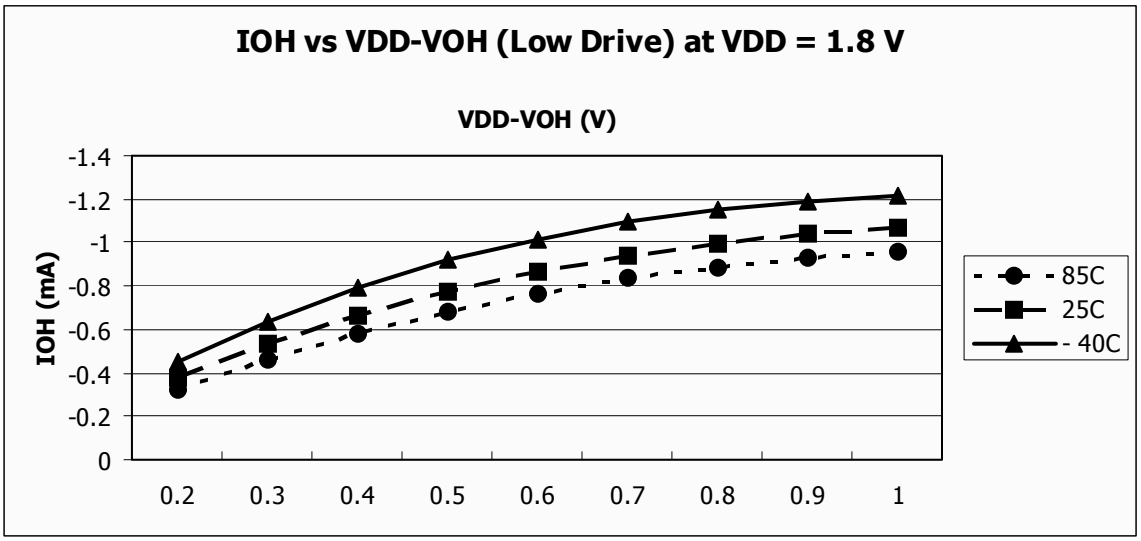


Figure 23. Typical I_{OH} vs. V_{DD}–V_{OH}
V_{DD} = 1.8 V (Low Drive)

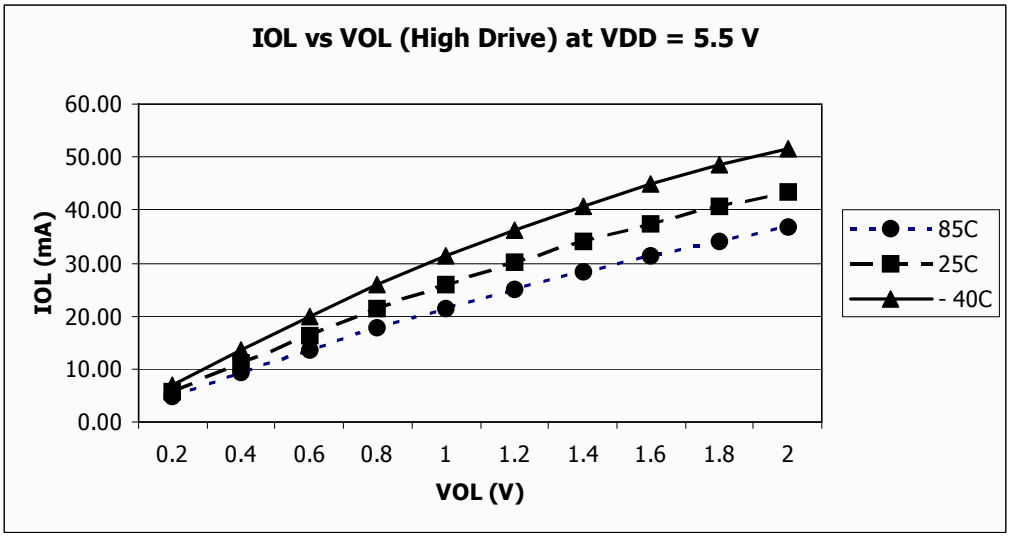


Figure 24. Typical I_{OL} vs. V_{OL}
V_{DD} = 5.5 V (High Drive)

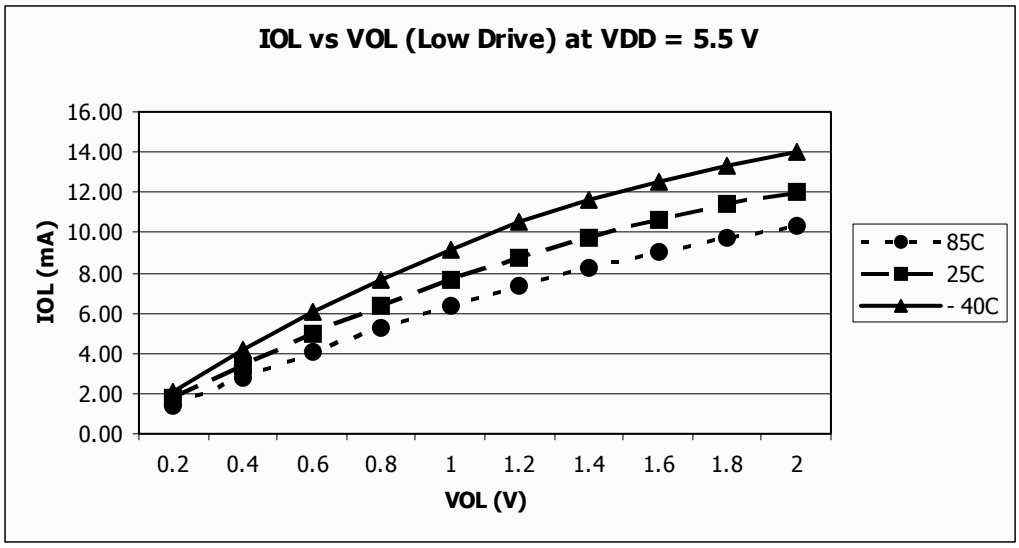


Figure 25. Typical I_{OL} vs. V_{OL}
V_{DD} = 5.5 V (Low Drive)

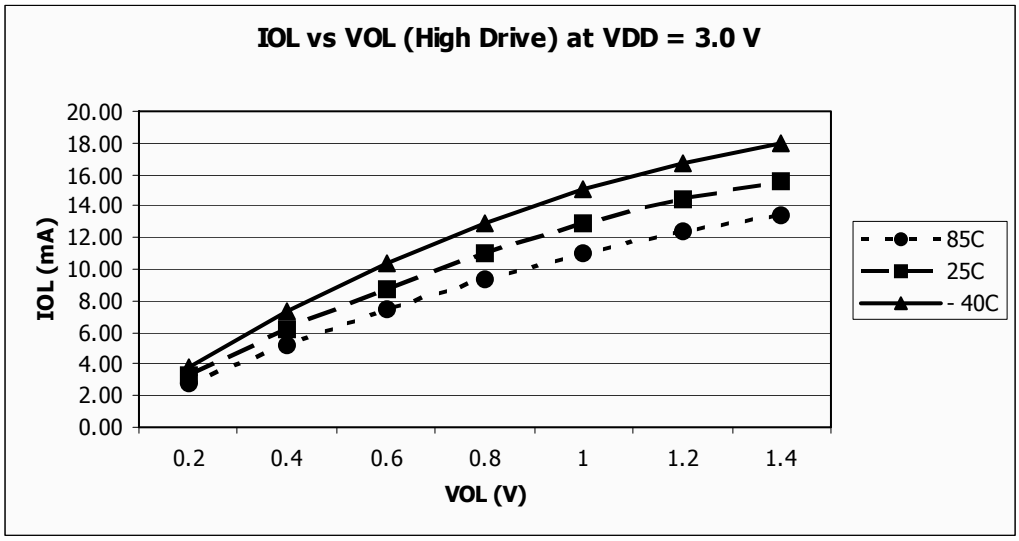


Figure 26. Typical I_{OL} vs. V_{OL}
V_{DD} = 3 V (High Drive)

Table 8. Supply Current Characteristics (continued)

N	C	Parameter	Symbol	V_{DD} (V)	Typical	Max[1]	Temp. (°C)	Unit
7	C	Wait mode supply current[3] measured at (f_{Bus} = 2.00 MHz)	WI_{DD2}	5	841.13 859.98 873.69	—	–40 25 85	µA
8	T			3	840.21 850.60 846.67	—	–40 25 85	
9	T			1.80	630.64 635.10 643.67	—	–40 25 85	
10	C	Wait mode supply current[3] measured at (f_{Bus} = 1.00 MHz)	WI_{DD1}	5	667.86 683.38 688.02	—	–40 25 85	µA
11	T			3	666.34 672.79 669.15	—	–40 25 85	
12	T			1.80	505.39 509.28 502.52	—	–40 25 85	
13	P	Stop mode supply current	SI_{DD}	5	1.15 1.40 7.67	11	–40 25 85	µA
14	C			3	1.05 1.26 4.52	—	–40 25 85	
15	C			1.80	0.39 0.56 4.21	—	–40 25 85	
16	C	ADC adder from stop[3]	—	5	128.86 140.44 154.97	—	–40 25 85	µA
17	T			3	102.98 111.71 118.33	—	–40 25 85	
18	T			1.80	54.77 66.33 74.42	—	–40 25 85	
19	C	ACMP adder from stop (ACME = 1)	—	5	14.43 15.96 16.77	—	–40 25 85	µA
20	T			3	14.37 14.72 14.45	—	–40 25 85	
21	T			1.80	13.05 14.02 12.92	—	–40 25 85	

Table 8. Supply Current Characteristics (continued)

N	C	Parameter	Symbol	V_{DD} (V)	Typical	Max[1]	Temp. (°C)	Unit
22	C	RTI adder from stop with 1 kHz clock source enabled[4]	—	5	0.10 0.10 0.17	—	–40 25 85	µA
23	T			3	0.02 0.06 0.02	—	–40 25 85	
24	T			1.80	0.40 0.45 0.20	—	–40 25 85	
25	T	RTI adder from stop with 32.768KHz external clock source reference enabled	—	5	0.70 1.08 1.94	—	–40 25 85	µA
26	T			3	0.56 0.56 0.62	—	–40 25 85	
27	T			1.80	0.70 0.86 0.50	—	–40 25 85	
28	C	LVI adder from stop (LVDE = 1 and LVDSE = 1)	—	5	58.93 68.27 76.60	—	–40 25 85	µA
29	T			3	58.89 61.98 63.45	—	–40 25 85	
30	T			1.80	52.84 54.52 52.49	—	–40 25 85	

1 Maximum value is measured at the nominal V_{DD} voltage times 10% tolerance. Values given here are preliminary estimates prior to completing characterization.

2 Not include any DC loads on port pins.

3 Required asynchronous ADC clock and LVD to be enabled.

4 Most customers are expected to find that auto-wakeup from stop can be used instead of the higher current wait mode. Wait mode typical is 672.79 µA at 3 V and 509.28 µA at 1.8 V with f_{Bus} = 1 MHz.

3.8 External Oscillator (XOSC) Characteristics

Table 9. Oscillator Electrical Specifications (Temperature Range = –40 to 85°C Ambient)

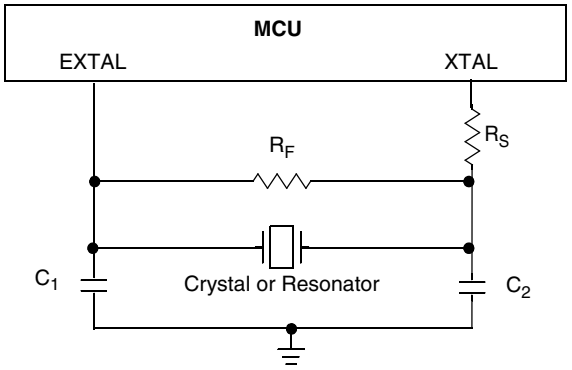
Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode[2] High range (RANGE = 1, HGO = 1) FBELP mode High range (RANGE = 1, HGO = 0) FBELP mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1, C_2	See crystal or resonator manufacturer's recommendation.			
3	D	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F	 — —	 10 1	 — —	MΩ
4	D	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time[3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[4]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 200 400 5 20	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode[2] FBELP mode	f_{extal}	0.03125 0	— —	5 40	MHz

1 Typical data was characterized at 5.0 V, 25 °C or is recommended value.

2 The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

4 4 MHz crystal.



3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.9.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

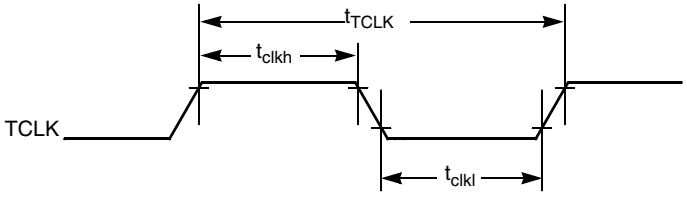


Figure 32. Timer External Clock

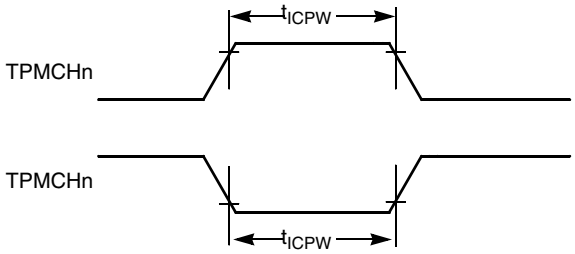


Figure 33. Timer Input Capture Pulse

3.10 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.80	—	5.5	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	µA
3	D	Analog input voltage[1]	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4	C	Analog input offset voltage[1]	V_{AIO}	—	20	40	mV
5	C	Analog Comparator hysteresis[1]	V_H	3.0	9.0	15.0	mV
6	C	Analog source impedance[1]	R_{AS}	—	—	10	kΩ
7	P	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
8	C	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	µs

Table 12. Analog Comparator Electrical Specifications (continued)

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
9	P	Analog Comparator bandgap reference voltage	V_{BG}	1.1	1.208	1.3	V

1 These data are characterized but not production tested.

3.11 Internal Clock Source Characteristics

Table 13. Internal Clock Source Specifications

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	C	Average internal reference frequency — untrimmed	f_{int_ut}	25	31.25	41.66	kHz
2	P	Average internal reference frequency — trimmed	f_{int_t}	31.25	32.768	39.0625	kHz
3	C	DCO output frequency range — untrimmed	f_{dco_ut}	12.8	16	21.33	MHz
4	P	DCO output frequency range — trimmed	f_{dco_t}	16	16.77	20	MHz
5	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco\_res\_t}$	—	—	0.2	$\%f_{dco}$
6	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	—	2	$\%f_{dco}$
7	C	FLL acquisition time[2,3]	$t_{acquire}$	—	—	1	ms
8	C	Stop recovery time (FLL wakeup to previous acquired frequency) IREFSTEN = 0 IREFSTEN = 1	t_wakeup	—	 100 86	—	µs

1 Data in typical column was characterized at 3.0 V and 5.0 V, 25 °C or is typical recommended value.

2 This parameter is characterized and not tested on each device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBILP) to FLL enabled (FEI, FBI).

3.12 ADC Characteristics

Table 14. 10-Bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	1.8	—	5.5	V	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	
Analog source resistance	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ	External to MCU
	8-bit mode (all valid f_{ADCK})		—	—	10		

Table 14. 10-Bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
ADC conversion clock Freq.	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

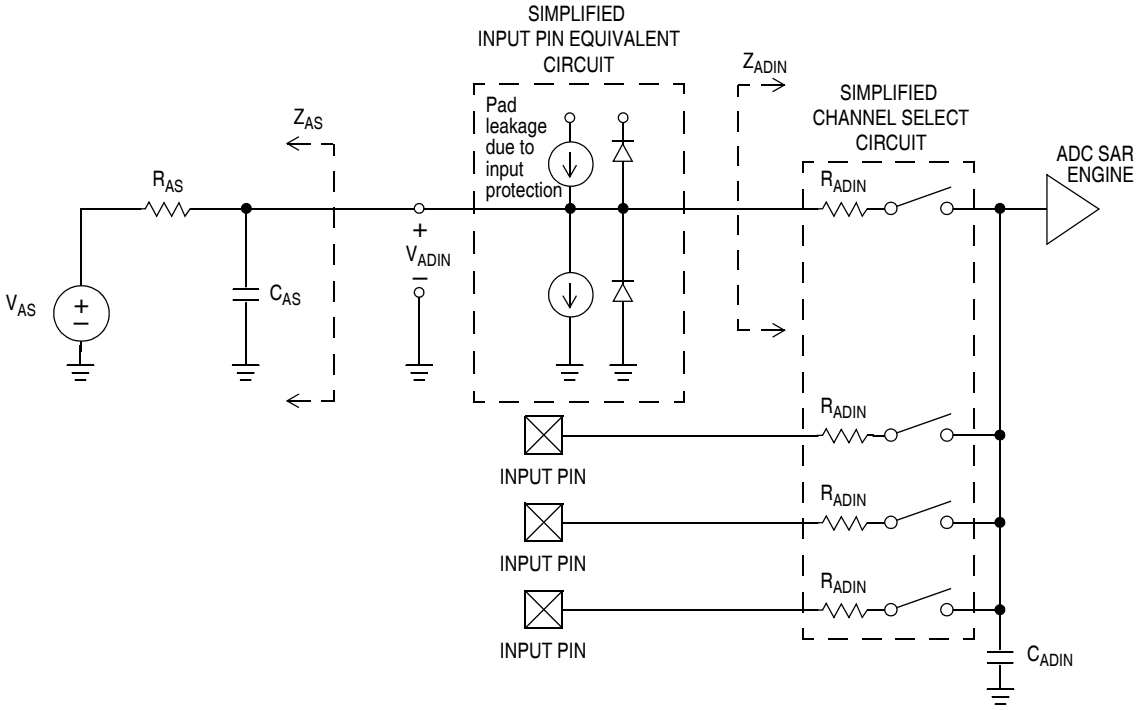


Figure 34. ADC Input Impedance Equivalency Diagram

Table 15. 10-Bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}, 2.7 V < V_{DDAD} < 5.5 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	133	—	µA	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	218	—	µA	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	327	—	µA	

Table 15. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 2.7 V < V_{DDAD} < 5.5 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
C	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	0.582	1	mA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	E_{TUE}	—	±1.5	±3.5	LSB[2]	Includes quantization
		8-bit mode		—	±0.7	±1.5		
T	Differential Non-Linearity	10-bit mode	DNL	—	±0.5	±1.0	LSB[2]	
		8-bit mode		—	±0.3	±0.5		
		Monotonicity and No-Missing-Codes guaranteed						
C	Integral Non-Linearity	10-bit mode	INL	—	±0.5	±1.0	LSB[2]	
		8-bit mode		—	±0.3	±0.5		
P	Zero-Scale Error	10-bit mode	E_{ZS}	—	±1.5	±2.5	LSB[2]	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	±0.5	±0.7		
P	Full-Scale Error	10-bit mode	E_{FS}	—	±1	±1.5	LSB[2]	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	±0.5	±0.5		
D	Quantization Error	10-bit mode	E_Q	—	—	±0.5	LSB[2]	
		8-bit mode		—	—	±0.5		
D	Input Leakage Error	10-bit mode	E_{IL}	—	±0.2	±2.5	LSB[2]	Pad leakage[2] * R_{AS}
		8-bit mode		—	±0.1	±1		

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 Based on input pad leakage current. Refer to pad electricals.

Table 16. 10-Bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}, 1.8 V < V_{DDAD} < 2.7 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
D	Input Leakage Error	10-bit mode	E_{IL}	—	—	—	LSB[2]	Pad leakage[2] * R_{AS}
		8-bit mode		—	±0.1	±1		

1 Typical values assume V_{DDAD} = 1.8 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

Table 17. Flash Characteristics

No.	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	D	Supply voltage for program/erase	V_{DD}	2.7	—	5.5	V
2	D	Program/Erase voltage	V_{PP}	11.8	12	12.2	V
3	C	V_{PP} current Program Mass erase	 I_{VPP_prog} I_{VPP_erase}	 — —	 — —	 200 100	 µA µA
4	D	Supply voltage for read operation 0 < f_{Bus} < 10 MHz	V_{Read}	1.8	—	5.5	V
5	P	Byte program time	t_{prog}	20	—	40	µs
6	P	Mass erase time	t_{me}	500	—	—	ms
7	C	Cumulative program HV time[2]	t_{hv}	—	—	8	ms
8	C	Total cumulative HV time (total of t_{me} & t_{hv} applied to device)	t_{hv_total}	—	—	2	hours
9	D	HVEN to program setup time	t_{pgs}	10	—	—	µs
10	D	PGM/MASS to HVEN setup time	t_{nvs}	5	—	—	µs
11	D	HVEN hold time for PGM	t_{nvh}	5	—	—	µs
12	D	HVEN hold time for MASS	t_{nvh1}	100	—	—	µs
13	D	V_{PP} to PGM/MASS setup time	t_{vps}	20	—	—	ns
14	D	HVEN to V_{PP} hold time	t_{vph}	20	—	—	ns
15	D	V_{PP} rise time[3]	t_{vrs}	200	—	—	ns
16	D	Recovery time	t_{rcv}	1	—	—	µs
17	D	Program/erase endurance T_L to T_H = –40 °C to 85 °C	—	1000	—	—	cycles
18	C	Data retention	t_{D_ret}	15	—	—	years

1 Typicals are measured at 25 °C.

2 t_{hv} is the cumulative high voltage programming time to the same row before next erase. Same address can not be programmed more than twice before next erase.

3 Fast V_{PP} rise time may potentially trigger the ESD protection structure, which may result in over current flowing into the pad and cause permanent damage to the pad. External filtering for the V_{PP} power source is recommended. An example V_{PP} filter is shown in Figure 35.

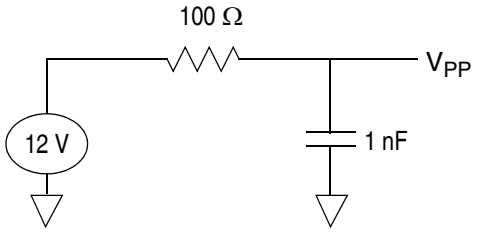
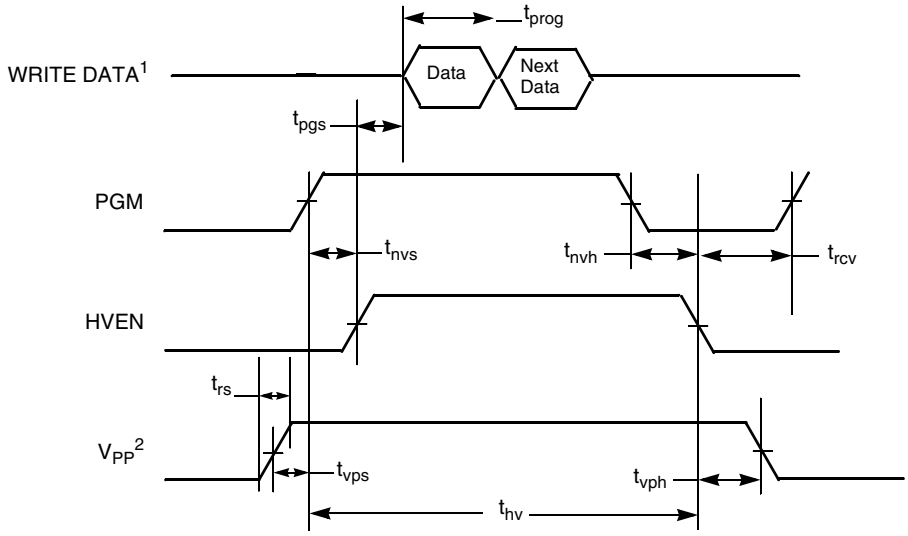


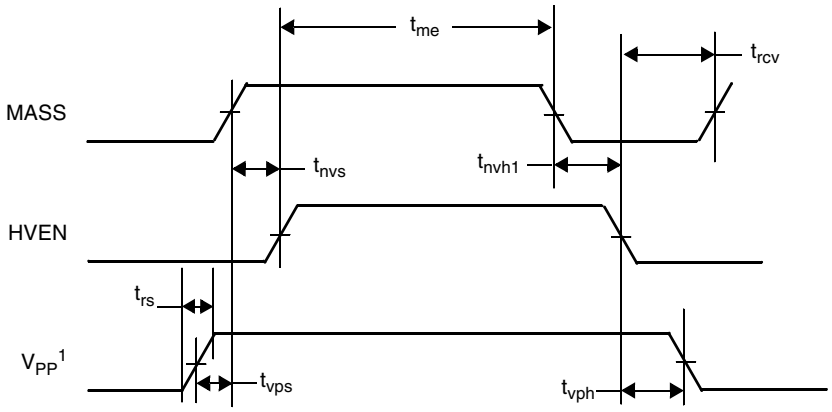
Figure 35. Example V_{PP} Filtering



1 Next Data applies if programming multiple bytes in a single row, refer to *MC9RS08KB12 Series Reference Manual*.

2 V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 36. Flash Program Timing



1 V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 37. Flash Mass Erase Timing

3.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).