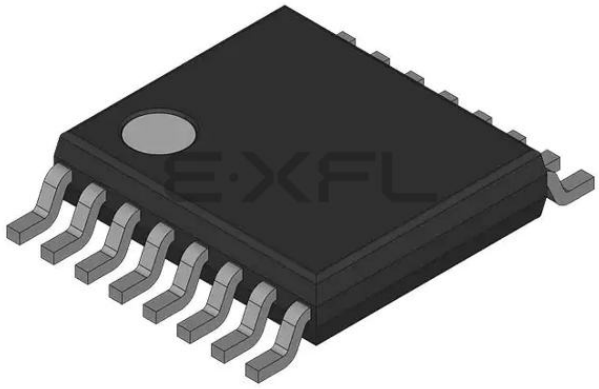


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

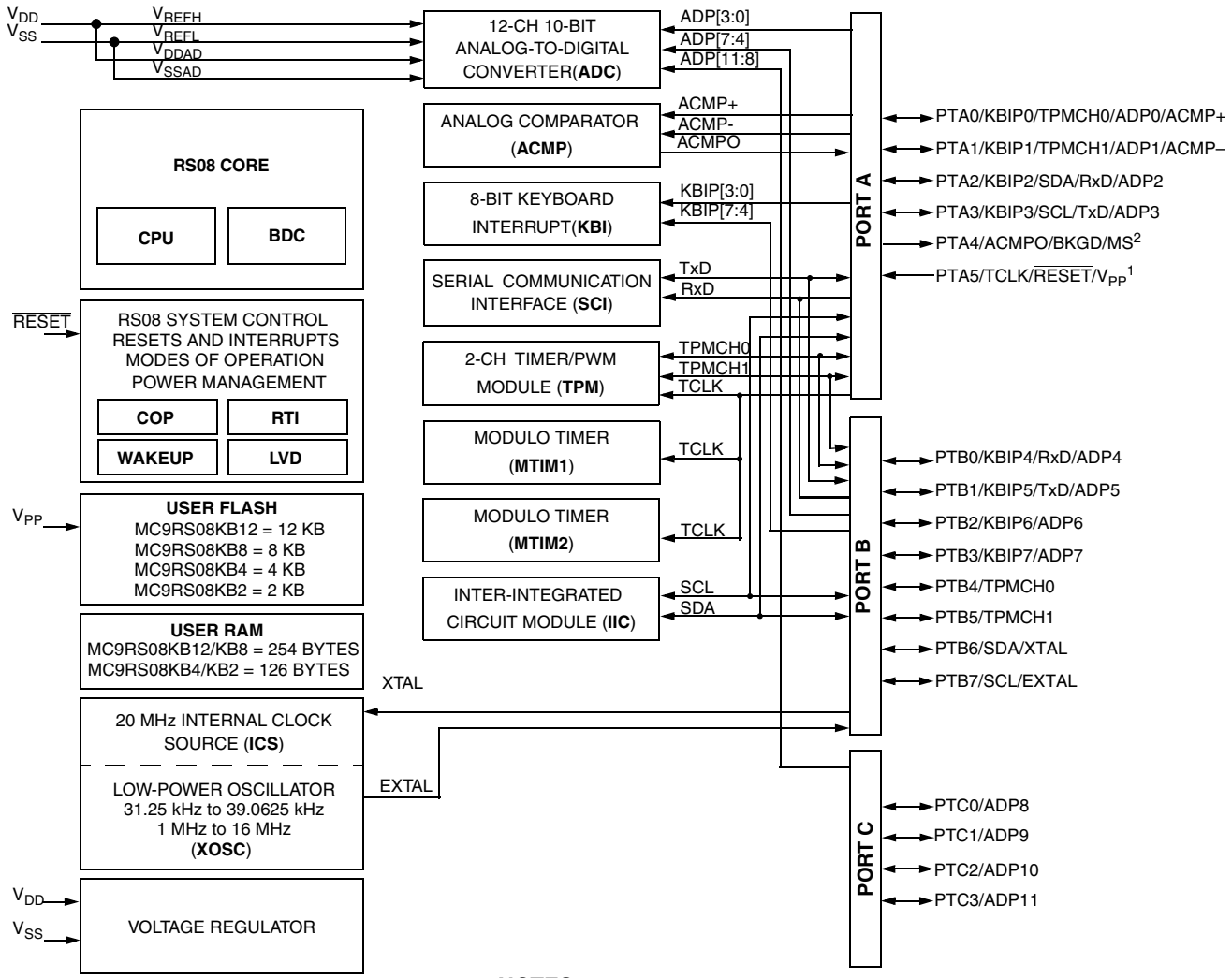
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	254 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9rs08kb8ctg

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9RS08KB12 MCU.



NOTES:

1. PTA5/TCLK/$\overline{\text{RESET}}$/V_{PP} is an input-only pin when used as port pin
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin

Figure 1. MC9RS08KB12 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08KB12 series.

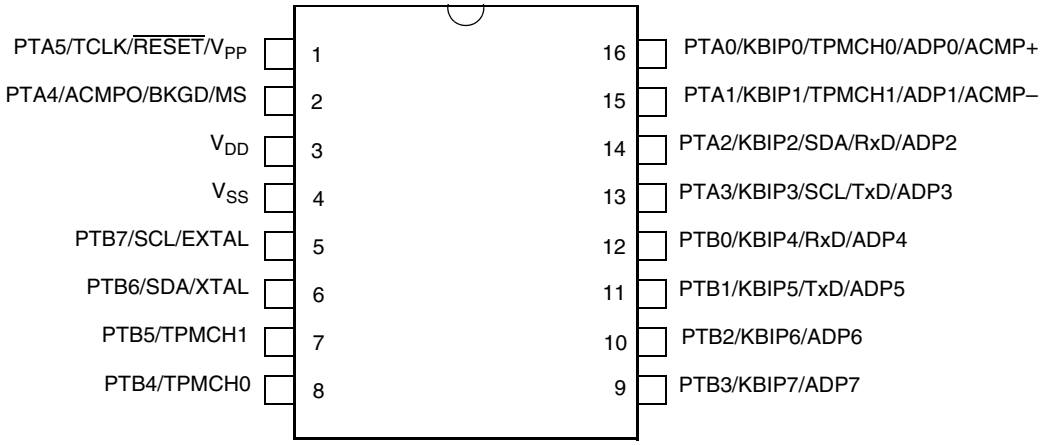


Figure 4. MC9RS08KB12 Series 16-Pin SOIC NB/TSSOP Package

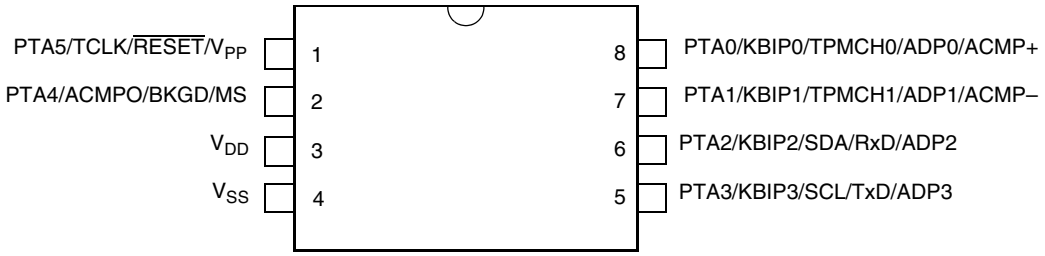


Figure 5. MC9RS08KB12 Series 8-Pin SOIC/DFN Package

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9RS08KB12 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.

During the device qualification ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-Up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	1	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient)

No.	C	Parameter	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage (run, wait and stop modes.) 0 < f_{Bus} <10 MHz	V_{DD}	1.8	—	5.5	V
2	C	Minimum RAM retention supply voltage applied to V_{DD}	V_{RAM}	0.8[1]	—	—	V
3	P	Low-voltage detection threshold (V_{DD} falling) (V_{DD} rising)	V_{LVD}	1.80 1.88	1.86 1.94	1.95 2.05	V
4	C	Power on RESET (POR) voltage	V_{POR}[1]	0.9	—	1.7	V
5	C	Input high voltage (V_{DD} > 2.3V) (all digital inputs)	V_{IH}	0.70 × V_{DD}	—	—	V
6	C	Input high voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IH}	0.85 × V_{DD}	—	—	V
7	C	Input low voltage (V_{DD} > 2.3 V) (all digital inputs)	V_{IL}	—	—	0.30 × V_{DD}	V
8	C	Input low voltage (1.8 V ≤ V_{DD} ≤ 2.3 V) (all digital inputs)	V_{IL}	—	—	0.30 × V_{DD}	V
9	C	Input hysteresis (all digital inputs)	V_{hys}[1]	0.06 × V_{DD}	—	—	V
10	P	Input leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input only pins	|I_{In}|	—	0.025	1.0	µA
11	P	High impedance (off-state) leakage current (per pin) V_{In} = V_{DD} or V_{SS}, all input/output	|I_{OZ}|	—	0.025	1.0	µA
12	P	Internal pullup resistors[2](all port pins)	R_{PU}	20	45	65	kΩ
13	P	Internal pulldown resistors[2](all port pins)	R_{PD}	20	45	65	kΩ
14	C	Output high voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA 1.8 V, I_{Load} = 0.5 mA	V_{OH}	V_{DD} – 0.8	— — —	— — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 3 mA 1.8 V, I_{Load} = 2 mA		V_{DD} – 0.8	— — —	— — —	
15	C	Maximum total I_{OH} for all port pins	|I_{OHT}|	—	—	40	mA

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

No.	C	Parameter	Symbol	Min	Typical	Max	Unit
16	C	Output low voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA 1.8 V, I_{Load} = 0.5 mA	V_{OL}	— — —	— — —	0.8	V
		Output low voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 3 mA 1.8 V, I_{Load} = 2 mA		— — —	— — —	0.8	
17	C	Maximum total I_{OL} for all port pins	I_{OLT}	—	—	40	mA
18	C	DC injection current[3, 4, 5, 6] $V_{In} < V_{SS}$, $V_{In} > V_{DD}$ Single pin limit Total MCU limit, includes sum of all stressed pins		— —	— —	0.2 0.8	mA
19	C	Input capacitance (all non-supply pins)	C_{In}	—	—	7	pF

1 This parameter is characterized and not tested on each device.

2 Measurement condition for pull resistors: $V_{In} = V_{SS}$ for pullup and $V_{In} = V_{DD}$ for pulldown.

3 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{RESET}/V_{PP}$ which is internally clamped to V_{SS} only.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 This parameter is characterized and not tested on each device.

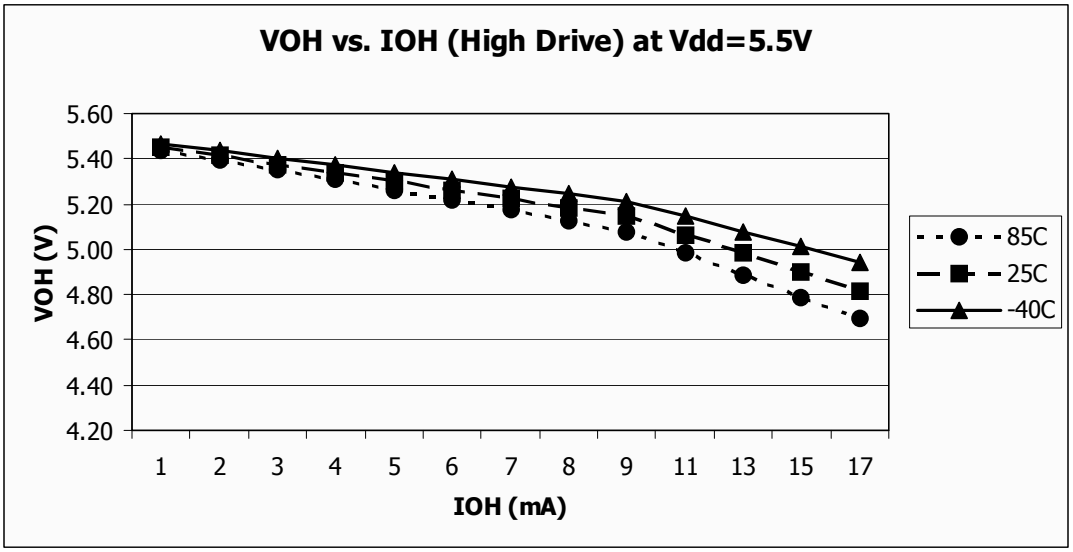


Figure 6. Typical V_{OH} vs. I_{OH}
V_{DD} = 5.5 V (High Drive)

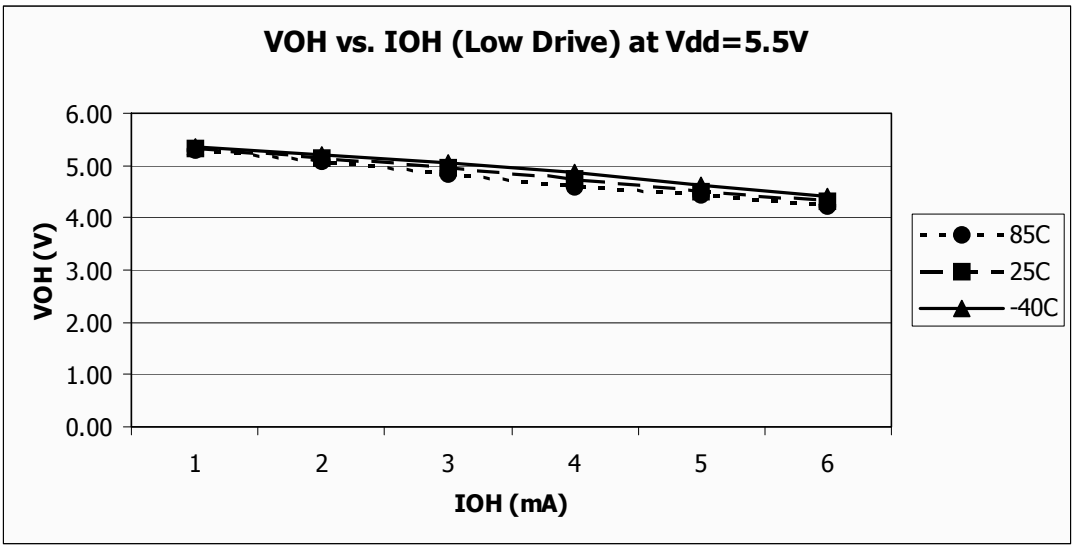


Figure 7. Typical V_{OH} vs. I_{OH}
V_{DD} = 5.5 V (Low Drive)

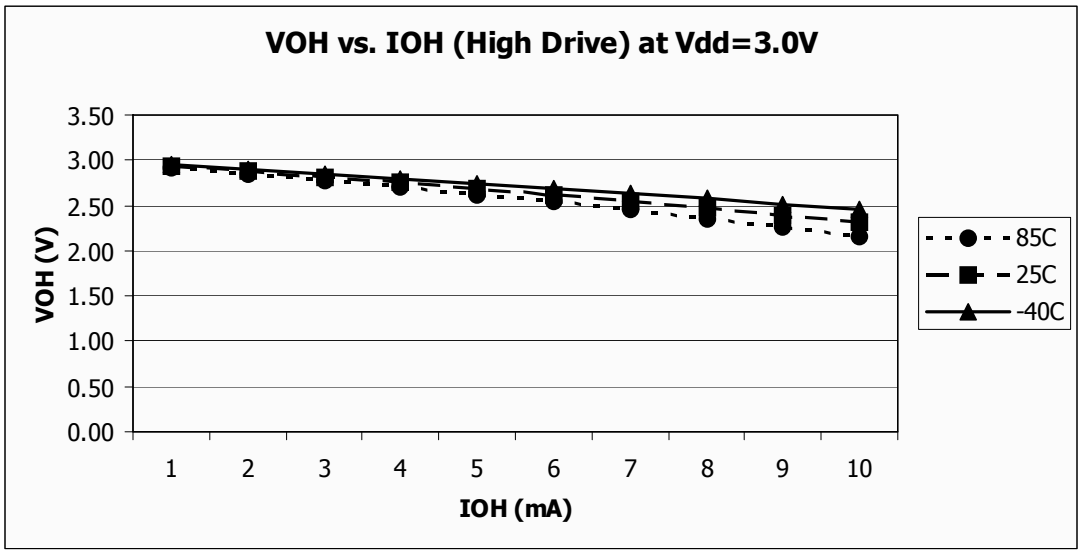


Figure 8. Typical V_{OH} vs. I_{OH}
V_{DD} = 3.0 V (High Drive)

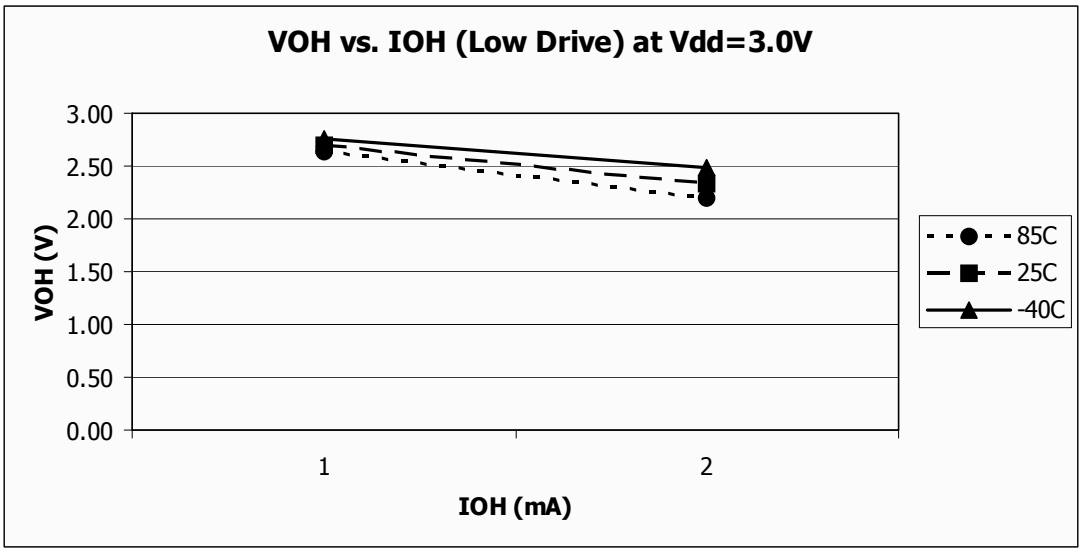


Figure 9. Typical V_{OH} vs. I_{OH}
V_{DD} = 3.0 V (Low Drive)

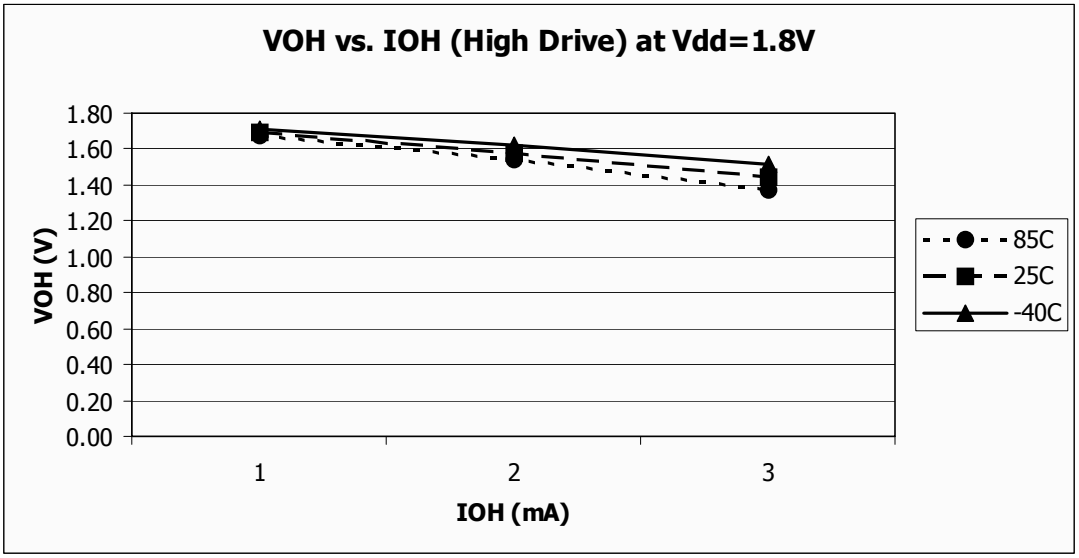


Figure 10. Typical V_{OH} vs. I_{OH}
V_{DD} = 1.8 V (High Drive)

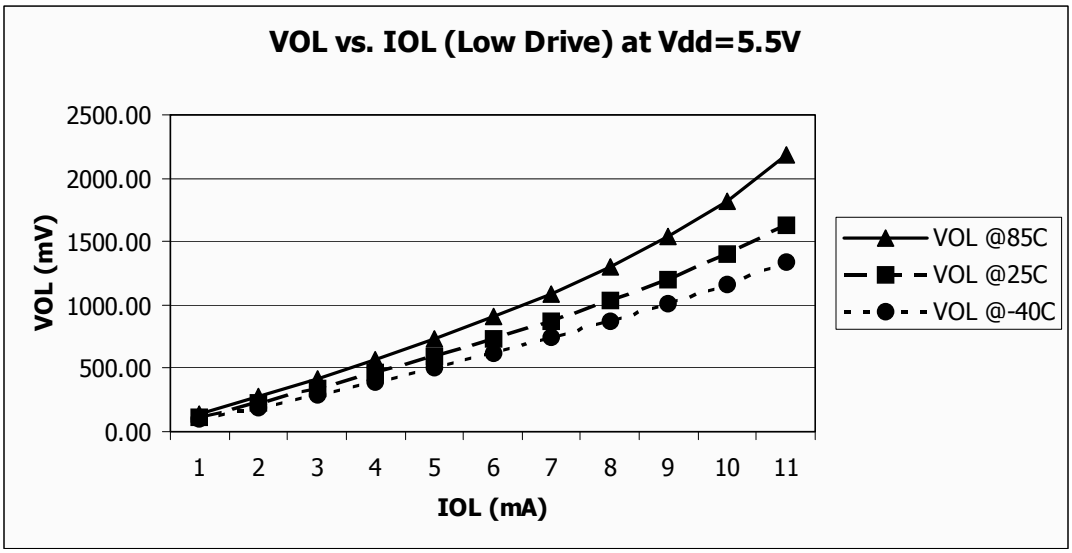


Figure 13. Typical V_{OL} vs. I_{OL}
V_{DD} = 5.5 V (Low Drive)

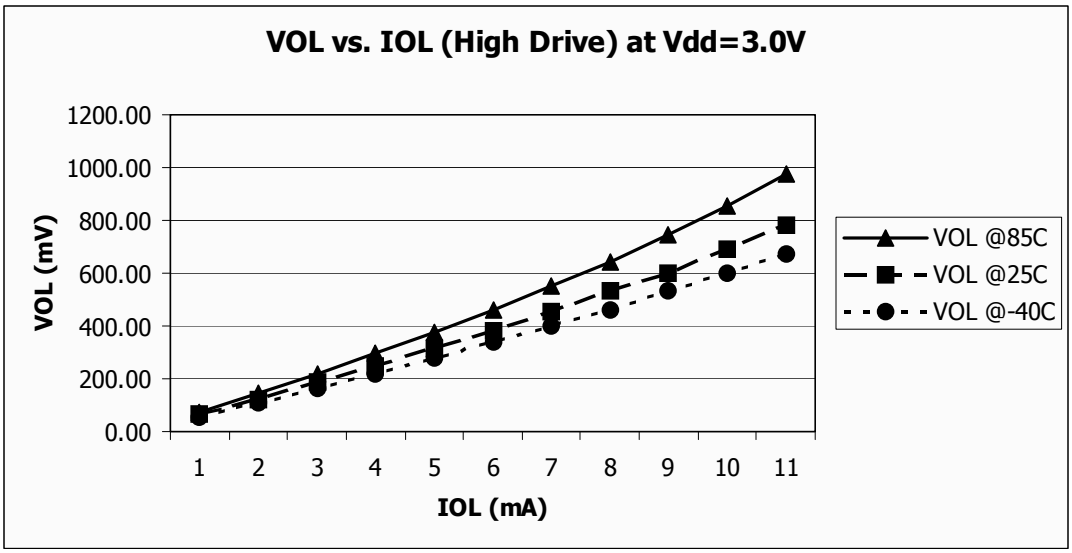


Figure 14. Typical V_{OL} vs. I_{OL}
V_{DD} = 3.0 V (High Drive)

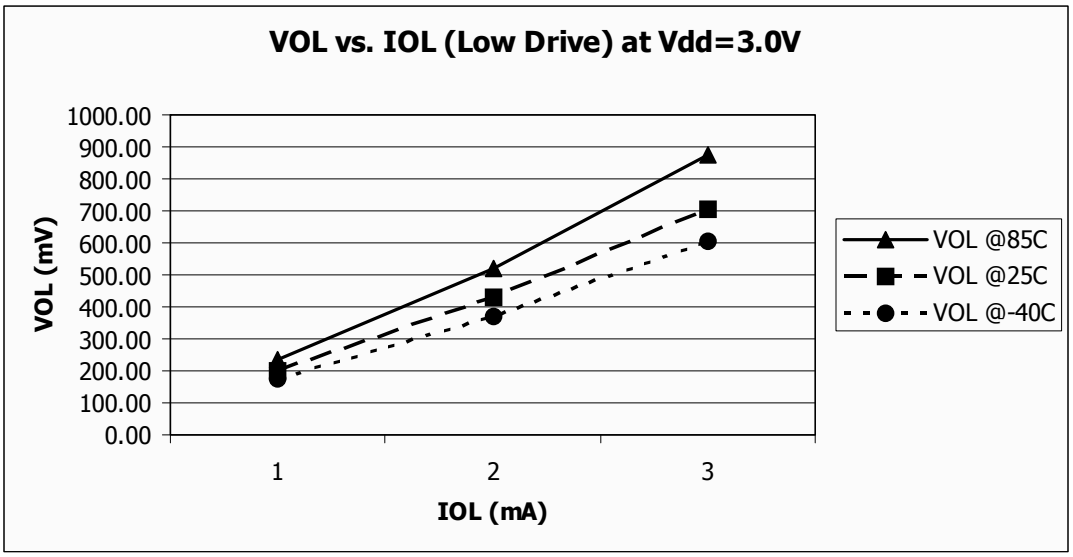


Figure 15. Typical V_{OL} vs. I_{OL}
V_{DD} = 3.0 V (Low Drive)

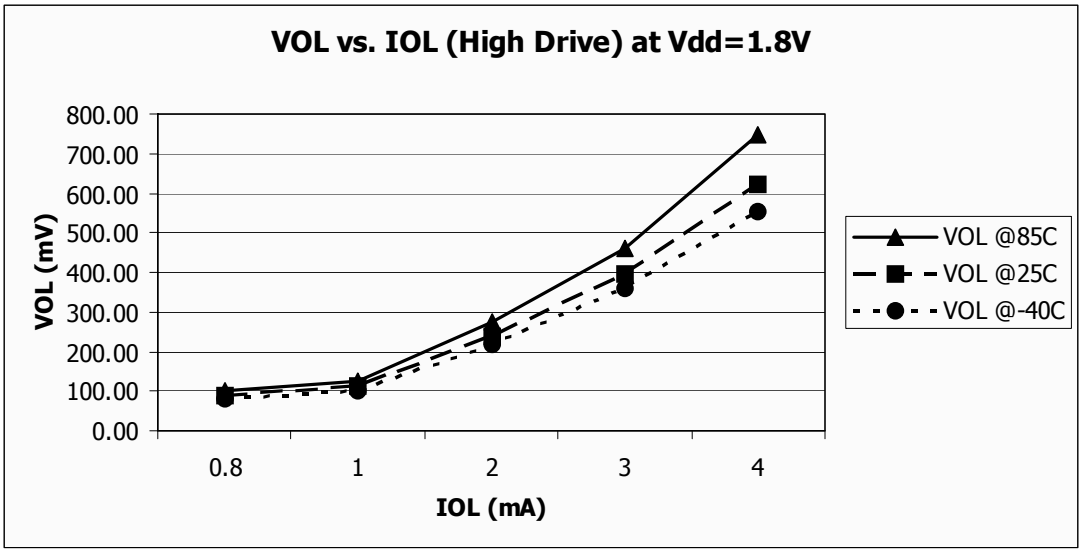


Figure 16. Typical V_{OL} vs. I_{OL}
V_{DD} = 1.8 V (High Drive)

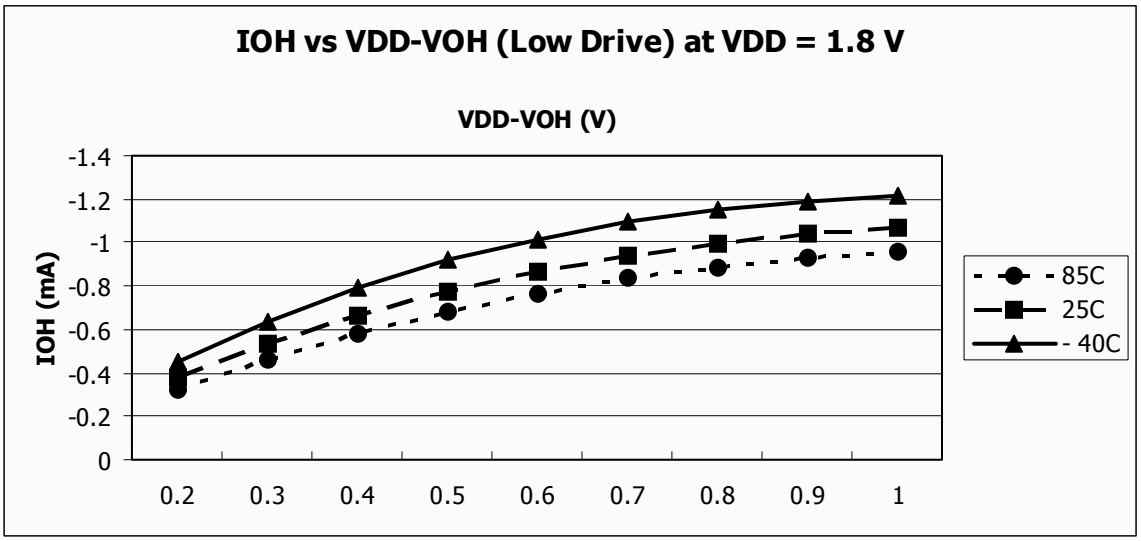


Figure 23. Typical I_{OH} vs. V_{DD}–V_{OH}
V_{DD} = 1.8 V (Low Drive)

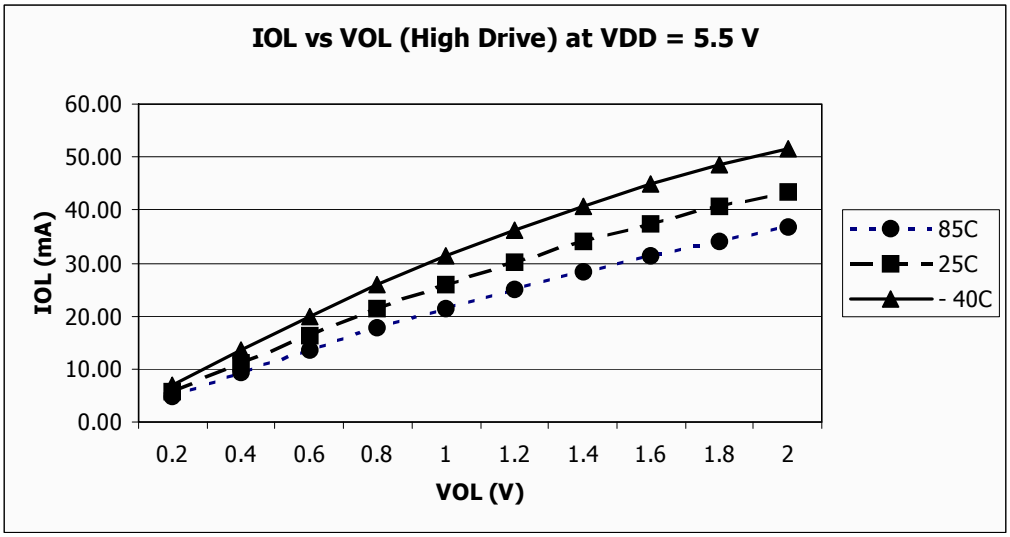


Figure 24. Typical I_{OL} vs. V_{OL}
V_{DD} = 5.5 V (High Drive)

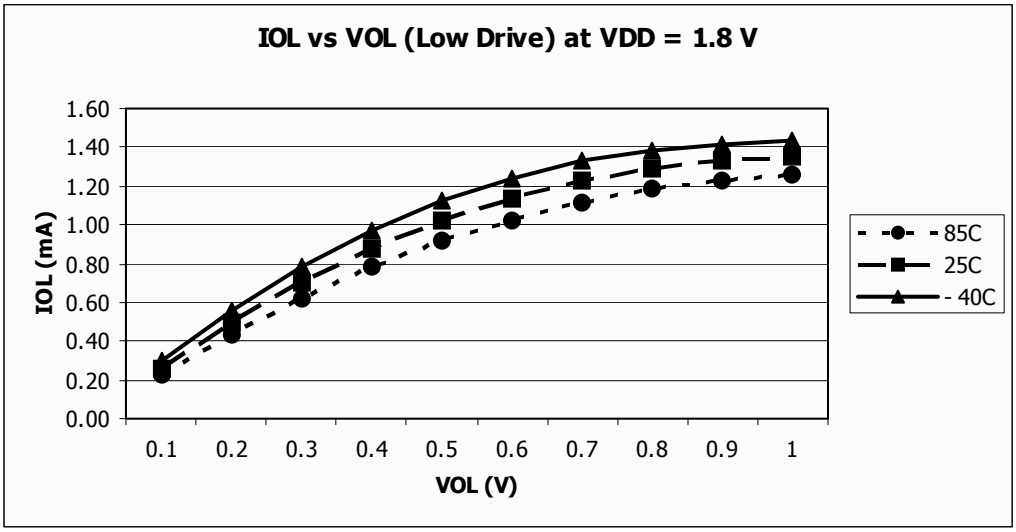


Figure 29. Typical I_{OL} vs. V_{OL} V_{DD} = 1.8 V (Low Drive)

3.7 Supply Current Characteristics

Table 8. Supply Current Characteristics

N	C	Parameter	Symbol	V_{DD} (V)	Typical	Max[1]	Temp. (°C)	Unit
1	P	Run supply current[2] measured at (f_{Bus} = 10 MHz)	RI_{DD10}	5	3.45 3.48 3.53	7	–40 25 85	mA
2	C			3	3.39 3.42 3.49	—	–40 25 85	
3	C			1.80	2.40 2.42 2.44	—	–40 25 85	
4	C	Run supply current[3] measured at (f_{Bus} = 1.25 MHz)	RI_{DD1}	5	0.93 0.96 0.99	—	–40 25 85	mA
5	T			3	0.91 0.92 0.92	—	–40 25 85	
6	T			1.80	0.66 0.67 0.68	—	–40 25 85	

Table 8. Supply Current Characteristics (continued)

N	C	Parameter	Symbol	V_{DD} (V)	Typical	Max[1]	Temp. (°C)	Unit
7	C	Wait mode supply current[3] measured at (f_{Bus} = 2.00 MHz)	WI_{DD2}	5	841.13 859.98 873.69	—	–40 25 85	µA
8	T			3	840.21 850.60 846.67	—	–40 25 85	
9	T			1.80	630.64 635.10 643.67	—	–40 25 85	
10	C	Wait mode supply current[3] measured at (f_{Bus} = 1.00 MHz)	WI_{DD1}	5	667.86 683.38 688.02	—	–40 25 85	µA
11	T			3	666.34 672.79 669.15	—	–40 25 85	
12	T			1.80	505.39 509.28 502.52	—	–40 25 85	
13	P	Stop mode supply current	SI_{DD}	5	1.15 1.40 7.67	11	–40 25 85	µA
14	C			3	1.05 1.26 4.52	—	–40 25 85	
15	C			1.80	0.39 0.56 4.21	—	–40 25 85	
16	C	ADC adder from stop[3]	—	5	128.86 140.44 154.97	—	–40 25 85	µA
17	T			3	102.98 111.71 118.33	—	–40 25 85	
18	T			1.80	54.77 66.33 74.42	—	–40 25 85	
19	C	ACMP adder from stop (ACME = 1)	—	5	14.43 15.96 16.77	—	–40 25 85	µA
20	T			3	14.37 14.72 14.45	—	–40 25 85	
21	T			1.80	13.05 14.02 12.92	—	–40 25 85	

Table 8. Supply Current Characteristics (continued)

N	C	Parameter	Symbol	V_{DD} (V)	Typical	Max[1]	Temp. (°C)	Unit
22	C	RTI adder from stop with 1 kHz clock source enabled[4]	—	5	0.10 0.10 0.17	—	–40 25 85	µA
23	T			3	0.02 0.06 0.02	—	–40 25 85	
24	T			1.80	0.40 0.45 0.20	—	–40 25 85	
25	T	RTI adder from stop with 32.768KHz external clock source reference enabled	—	5	0.70 1.08 1.94	—	–40 25 85	µA
26	T			3	0.56 0.56 0.62	—	–40 25 85	
27	T			1.80	0.70 0.86 0.50	—	–40 25 85	
28	C	LVI adder from stop (LVDE = 1 and LVDSE = 1)	—	5	58.93 68.27 76.60	—	–40 25 85	µA
29	T			3	58.89 61.98 63.45	—	–40 25 85	
30	T			1.80	52.84 54.52 52.49	—	–40 25 85	

1 Maximum value is measured at the nominal V_{DD} voltage times 10% tolerance. Values given here are preliminary estimates prior to completing characterization.

2 Not include any DC loads on port pins.

3 Required asynchronous ADC clock and LVD to be enabled.

4 Most customers are expected to find that auto-wakeup from stop can be used instead of the higher current wait mode. Wait mode typical is 672.79 µA at 3 V and 509.28 µA at 1.8 V with f_{Bus} = 1 MHz.

3.8 External Oscillator (XOSC) Characteristics

Table 9. Oscillator Electrical Specifications (Temperature Range = –40 to 85°C Ambient)

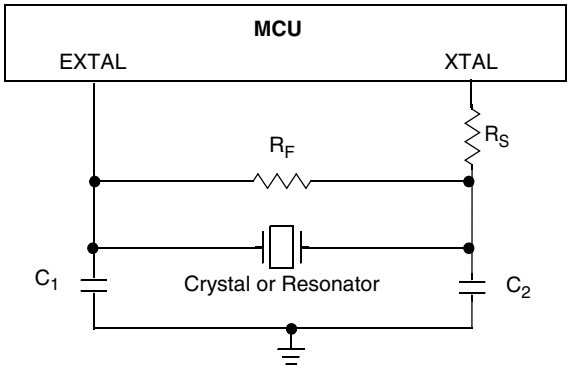
Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode[2] High range (RANGE = 1, HGO = 1) FBELP mode High range (RANGE = 1, HGO = 0) FBELP mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1, C_2	See crystal or resonator manufacturer's recommendation.			
3	D	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F	 — —	 10 1	 — —	MΩ
4	D	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time[3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[4]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 200 400 5 20	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode[2] FBELP mode	f_{extal}	0.03125 0	— —	5 40	MHz

1 Typical data was characterized at 5.0 V, 25 °C or is recommended value.

2 The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

4 4 MHz crystal.



3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.9.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

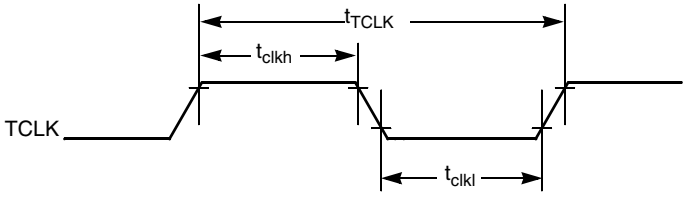


Figure 32. Timer External Clock

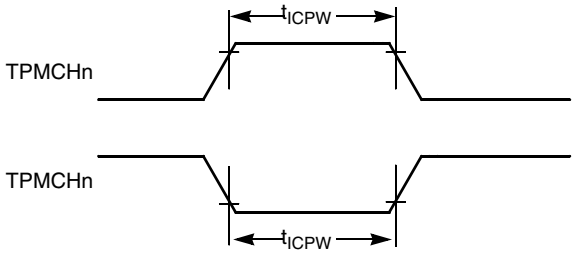


Figure 33. Timer Input Capture Pulse

3.10 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.80	—	5.5	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	µA
3	D	Analog input voltage[1]	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4	C	Analog input offset voltage[1]	V_{AIO}	—	20	40	mV
5	C	Analog Comparator hysteresis[1]	V_H	3.0	9.0	15.0	mV
6	C	Analog source impedance[1]	R_{AS}	—	—	10	kΩ
7	P	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
8	C	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	µs

Table 14. 10-Bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
ADC conversion clock Freq.	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

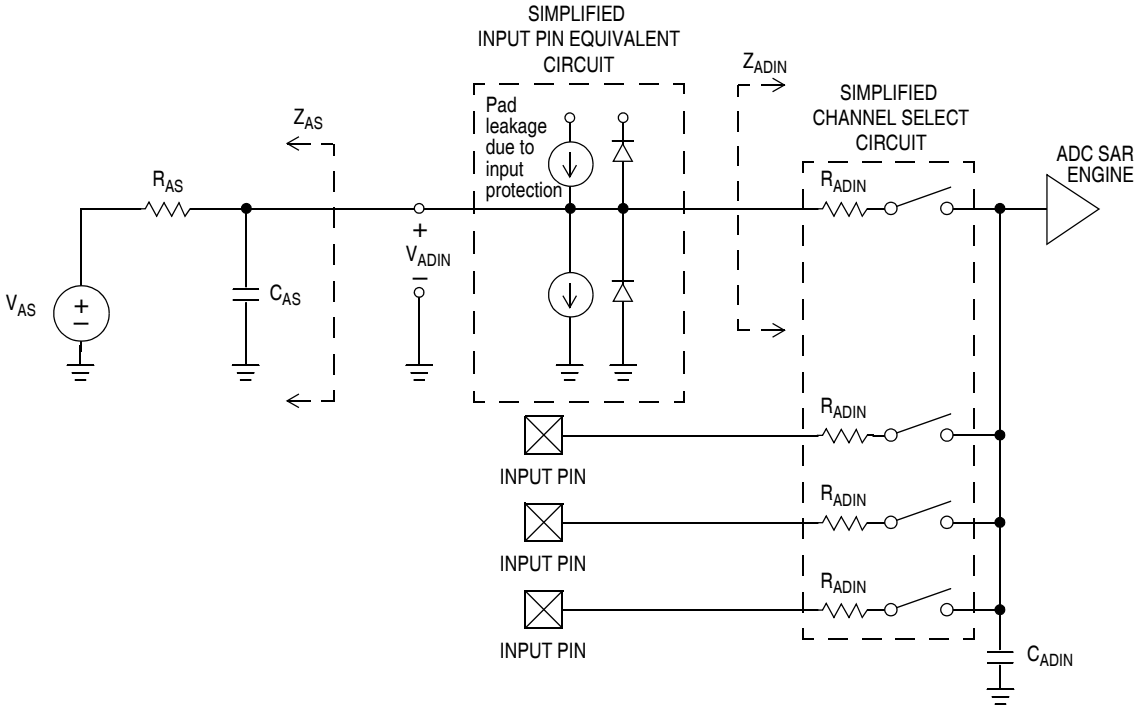


Figure 34. ADC Input Impedance Equivalency Diagram

Table 15. 10-Bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}, 2.7 V < V_{DDAD} < 5.5 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	133	—	µA	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	218	—	µA	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	327	—	µA	

Table 15. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 2.7 V < V_{DDAD} < 5.5 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
C	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	0.582	1	mA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	E_{TUE}	—	±1.5	±3.5	LSB[2]	Includes quantization
		8-bit mode		—	±0.7	±1.5		
T	Differential Non-Linearity	10-bit mode	DNL	—	±0.5	±1.0	LSB[2]	
		8-bit mode		—	±0.3	±0.5		
		Monotonicity and No-Missing-Codes guaranteed						
C	Integral Non-Linearity	10-bit mode	INL	—	±0.5	±1.0	LSB[2]	
		8-bit mode		—	±0.3	±0.5		
P	Zero-Scale Error	10-bit mode	E_{ZS}	—	±1.5	±2.5	LSB[2]	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	±0.5	±0.7		
P	Full-Scale Error	10-bit mode	E_{FS}	—	±1	±1.5	LSB[2]	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	±0.5	±0.5		
D	Quantization Error	10-bit mode	E_Q	—	—	±0.5	LSB[2]	
		8-bit mode		—	—	±0.5		
D	Input Leakage Error	10-bit mode	E_{IL}	—	±0.2	±2.5	LSB[2]	Pad leakage[2] * R_{AS}
		8-bit mode		—	±0.1	±1		

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 Based on input pad leakage current. Refer to pad electricals.

Table 16. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 1.8 V < V_{DDAD} < 2.7 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	8-bit mode	I_{DDAD}	—	88	—	μA	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	8-bit mode	I_{DDAD}	—	152	—	μA	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	8-bit mode	I_{DDAD}	—	214	—	μA	
T	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	8-bit mode	I_{DDAD}	—	390	—	μA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	E_{TUE}	—	—	—	LSB[2]	Includes quantization
		8-bit mode		—	±3.5	—		
T	Differential Non-Linearity	10-bit mode	DNL	—	—	—	LSB[2]	
		8-bit mode		—	±1.0	—		
		Monotonicity and No-Missing-Codes guaranteed						
C	Integral Non-Linearity	10-bit mode	INL	—	—	—	LSB[2]	
		8-bit mode		—	±1.5	—		
C	Zero-Scale Error	10-bit mode	E_{ZS}	—	—	—	LSB[2]	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	±1.5	—		
C	Full-Scale Error	10-bit mode	E_{FS}	—	—	—	LSB[2]	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	±1.0	—		
D	Quantization Error	10-bit mode	E_Q	—	—	—	LSB[2]	
		8-bit mode		—	—	±0.5		

3.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).