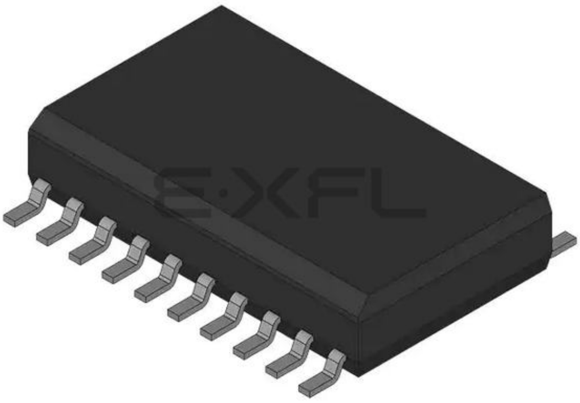

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	254 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9rs08kb8cwj

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

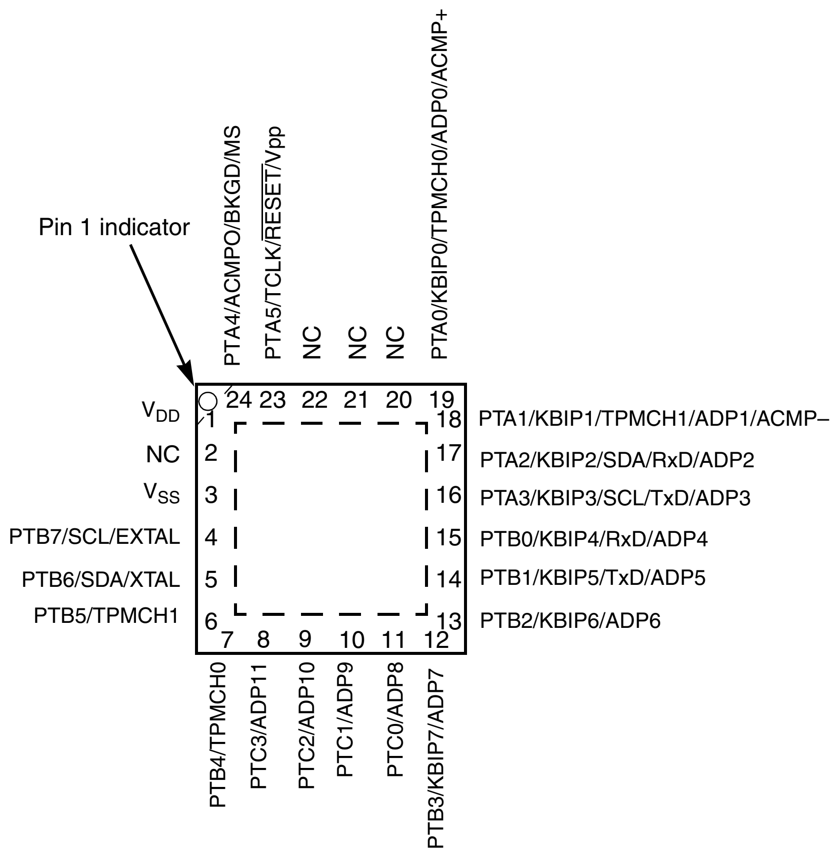


Figure 2. MC9RS08KB12 Series 24-Pin QFN Package

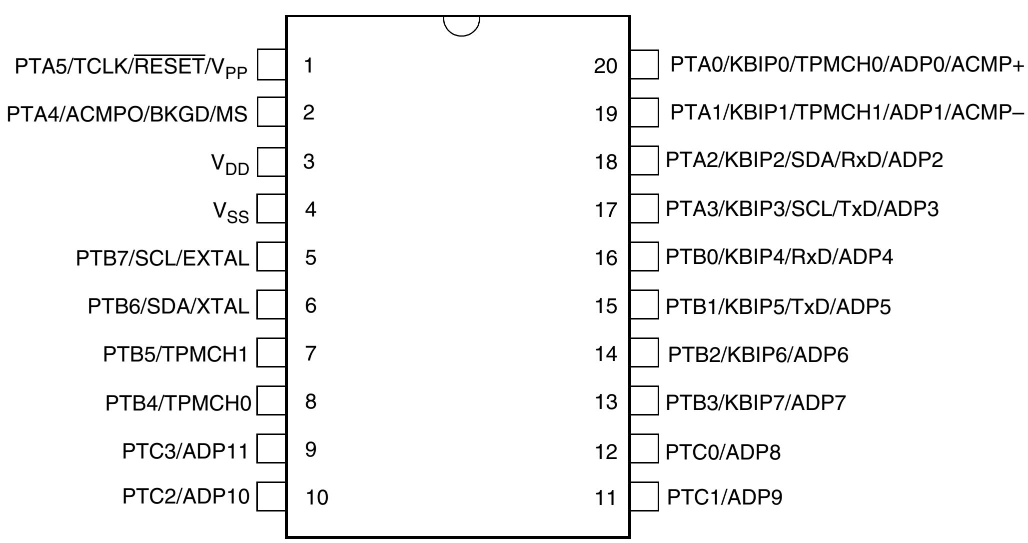


Figure 3. MC9RS08KB12 Series 20-Pin SOIC Package

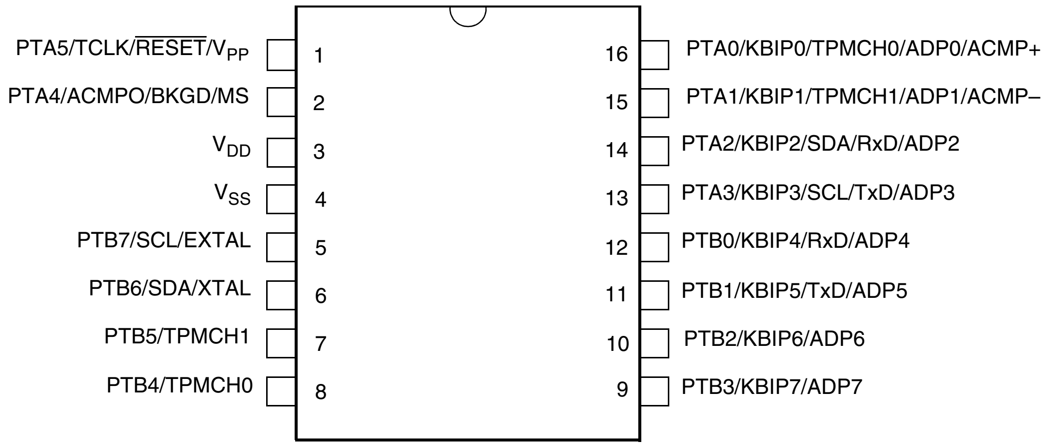


Figure 4. MC9RS08KB12 Series 16-Pin SOIC NB/TSSOP Package

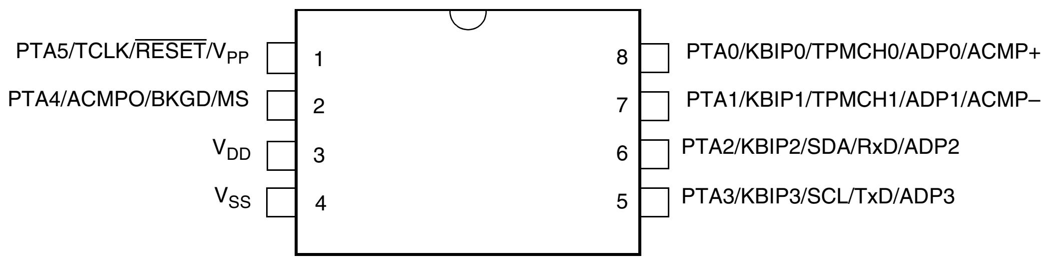


Figure 5. MC9RS08KB12 Series 8-Pin SOIC/DFN Package

3 Electrical Characteristics

3.1 Introduction

This chapter contains electrical and timing specifications for the MC9RS08KB12 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.

Table 2. Parameter Classifications

D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{\text{RESET}}/V_{PP}$ pin which is internally clamped to V_{SS} only.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external VDD load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of

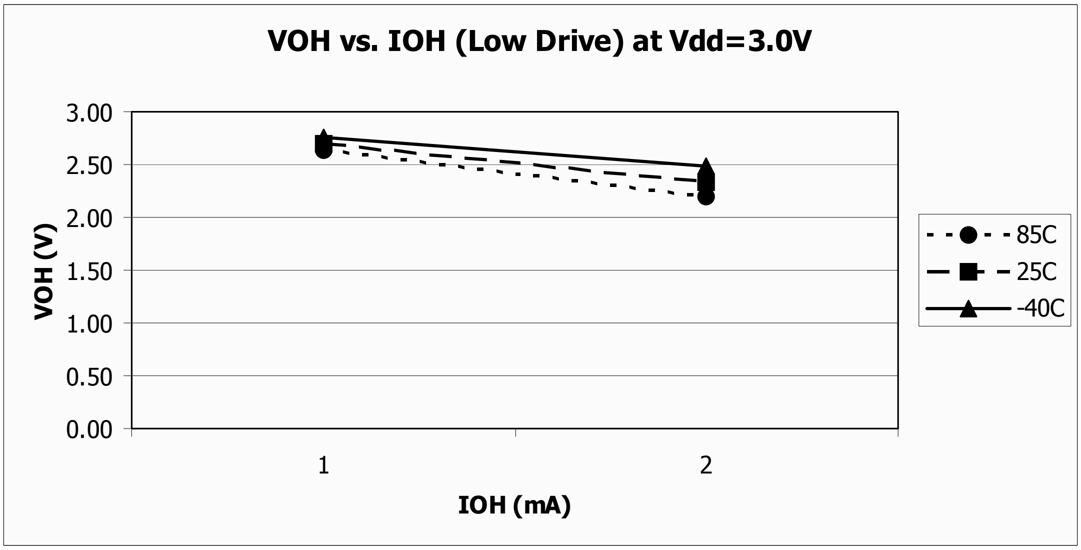


Figure 9. Typical V_{OH} vs. I_{OH}
V_{DD} = 3.0 V (Low Drive)

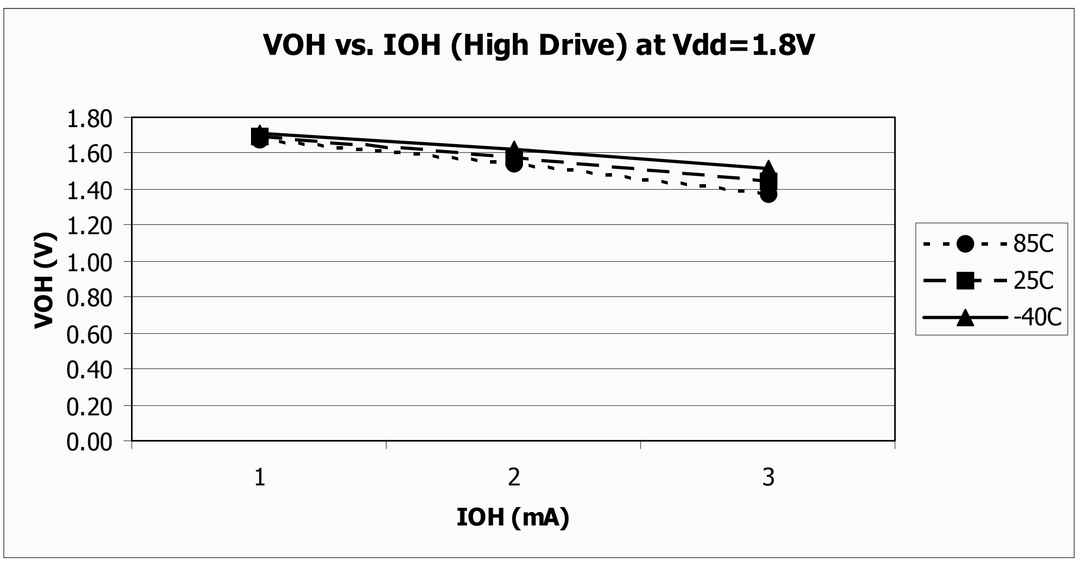


Figure 10. Typical V_{OH} vs. I_{OH}
V_{DD} = 1.8 V (High Drive)

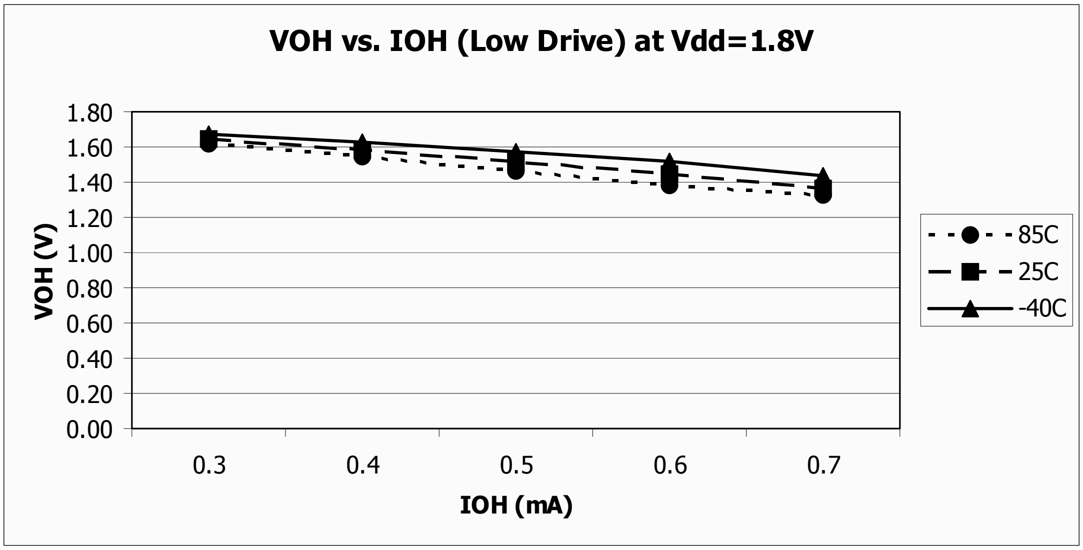


Figure 11. Typical V_{OH} vs. I_{OH}
V_{DD} = 1.8 V (Low Drive)

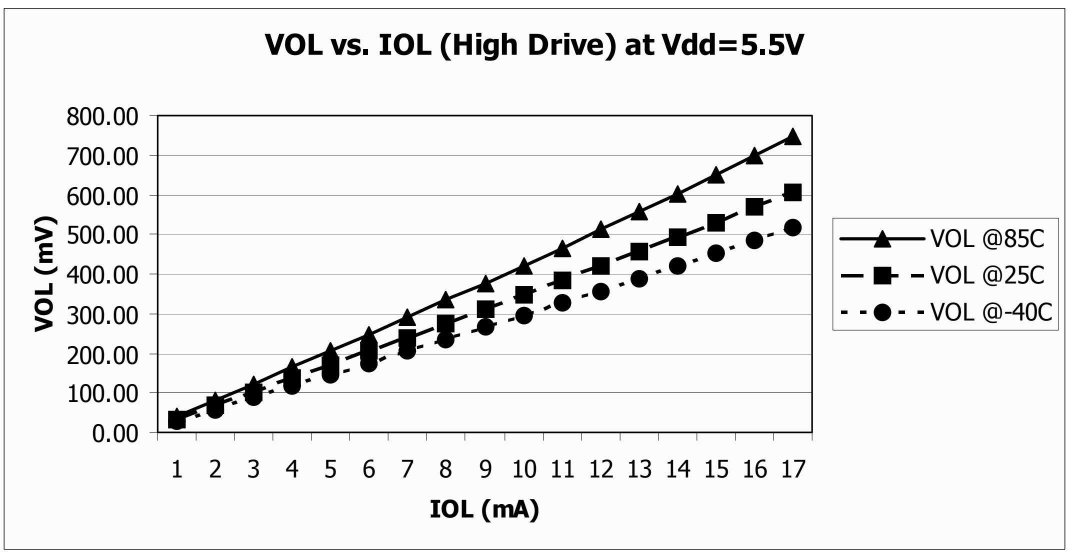


Figure 12. Typical V_{OL} vs. I_{OL}
V_{DD} = 5.5 V (High Drive)

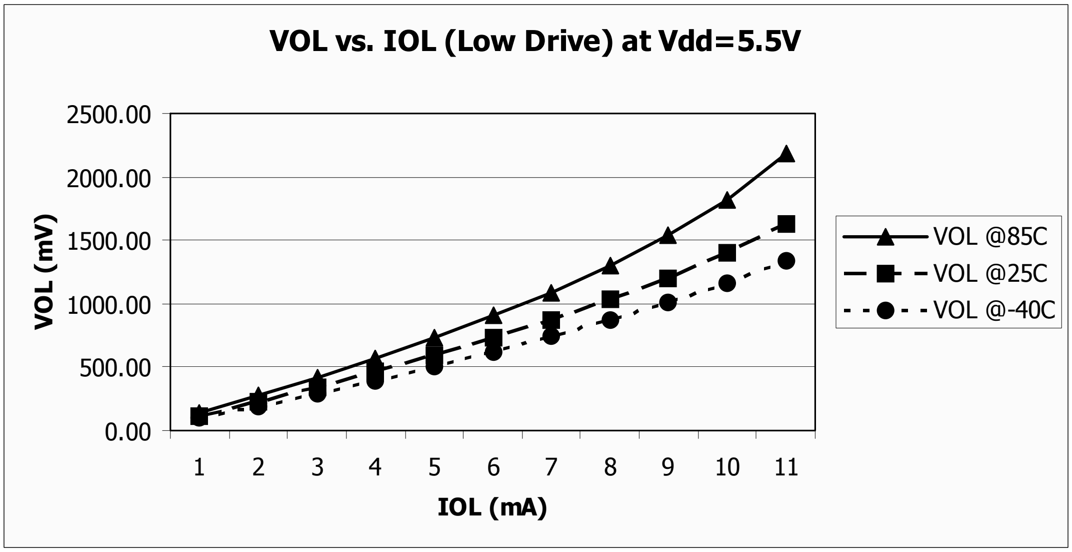


Figure 13. Typical V_{OL} vs. I_{OL}
V_{DD} = 5.5 V (Low Drive)

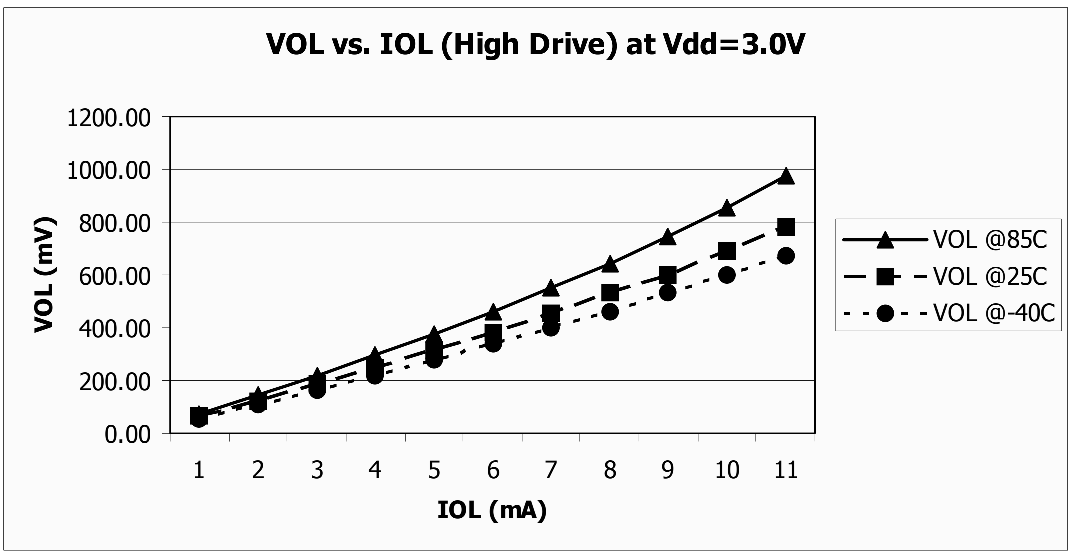


Figure 14. Typical V_{OL} vs. I_{OL}
V_{DD} = 3.0 V (High Drive)

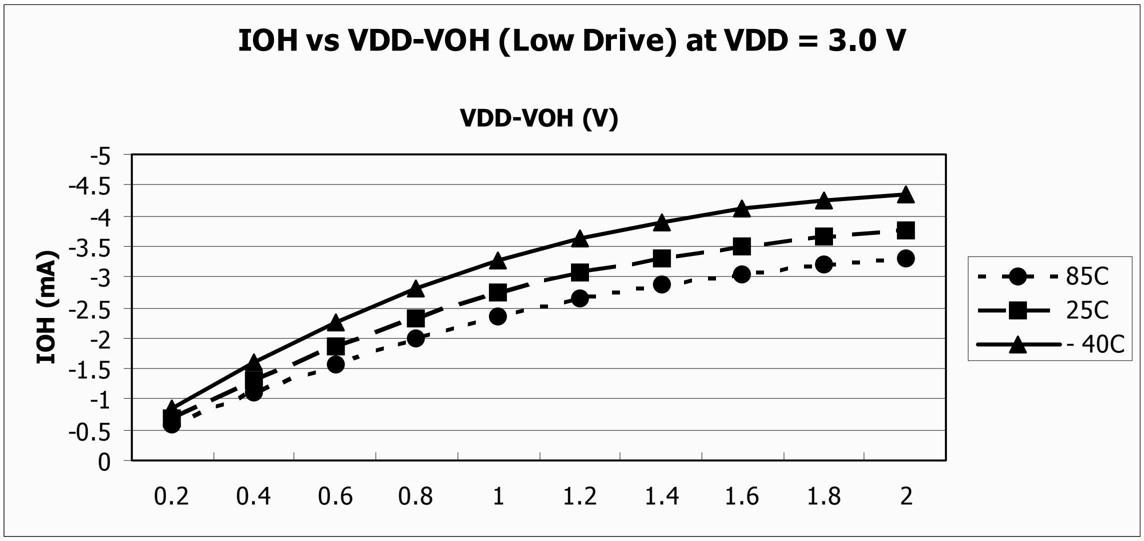


Figure 21. Typical I_{OH} vs. V_{DD}–V_{OH}
V_{DD} = 3 V (Low Drive)

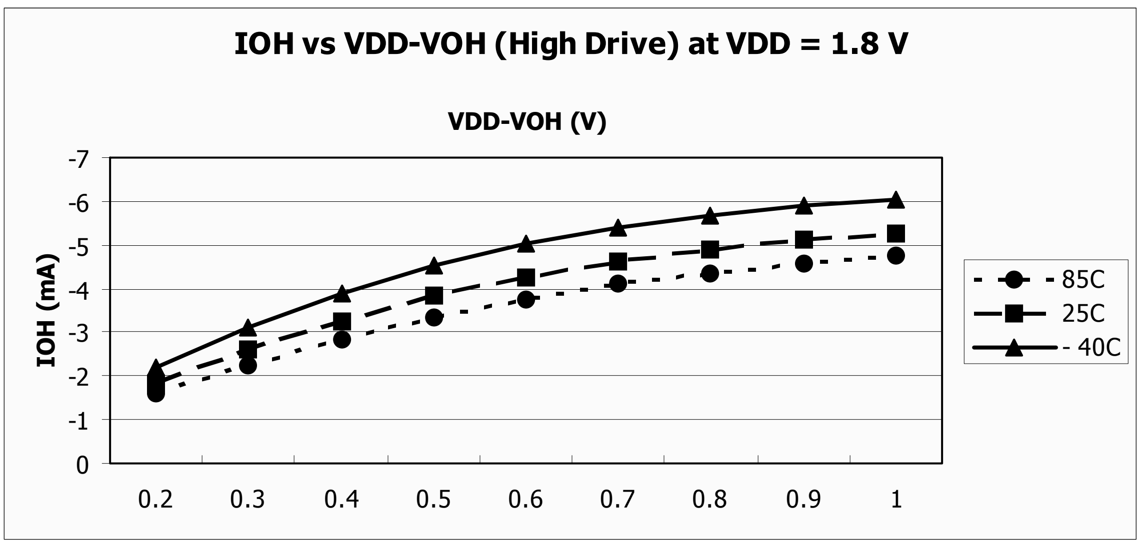


Figure 22. Typical I_{OH} vs. V_{DD}–V_{OH}
V_{DD} = 1.8 V (High Drive)

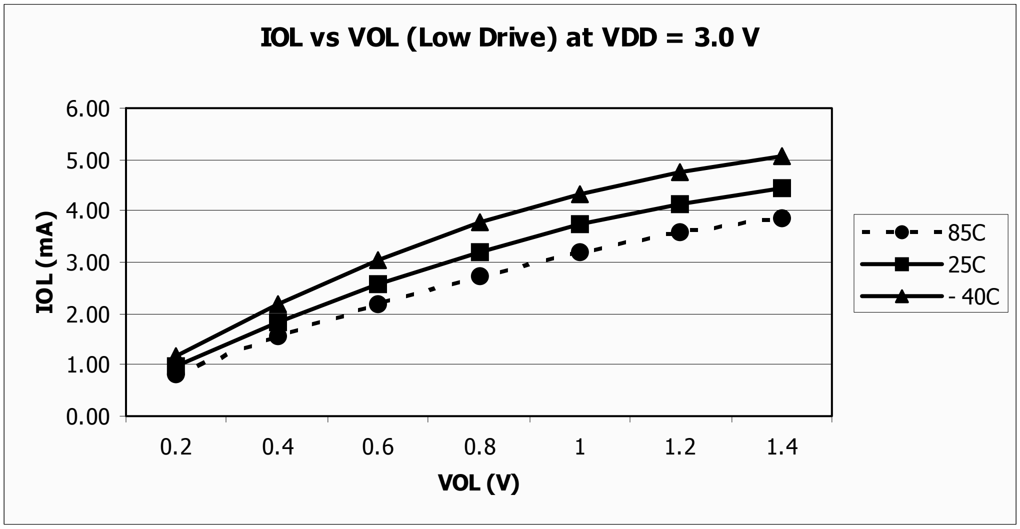


Figure 27. Typical I_{OL} vs. V_{OL}
V_{DD} = 3 V (Low Drive)

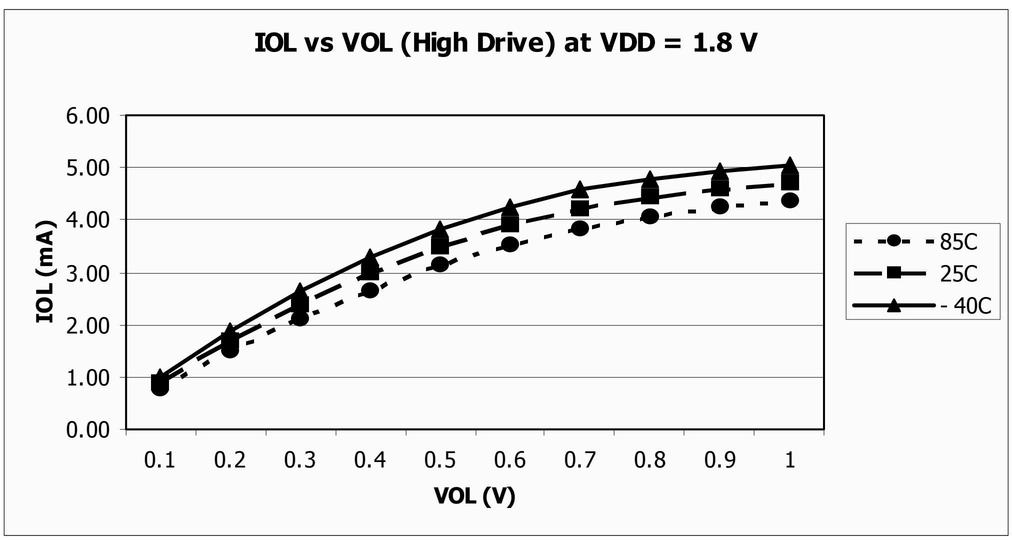


Figure 28. Typical I_{OL} vs. V_{OL}
V_{DD} = 1.8 V (High Drive)

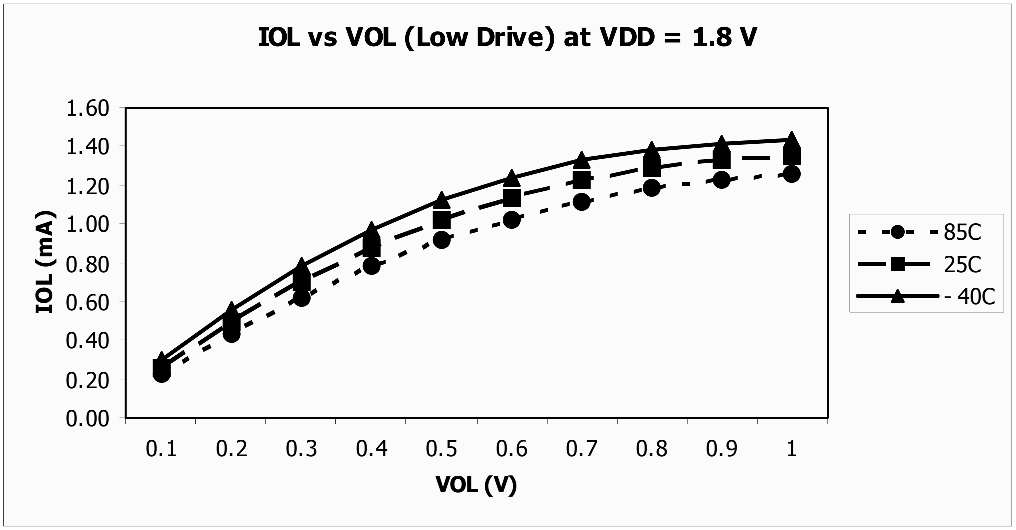


Figure 29. Typical I_{OL} vs. V_{OL}
V_{DD} = 1.8 V (Low Drive)

3.7 Supply Current Characteristics

Table 8. Supply Current Characteristics

N	C	Parameter	Symbol	V_{DD} (V)	Typical	Max[1]	Temp. (°C)	Unit
1	P	Run supply current[2] measured at (f_{Bus} = 10 MHz)	RI_{DD10}	5	3.45 3.48 3.53	7	–40 25 85	mA
2	C			3	3.39 3.42 3.49	—	–40 25 85	
3	C			1.80	2.40 2.42 2.44	—	–40 25 85	
4	C	Run supply current[3] measured at (f_{Bus} = 1.25 MHz)	RI_{DD1}	5	0.93 0.96 0.99	—	–40 25 85	mA
5	T			3	0.91 0.92 0.92	—	–40 25 85	
6	T			1.80	0.66 0.67 0.68	—	–40 25 85	

Table 8. Supply Current Characteristics (continued)

N	C	Parameter	Symbol	V_{DD} (V)	Typical	Max[1]	Temp. (°C)	Unit
22	C	RTI adder from stop with 1 kHz clock source enabled[4]	—	5	0.10 0.10 0.17	—	–40 25 85	µA
23	T			3	0.02 0.06 0.02	—	–40 25 85	
24	T			1.80	0.40 0.45 0.20	—	–40 25 85	
25	T	RTI adder from stop with 32.768KHz external clock source reference enabled	—	5	0.70 1.08 1.94	—	–40 25 85	µA
26	T			3	0.56 0.56 0.62	—	–40 25 85	
27	T			1.80	0.70 0.86 0.50	—	–40 25 85	
28	C	LVI adder from stop (LVDE = 1 and LVDSE = 1)	—	5	58.93 68.27 76.60	—	–40 25 85	µA
29	T			3	58.89 61.98 63.45	—	–40 25 85	
30	T			1.80	52.84 54.52 52.49	—	–40 25 85	

[1] Maximum value is measured at the nominal V_{DD} voltage times 10% tolerance. Values given here are preliminary estimates prior to completing characterization.

[2] Not include any DC loads on port pins.

[3] Required asynchronous ADC clock and LVD to be enabled.

[4] Most customers are expected to find that auto-wakeup from stop can be used instead of the higher current wait mode. Wait mode typical is 672.79 µA at 3 V and 509.28 µA at 1.8 V with f_{Bus} = 1 MHz.

3.9.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

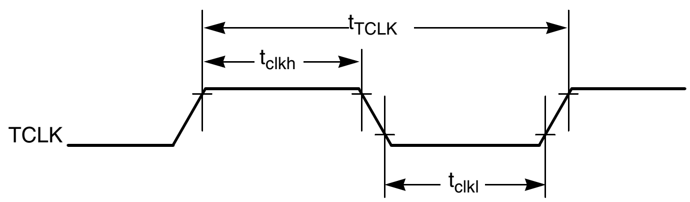


Figure 32. Timer External Clock

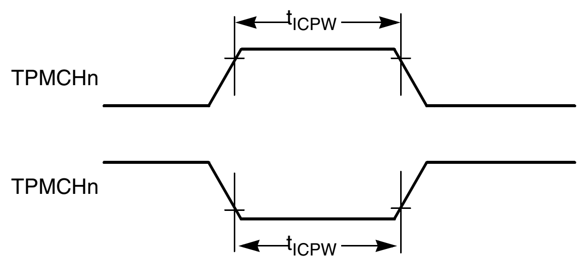


Figure 33. Timer Input Capture Pulse

3.10 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DD}	1.80	—	5.5	V
2	P	Supply current (active)	I_{DDAC}	—	20	35	µA
3	D	Analog input voltage[1]	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
4	C	Analog input offset voltage[1]	V_{AIO}	—	20	40	mV
5	C	Analog Comparator hysteresis[1]	V_H	3.0	9.0	15.0	mV
6	C	Analog source impedance[1]	R_{AS}	—	—	10	kΩ
7	P	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
8	C	Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	µs

Table 14. 10-Bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
ADC conversion clock Freq.	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC=1)		0.4	—	4.0		

[1] Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

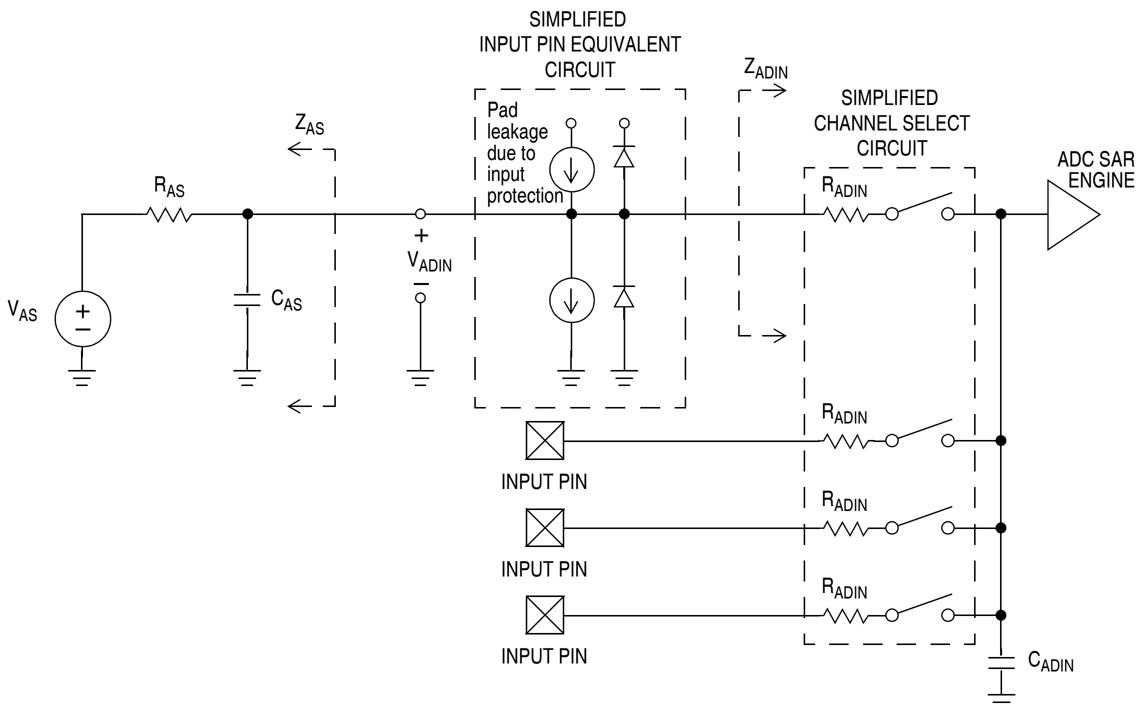


Figure 34. ADC Input Impedance Equivalency Diagram

Table 15. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 2.7 V < V_{DDAD} < 5.5 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	133	—	µA	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	218	—	µA	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	327	—	µA	

Table 15. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 2.7 V < V_{DDAD} < 5.5 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
C	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	0.582	1	mA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	E_{TUE}	—	±1.5	±3.5	LSB[2]	Includes quantization
		8-bit mode		—	±0.7	±1.5		
T	Differential Non-Linearity	10-bit mode	DNL	—	±0.5	±1.0	LSB[2]	
		8-bit mode		—	±0.3	±0.5		
		Monotonicity and No-Missing-Codes guaranteed						
C	Integral Non-Linearity	10-bit mode	INL	—	±0.5	±1.0	LSB[2]	
		8-bit mode		—	±0.3	±0.5		
P	Zero-Scale Error	10-bit mode	E_{ZS}	—	±1.5	±2.5	LSB[2]	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	±0.5	±0.7		
P	Full-Scale Error	10-bit mode	E_{FS}	—	±1	±1.5	LSB[2]	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	±0.5	±0.5		
D	Quantization Error	10-bit mode	E_Q	—	—	±0.5	LSB[2]	
		8-bit mode		—	—	±0.5		
D	Input Leakage Error	10-bit mode	E_{IL}	—	±0.2	±2.5	LSB[2]	Pad leakage[2] * R_{AS}
		8-bit mode		—	±0.1	±1		

[1] Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] Based on input pad leakage current. Refer to pad electricals.

Table 16. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 1.8 V < V_{DDAD} < 2.7 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	8-bit mode	I_{DDAD}	—	88	—	µA	
T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	8-bit mode	I_{DDAD}	—	152	—	µA	
T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	8-bit mode	I_{DDAD}	—	214	—	µA	
T	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	8-bit mode	I_{DDAD}	—	390	—	µA	
C	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
		Low Power (ADLPC = 1)		1.25	2	3.3		
D	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See reference manual for conversion time variances
		Long Sample (ADLSMP = 1)		—	40	—		
D	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long Sample (ADLSMP = 1)		—	23.5	—		
C	Total Unadjusted Error	10-bit mode	E_{TUE}	—	—	—	LSB[2]	Includes quantization
		8-bit mode		—	±3.5	—		
T	Differential Non-Linearity	10-bit mode	DNL	—	—	—	LSB[2]	
		8-bit mode		—	±1.0	—		
		Monotonicity and No-Missing-Codes guaranteed						
C	Integral Non-Linearity	10-bit mode	INL	—	—	—	LSB[2]	
		8-bit mode		—	±1.5	—		
C	Zero-Scale Error	10-bit mode	E_{ZS}	—	—	—	LSB[2]	$V_{ADIN} = V_{SSA}$
		8-bit mode		—	±1.5	—		
C	Full-Scale Error	10-bit mode	E_{FS}	—	—	—	LSB[2]	$V_{ADIN} = V_{DDA}$
		8-bit mode		—	±1.0	—		
D	Quantization Error	10-bit mode	E_Q	—	—	—	LSB[2]	
		8-bit mode		—	—	±0.5		

Table 16. 10-Bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, 1.8 V < V_{DDAD} < 2.7 V)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
D	Input Leakage Error	10-bit mode	E_{IL}	—	—	—	LSB[2]	Pad leakage[2] * R_{AS}
		8-bit mode		—	±0.1	±1		

[1] Typical values assume V_{DDAD} = 1.8 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

Table 17. Flash Characteristics

No.	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	D	Supply voltage for program/erase	V_{DD}	2.7	—	5.5	V
2	D	Program/Erase voltage	V_{PP}	11.8	12	12.2	V
3	C	VPP current Program Mass erase	 I_{VPP_prog} I_{VPP_erase}	 — —	 — —	 200 100	 µA µA
4	D	Supply voltage for read operation 0 < f_{Bus} < 10 MHz	V_{Read}	1.8	—	5.5	V
5	P	Byte program time	t_{prog}	20	—	40	µs
6	P	Mass erase time	t_{me}	500	—	—	ms
7	C	Cumulative program HV time[2]	t_{hv}	—	—	8	ms
8	C	Total cumulative HV time (total of t_{me} & t_{hv} applied to device)	t_{hv_total}	—	—	2	hours
9	D	HVEN to program setup time	t_{pgs}	10	—	—	µs
10	D	PGM/MASS to HVEN setup time	t_{nvs}	5	—	—	µs
11	D	HVEN hold time for PGM	t_{nvh}	5	—	—	µs
12	D	HVEN hold time for MASS	t_{nvh1}	100	—	—	µs
13	D	V_{PP} to PGM/MASS setup time	t_{vps}	20	—	—	ns
14	D	HVEN to V_{PP} hold time	t_{vph}	20	—	—	ns
15	D	V_{PP} rise time[3]	t_{vrs}	200	—	—	ns
16	D	Recovery time	t_{rcv}	1	—	—	µs
17	D	Program/erase endurance T_L to T_H = –40 °C to 85 °C	—	1000	—	—	cycles
18	C	Data retention	t_{D_ret}	15	—	—	years

[1] Typicals are measured at 25 °C.

[2] t_{hv} is the cumulative high voltage programming time to the same row before next erase. Same address can not be programmed more than twice before next erase.

[3] Fast V_{PP} rise time may potentially trigger the ESD protection structure, which may result in over current flowing into the pad and cause permanent damage to the pad. External filtering for the V_{PP} power source is recommended. An example V_{PP} filter is shown in Figure 35.

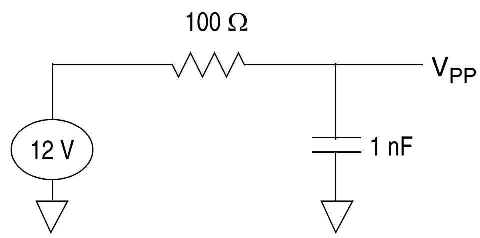
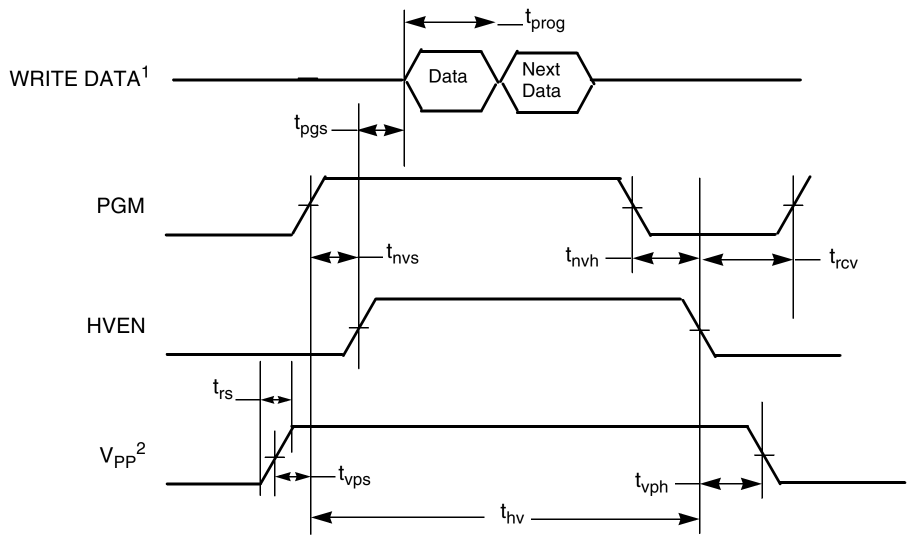


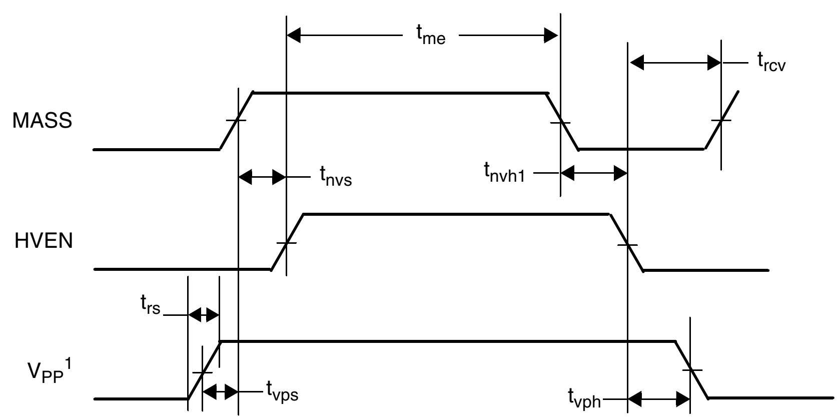
Figure 35. Example V_{PP} Filtering



[1] Next Data applies if programming multiple bytes in a single row, refer to *MC9RS08KB12 Series Reference Manual*.

[2] V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 36. Flash Program Timing



[1] V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 37. Flash Mass Erase Timing

3.14 EMC Performance

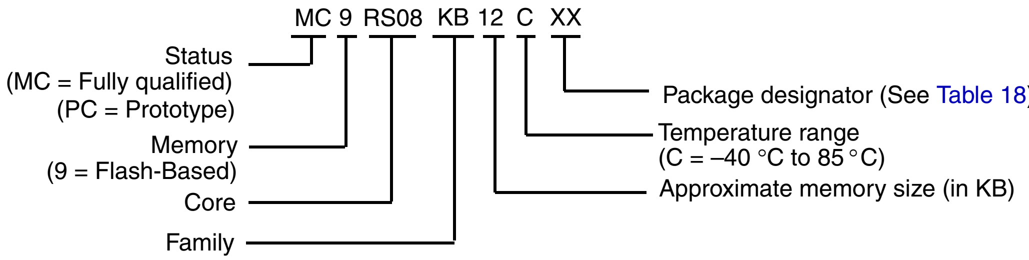
Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

4 Ordering Information

This section contains ordering numbers for MC9RS08KB12 series devices. See below for an example of the device numbering system.



5 Package Information and Mechanical Drawings

Table 18 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9RS08KB12 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 18, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 18) in the "Enter Keyword" search box at the top of the page.

Table 18. Device Numbering System

Device Number	Memory		Package		
	Flash	RAM	Type	Designator	Document No.
MC9RS08KB12 **MC9RS08KB8** **MC9RS08KB4**	12 KB 8 KB 4 KB	254 bytes 254 bytes 126 bytes	24 QFN	FK	98ASA00087D
			20 SOIC WB	WJ	98ASB42343B
			16 SOIC NB	SG	98ASB42566B
			16 TSSOP	TG	98ASH70247A
MC9RS08KB2	2 KB	126 bytes	8 SOIC NB	SC	98ASB42564B
			8 DFN	DC	98ARL10557D

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Document Number: MC9RS08KB12
Rev. 5
1/2012