# Cypress Semiconductor Corp - MB95F418HPMC-G-SNE2 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-8FX |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, SIO, UART/USART |
| Peripherals | LCD, POR, PWM, WDT |
| Number of I/O | 74 |
| Program Memory Size | 60KB (60K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.98K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | 80-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb95f418hpmc-g-sne2 |

### Low-voltage detection reset circuit

Built-in low-voltage detector

### Clock supervisor counter

Built-in clock supervisor counter function

### Programmable port input voltage level

CMOS input level / hysteresis input level

### Dual operation Flash memory

The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

### Flash memory security function

Protects the content of the Flash memory

# 4. Differences among Products and Notes on Product Selection

### Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see “17. Electrical Characteristics”.

### Package

For details of information on each package, see “3. Packages And Corresponding Products” and “21. Package Dimension”.

### Operating voltage

The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see “17. Electrical Characteristics”.

### On-chip debug function

The on-chip debug function requires that $V_{CC}$, $V_{SS}$ and 1 serial-wire be connected to an evaluation tool. For details of the connection method, refer to “Chapter 31 Example Of Serial Programming Connection” in the hardware manual of the MB95410H/470H Series.

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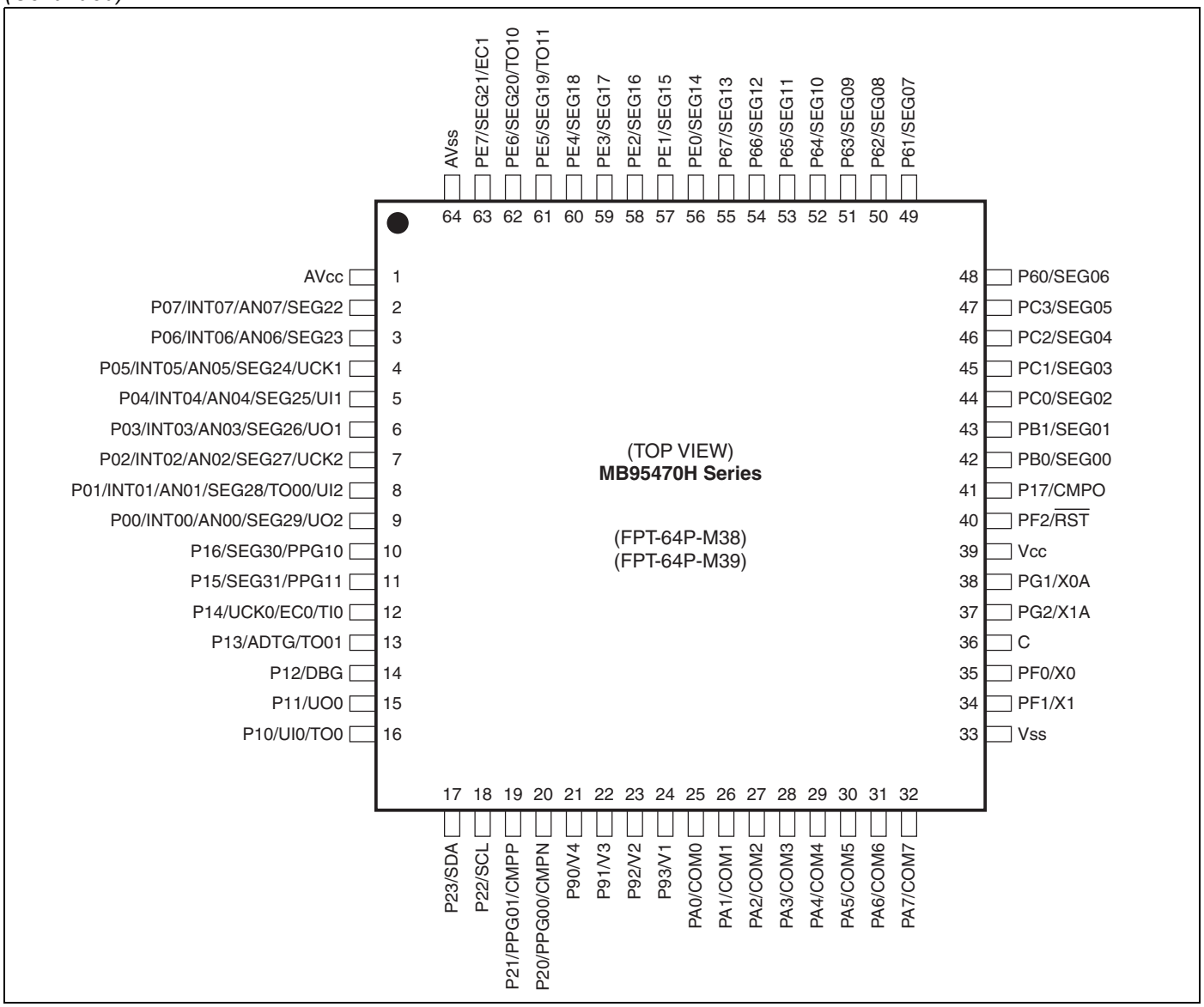

AVss
PE7/SEG21/EC1
PE6/SEG20/TO10
PE5/SEG19/TO11
PE4/SEG18
PE3/SEG17
PE2/SEG16
PE1/SEG15
PE0/SEG14
P67/SEG13
P66/SEG12
P65/SEG11
P64/SEG10
P63/SEG09
P62/SEG08
P61/SEG07
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
AVcc 1
P07/INT07/AN07/SEG22 2
P06/INT06/AN06/SEG23 3
P05/INT05/AN05/SEG24/UCK1 4
P04/INT04/AN04/SEG25/UI1 5
P03/INT03/AN03/SEG26/UO1 6
P02/INT02/AN02/SEG27/UCK2 7
P01/INT01/AN01/SEG28/TO00/UI2 8
P00/INT00/AN00/SEG29/UO2 9
P16/SEG30/PPG10 10
P15/SEG31/PPG11 11
P14/UCK0/EC0/TI0 12
P13/ADTG/TO01 13
P12/DBG 14
P11/UO0 15
P10/UI0/TO0 16
(TOP VIEW)
MB95470H Series
(FPT-64P-M38)
(FPT-64P-M39)
48 P60/SEG06
47 PC3/SEG05
46 PC2/SEG04
45 PC1/SEG03
44 PC0/SEG02
43 PB1/SEG01
42 PB0/SEG00
41 P17/CMPO
40 PF2/RST
39 Vcc
38 PG1/X0A
37 PG2/X1A
36 C
35 PF0/X0
34 PF1/X1
33 Vss
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
P23/SDA
P22/SCL
P21/PPG01/CMPP
P20/PPG00/CMPN
P90/V4
P91/V3
P92/V2
P93/V1
PA0/COM0
PA1/COM1
PA2/COM2
PA3/COM3
PA4/COM4
PA5/COM5
PA6/COM6
PA7/COM7

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 9 | P00 | W | General-purpose I/O port |
| | INT00 | | External interrupt input pin |
| | AN00 | | A/D analog input pin |
| | UO2 | | UART/SIO ch. 2 data output pin |
| 10 | P16 | Y | General-purpose I/O port |
| | PPG10 | | 8/16-bit PPG ch. 1 output pin |
| 11 | P15 | Y | General-purpose I/O port |
| | PPG11 | | 8/16-bit PPG ch. 1 output pin |
| 12 | P14 | H | General-purpose I/O port |
| | UCK0 | | UART/SIO ch. 0 clock I/O pin |
| 13 | P13 | H | General-purpose I/O port |
| | ADTG | | A/D trigger input (ADTG) pin |
| 14 | P12 | D | General-purpose I/O port |
| | DBG | | DBG input pin |
| 15 | P11 | H | General-purpose I/O port |
| | UO0 | | UART/SIO ch. 0 data output pin |
| 16 | P10 | G | General-purpose I/O port |
| | UI0 | | UART/SIO ch. 0 data input pin |
| 17 | P53 | H | General-purpose I/O port |
| | TO0 | | 16-bit reload timer output pin |
| 18 | P52 | H | General-purpose I/O port |
| | TI0 | | 16-bit reload timer input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 19 | P51 | H | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 20 | P50 | H | General-purpose I/O port |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 21 | P23 | I | General-purpose I/O port |
| | SDA | | $I^2C$ data I/O pin |
| 22 | P22 | I | General-purpose I/O port |
| | SCL | | $I^2C$ clock I/O pin |
| 23 | P21 | T | General-purpose I/O port |
| | PPG01 | | 8/16-bit PPG ch. 0 output pin |
| | CMPP | | Voltage comparator input pin |
| 24 | P20 | T | General-purpose I/O port |
| | PPG00 | | 8/16-bit PPG ch. 0 output pin |
| | CMPN | | Voltage comparator input pin |

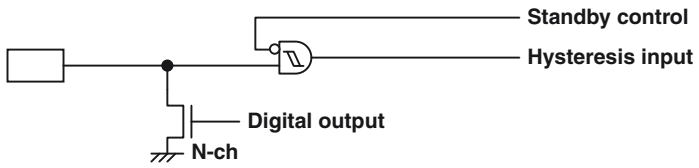
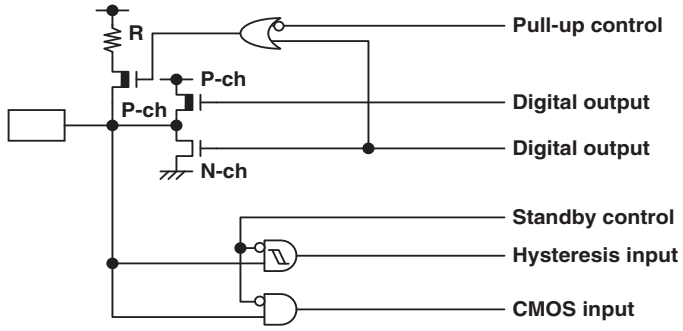
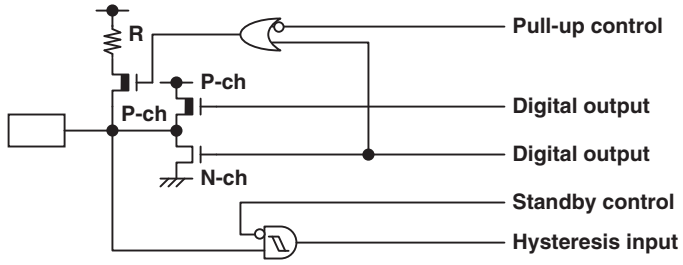
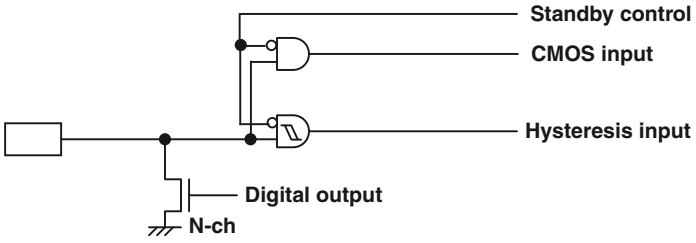
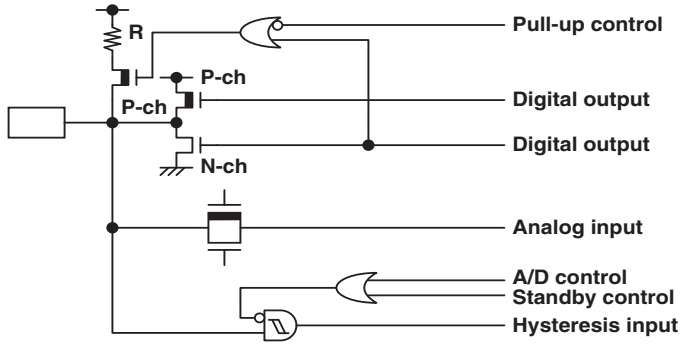
*(Continued)*

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 44 | C | — | Capacitor connection pin |
| 45 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock oscillation pin (32 kHz) |
| 46 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock oscillation pin (32 kHz) |
| 47 | $V_{CC}$ | — | Power supply pin |
| 48 | PF2 | A | General-purpose I/O port |
| | RST | | Reset pin<br>Dedicate reset pin for MB95F414H/F416H/F418H |
| 49 | P17 | H | General-purpose I/O port |
| | CMPO | | Voltage comparator output pin |
| 50 | PB0 | M | General-purpose I/O port |
| | SEG00 | | LCDC SEG output pin |
| 51 | PB1 | M | General-purpose I/O port |
| | SEG01 | | LCDC SEG output pin |
| 52 | PC0 | M | General-purpose I/O port |
| | SEG02 | | LCDC SEG output pin |
| 53 | PC1 | M | General-purpose I/O port |
| | SEG03 | | LCDC SEG output pin |
| 54 | PC2 | M | General-purpose I/O port |
| | SEG04 | | LCDC SEG output pin |
| 55 | PC3 | M | General-purpose I/O port |
| | SEG05 | | LCDC SEG output pin |
| 56 | PC4 | M | General-purpose I/O port |
| | SEG06 | | LCDC SEG output pin |
| 57 | PC5 | M | General-purpose I/O port |
| | SEG07 | | LCDC SEG output pin |
| 58 | PC6 | M | General-purpose I/O port |
| | SEG08 | | LCDC SEG output pin |
| 59 | PC7 | M | General-purpose I/O port |
| | SEG09 | | LCDC SEG output pin |
| 60 | P60 | M | General-purpose I/O port |
| | SEG10 | | LCDC SEG output pin |
| 61 | P61 | M | General-purpose I/O port |
| | SEG11 | | LCDC SEG output pin |
| 62 | P62 | M | General-purpose I/O port |
| | SEG12 | | LCDC SEG output pin |

*(Continued)*

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 41 | P17 | H | General-purpose I/O port |
| | CMPO | | Voltage comparator output pin |
| 42 | PB0 | M | General-purpose I/O port |
| | SEG00 | | LCDC SEG output pin |
| 43 | PB1 | M | General-purpose I/O port |
| | SEG01 | | LCDC SEG output pin |
| 44 | PC0 | M | General-purpose I/O port |
| | SEG02 | | LCDC SEG output pin |
| 45 | PC1 | M | General-purpose I/O port |
| | SEG03 | | LCDC SEG output pin |
| 46 | PC2 | M | General-purpose I/O port |
| | SEG04 | | LCDC SEG output pin |
| 47 | PC3 | M | General-purpose I/O port |
| | SEG05 | | LCDC SEG output pin |
| 48 | P60 | M | General-purpose I/O port |
| | SEG06 | | LCDC SEG output pin |
| 49 | P61 | M | General-purpose I/O port |
| | SEG07 | | LCDC SEG output pin |
| 50 | P62 | M | General-purpose I/O port |
| | SEG08 | | LCDC SEG output pin |
| 51 | P63 | M | General-purpose I/O port |
| | SEG09 | | LCDC SEG output pin |
| 52 | P64 | M | General-purpose I/O port |
| | SEG10 | | LCDC SEG output pin |
| 53 | P65 | M | General-purpose I/O port |
| | SEG11 | | LCDC SEG output pin |
| 54 | P66 | M | General-purpose I/O port |
| | SEG12 | | LCDC SEG output pin |
| 55 | P67 | M | General-purpose I/O port |
| | SEG13 | | LCDC SEG output pin |
| 56 | PE0 | M | General-purpose I/O port |
| | SEG14 | | LCDC SEG output pin |
| 57 | PE1 | M | General-purpose I/O port |
| | SEG15 | | LCDC SEG output pin |

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| D |  | • N-ch open drain output<br>• Hysteresis input |
| G |  | • CMOS output<br>• Hysteresis input<br>• CMOS input<br>• Pull-up control available |
| H |  | • CMOS output<br>• Hysteresis input<br>• Pull-up control available |
| I |  | • N-ch open drain output<br>• CMOS input<br>• Hysteresis input |
| J |  | • CMOS output<br>• Hysteresis input<br>• Analog input<br>• Pull-up control available |

*(Continued)*

## 9. Notes on Device Handling

### Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than $V_{CC}$ or a voltage lower than $V_{SS}$ is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "17.1 Absolute Maximum Ratings" of “17. Electrical Characteristics” is applied to the $V_{CC}$ pin or the $V_{SS}$ pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

### Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the $V_{CC}$ power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in $V_{CC}$ ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard $V_{CC}$ value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

### Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

## 10. Pin Connection

### Treatment of unused input pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

### Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the $V_{CC}$ pin and the $V_{SS}$ pin to the power supply and ground outside the device. In addition, connect the current supply source to the $V_{CC}$ pin and the $V_{SS}$ pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the $V_{CC}$ pin and the $V_{SS}$ pin at a location close to this device.

### DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the $V_{CC}$ or $V_{SS}$ pin when designing the layout of the printed circuit board.

The DBG pin should not stay at “L” level after power-on until the reset output is released.

### $\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{\text{RST}}$ pin and the $V_{CC}$ or $V_{SS}$ pin when designing the layout of the printed circuit board.

The PF2/$\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output function of the PF2/$\overline{\text{RST}}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function or the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

### Analog power supply

Always set the same potential to $AV_{CC}$ and $V_{CC}$ pins. When $V_{CC}$ is larger than $AV_{CC}$, the current may flow through the AN00 to AN07 pins.

## 14. I/O Map (MB95410H Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| $0000_H$ | PDR0 | Port 0 data register | R/W | $00000000_B$ |
| $0001_H$ | DDR0 | Port 0 direction register | R/W | $00000000_B$ |
| $0002_H$ | PDR1 | Port 1 data register | R/W | $00000000_B$ |
| $0003_H$ | DDR1 | Port 1 direction register | R/W | $00000000_B$ |
| $0004_H$ | — | (Disabled) | — | — |
| $0005_H$ | WATR | Oscillation stabilization wait time setting register | R/W | $11111111_B$ |
| $0006_H$ | PLLC | PLL control register | R/W | $00000000_B$ |
| $0007_H$ | SYCC | System clock control register | R/W | $XXXXXX11_B$ |
| $0008_H$ | STBC | Standby control register | R/W | $00000XXX_B$ |
| $0009_H$ | RSRR | Reset source register | R/W | $000XXXXX_B$ |
| $000A_H$ | TBTC | Time-base timer control register | R/W | $00000000_B$ |
| $000B_H$ | WPCR | Watch prescaler control register | R/W | $00000000_B$ |
| $000C_H$ | WDTC | Watchdog timer control register | R/W | $00000000_B$ |
| $000D_H$ | SYCC2 | System clock control register 2 | R/W | $XX100011_B$ |
| $000E_H$ | PDR2 | Port 2 data register | R/W | $00000000_B$ |
| $000F_H$ | DDR2 | Port 2 direction register | R/W | $00000000_B$ |
| $0010_H$, $0011_H$ | — | (Disabled) | — | — |
| $0012_H$ | PDR4 | Port 4 data register | R/W | $00000000_B$ |
| $0013_H$ | DDR4 | Port 4 direction register | R/W | $00000000_B$ |
| $0014_H$ | PDR5 | Port 5 data register | R/W | $00000000_B$ |
| $0015_H$ | DDR5 | Port 5 direction register | R/W | $00000000_B$ |
| $0016_H$ | PDR6 | Port 6 data register | R/W | $00000000_B$ |
| $0017_H$ | DDR6 | Port 6 direction register | R/W | $00000000_B$ |
| $0018_H$ to $001B_H$ | — | (Disabled) | — | — |
| $001C_H$ | PDR9 | Port 9 data register | R/W | $00000000_B$ |
| $001D_H$ | DDR9 | Port 9 direction register | R/W | $00000000_B$ |
| $001E_H$ | PDRA | Port A data register | R/W | $00000000_B$ |
| $001F_H$ | DDRA | Port A direction register | R/W | $00000000_B$ |
| $0020_H$ | PDRB | Port B data register | R/W | $00000000_B$ |
| $0021_H$ | DDRB | Port B direction register | R/W | $00000000_B$ |
| $0022_H$ | PDRC | Port C data register | R/W | $00000000_B$ |
| $0023_H$ | DDRC | Port C direction register | R/W | $00000000_B$ |
| $0024_H$, $0025_H$ | — | (Disabled) | — | — |

*(Continued)*

# 17. Electrical Characteristics

## 17.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1 | $V_{CC}$ | $V_{SS}$ − 0.3 | $V_{SS}$ + 6 | V | |
| Input voltage*1 | $V_I$ | $V_{SS}$ − 0.3 | $V_{SS}$ + 6 | V | *2 |
| Output voltage*1 | $V_O$ | $V_{SS}$ − 0.3 | $V_{SS}$ + 6 | V | *2 |
| Maximum clamp current | $I_{CLAMP}$ | −2 | +2 | mA | Applicable to specific pins*3 |
| Total maximum clamp current | $\Sigma\lvert I_{CLAMP}\rvert$ | — | 20 | mA | Applicable to specific pins*3 |
| “L” level maximum output current | $I_{CL}$ | — | 15 | mA | |
| “L” level average current | $I_{CLAV}$ | — | 4 | mA | Average output current = operating current × operating ratio (1 pin) |
| “L” level total maximum output current | $\Sigma I_{OL}$ | — | 100 | mA | |
| “L” level total average output current | $\Sigma I_{OLAV}$ | — | 50 | mA | Total average output current = operating current × operating ratio (Total number of pins) |
| “H” level maximum output current | $I_{CH}$ | — | −15 | mA | |
| “H” level average current | $I_{CHAV}$ | — | −4 | mA | Average output current = operating current × operating ratio (1 pin) |
| “H” level total maximum output current | $\Sigma I_{OH}$ | — | −100 | mA | |
| “H” level total average output current | $\Sigma I_{OHAV}$ | — | −50 | mA | Total average output current = operating current × operating ratio (Total number of pins) |
| Power consumption | $P_d$ | — | 320 | mW | |
| Operating temperature | $T_A$ | −40 | +85 | °C | |
| Storage temperature | $T_{stg}$ | −55 | +150 | °C | |

*1: These parameters are based on the condition that $V_{SS}$ = 0.0 V.

*2: $V_I$ and $V_O$ must not exceed $V_{CC}$ + 0.3 V. $V_I$ must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the $I_{CLAMP}$ rating is used instead of the $V_I$ rating.

*(Continued)*

($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = 0.0 V, $T_A$ = -40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ*4 | Max | | |
| Power supply current*3 | $I_{CCMPLL}$ | $V_{CC}$ (External clock operation) | $V_{CC}$ = 5.5 V<br>$F_{CH}$ = 4 MHz<br>$F_{MP}$ = 10 MHz<br>Main PLL mode (multiplied by 2.5)<br>$T_A$ = +25°C | — | 9.7 | 12.5 | mA | |
| | | | $V_{CC}$ = 5.5 V<br>$F_{CH}$ = 6.44 MHz<br>$F_{MP}$ = 16 MHz<br>Main PLL mode (multiplied by 2.5)<br>$T_A$ = +25°C | — | 13.9 | 20 | mA | |
| | $I_{CCMCR}$ | $V_{CC}$ | $V_{CC}$ = 5.5 V<br>$F_{CRH}$ = 12.5 MHz<br>$F_{MP}$ = 12.5 MHz<br>Main CR clock mode | — | 11 | 13.2 | mA | |
| | $I_{CCSCR}$ | | $V_{CC}$ = 5.5 V<br>Sub-CR clock mode (multiplied by 2.5)<br>$T_A$ = +25°C | — | 112 | 410 | µA | |
| | $I_{CCTS}$ | $V_{CC}$ (External clock operation) | $V_{CC}$ = 5.5 V<br>$F_{CH}$ = 32 MHz<br>Time-base timer mode<br>$T_A$ = +25°C | — | 1 | 3 | mA | |
| | $I_{CCH}$ | | $V_{CC}$ = 5.5 V<br>Substop mode<br>$T_A$ = +25°C | — | 3.1 | 22.5 | µA | Main stop mode with one clock selected |
| | $I_A$ | $AV_{CC}$ | Current consumption for A/D conversion at 16 MHz | — | 1.5 | 4.7 | mA | |
| | $I_{AH}$ | | Current consumption for stopping A/D conversion at 16 MHz | — | 1 | 5 | µA | |
| | $I_V$ | | Current consumption of voltage comparator at 16 MHz | — | 113 | 350 | µA | |

*(Continued)*

*(Continued)*

($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = 0.0 V, $T_A$ = -40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ*4 | Max | | |
| Power supply current*3 | $I_{LVD}$ | $V_{CC}$ | Current consumption of the low-voltage detection circuit | — | 31 | 54 | µA | |
| | $I_{CRH}$ | | Current consumption of the main CR oscillator | — | 0.5 | 0.6 | mA | |
| | $I_{CRL}$ | | Current consumption of the sub-CR oscillator oscillating at 100 kHz | — | 20 | 72 | µA | |
| LCD internal division resistance | $R_{LCD}$ | — | Between V4 and $V_{SS}$ | — | 400 | — | kΩ | |
| | | | | — | 40 | — | kΩ | |
| COM0 to COM7 output impedance | $R_{VCOM}$ | COM0 to COM7 | V1 to V4 = 4.1 V | — | — | 5 | kΩ | |
| SEG00 to SEG39 output impedance | $R_{VSEG}$ | SEG00 to SEG39 | | — | — | 7 | kΩ | |
| LCD leakage current | $I_{LCDL}$ | V0 to V4, COM0 to COM7, SEG00 to SEG39 | — | −1 | — | +1 | µA | |

*1: The input levels of P01, P04, P10, P22 and P23 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*2: P40 to P43, P50 to P53, P94, PB2 to PB4 and PC4 to PC7 are only available on the MB95410H Series.

*3:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit ($I_{LVD}$) to one of the value from $I_{CC}$ to $I_{CCH}$. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators ($I_{CRH}$, $I_{CRL}$) and a specified value. In on-chip debug mode, the CR oscillator ($I_{CRH}$) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See “17.4. AC Characteristics: 17.4.1. Clock Timing” for $F_{CH}$ and $F_{CL}$.
- See “17.4. AC Characteristics: 17.4.2. Source Clock/Machine Clock” for $F_{MP}$ and $F_{MPL}$.

*4: $V_{CC}$ = 5.0 V, $T_A$ = +25°C

**Input waveform generated when an external clock (main clock) is used**

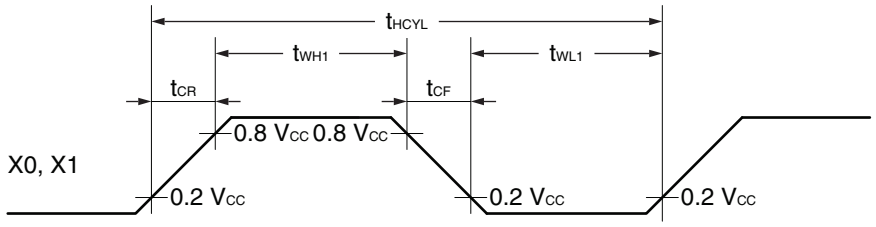
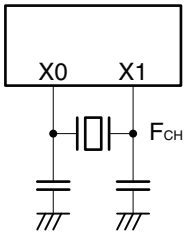
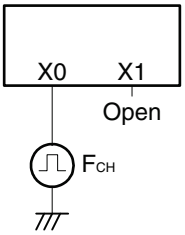



**Figure of main clock input port external connection**

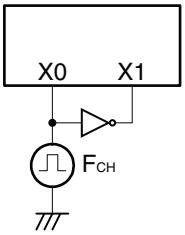
When a crystal oscillator or a ceramic oscillator is used




When the external clock is used (X1 is open)




When the external clock is used




**Input waveform generated when an external clock (subclock) is used**

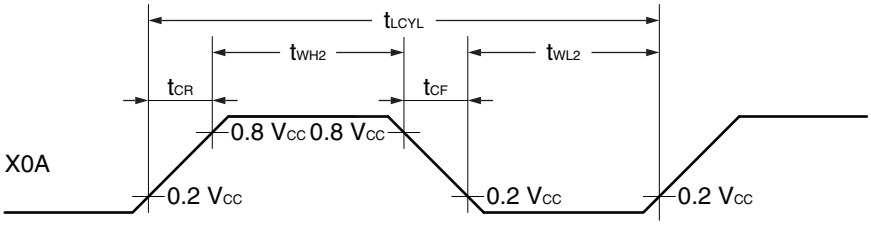
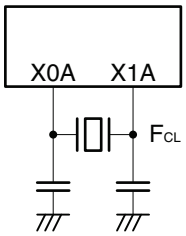
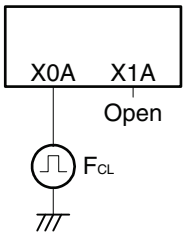



**Figure of subclock input port external connection**

When a crystal oscillator or a ceramic oscillator is used




When the external clock is used



### 17.4.2 Source Clock/Machine Clock

($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = 0.0 V, $T_A$ = -40°C to +85°C)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Source clock cycle time*1 | $t_{SCLK}$ | — | 61.5 | — | 2000 | ns | When the main oscillation clock is used<br>Min: $F_{CH}$ = 32.5 MHz, divided by 2<br>Max: $F_{CH}$ = 1 MHz, divided by 2 |
| | | | 61.5 | — | 2000 | ns | When the main oscillation clock is used<br>Min: $F_{CH}$ = 8.125 MHz, multiplied by the PLL multiplier of 2<br>Max: $F_{CH}$ = 1 MHz, divided by 2 |
| | | | 80 | — | 1000 | ns | When the main CR clock is used<br>Min: $F_{CRH}$ = 12.5 MHz<br>Max: $F_{CRH}$ = 1 MHz |
| | | | — | 61 | — | µs | When the sub-oscillation clock is used<br>$F_{CL}$ = 32.768 kHz, divided by 2 |
| | | | — | 20 | — | µs | When the sub-CR clock is used<br>$F_{CRL}$ = 100 kHz, divided by 2 |
| Source clock frequency | $F_{SP}$ | — | 0.50 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | 1 | — | 12.5 | MHz | When the main CR clock is used |
| | $F_{SPL}$ | | — | 16.384 | — | kHz | When the sub-oscillation clock is used |
| | | | — | 50 | — | kHz | When the sub-CR clock is used<br>$F_{CRL}$ = 100 kHz, divided by 2 |
| Machine clock cycle time*2 (minimum instruction execution time) | $t_{MCLK}$ | — | 61.5 | — | 32000 | ns | When the main oscillation clock is used<br>Min: $F_{SP}$ = 16.25 MHz, no division<br>Max: $F_{SP}$ = 0.5 MHz, divided by 16 |
| | | | 80 | — | 16000 | ns | When the main CR clock is used<br>Min: $F_{SP}$ = 12.5 MHz<br>Max: $F_{SP}$ = 1 MHz, divided by 16 |
| | | | 61 | — | 976.5 | µs | When the sub-oscillation clock is used<br>Min: $F_{SPL}$ = 16.384 kHz, no division<br>Max: $F_{SPL}$ = 16.384 kHz, divided by 16 |
| | | | 20 | — | 320 | µs | When the sub-CR clock is used<br>Min: $F_{SPL}$ = 50 kHz, no division<br>Max: $F_{SPL}$ = 50 kHz, divided by 16 |
| Machine clock frequency | $F_{MP}$ | — | 0.031 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | 0.0625 | — | 12.5 | MHz | When the main CR clock is used |
| | $F_{MPL}$ | | 1.024 | — | 16.384 | kHz | When the sub-oscillation clock is used |
| | | | 3.125 | — | 50 | kHz | When the sub-CR clock is used<br>$F_{CRL}$ = 100 kHz |

*1: This is the clock before it is divided according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1, DIV0). This source clock is divided to become a machine clock according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1, DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- PLL multiplication of main clock (select from 2, 2.5, 4 multiplication)
- Main CR clock divided by 2
- Subclock divided by 2
- Sub-CR clock divided by 2

*(Continued)*

### 17.4.3 External Reset

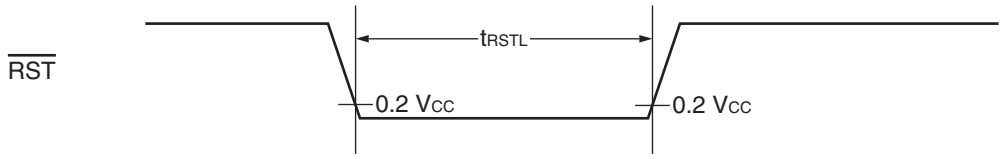
($V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = 0.0 V, $T_A$ = -40°C to +85°C)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $\overline{RST}$ "L" level pulse width | $t_{RSTL}$ | 2 $t_{MCLK}$*1 | — | ns | In normal operation |
| | | Oscillation time of the oscillator*2 + 100 | — | µs | In stop mode, subclock mode, subsleep mode, watch mode, and power-on |
| | | 100 | — | µs | In time-base timer mode |

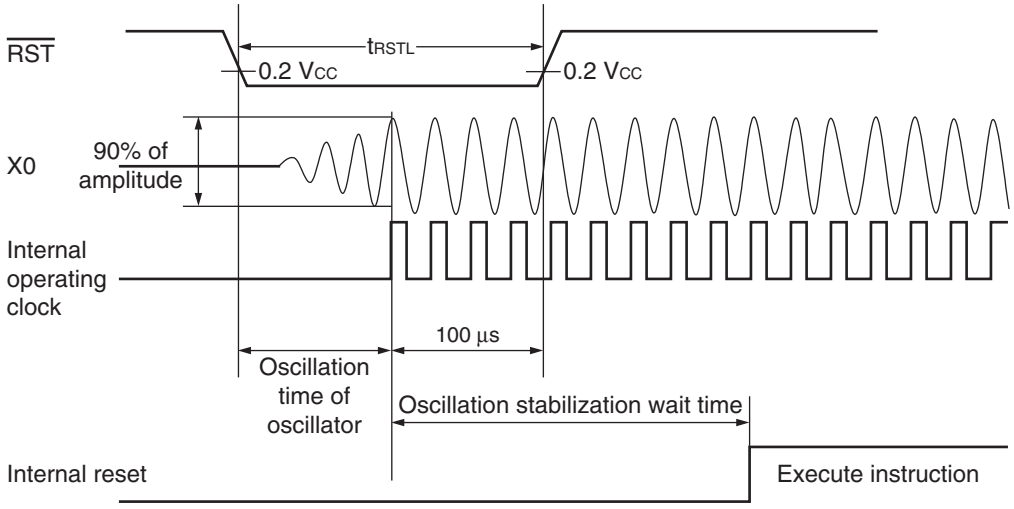
*1: See "17.4.2. Source Clock/Machine Clock" for $t_{MCLK}$.

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

**In normal operation**




**In stop mode, subclock mode, subsleep mode, watch mode and power-on**



### 17.4.8 $I^2C$ Timing

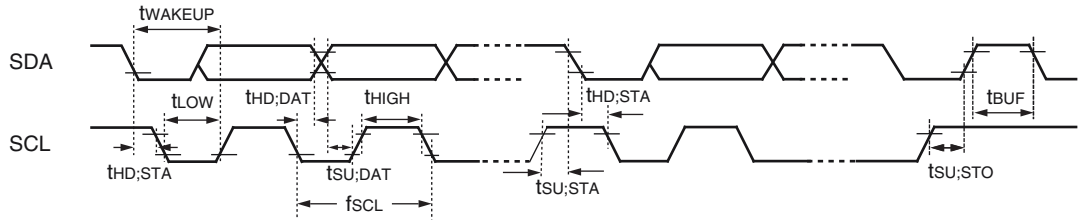
($V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = -40°C to +85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Standard-mode | | Fast-mode | | |
| | | | | Min | Max | Min | Max | |
| SCL clock frequency | $f_{SCL}$ | SCL | R = 1.7 kΩ, C = 50 pF*1 | 0 | 100 | 0 | 400 | kHz |
| (Repeat) Start condition hold time SDA ↓ → SCL ↓ | $t_{HD;STA}$ | SCL, SDA | | 4.0 | — | 0.6 | — | µs |
| SCL clock “L” width | $t_{LOW}$ | SCL | | 4.7 | — | 1.3 | — | µs |
| SCL clock “H” width | $t_{HIGH}$ | SCL | | 4.0 | — | 0.6 | — | µs |
| (Repeat) Start condition setup time SCL ↑ → SDA ↓ | $t_{SU;STA}$ | SCL, SDA | | 4.7 | — | 0.6 | — | µs |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HD;DAT}$ | SCL, SDA | | 0 | 3.45*2 | 0 | 0.9*3 | µs |
| Data setup time SDA ↓ ↑ → SCL ↑ | $t_{SU;DAT}$ | SCL, SDA | | 0.25 | — | 0.1 | — | µs |
| Stop condition setup time SCL ↑ → SDA ↑ | $t_{SU;STO}$ | SCL, SDA | | 4.0 | — | 0.6 | — | µs |
| Bus free time between stop condition and start condition | $t_{BUF}$ | SCL, SDA | | 4.7 | — | 1.3 | — | µs |

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” ($t_{LOW}$) does not extend.

*3: A Fast-mode $I^2C$-bus device can be used in a Standard-mode $I^2C$-bus system, provided that the condition of $t_{SU;DAT}$ ≥ 250 ns is fulfilled.




*(Continued)*

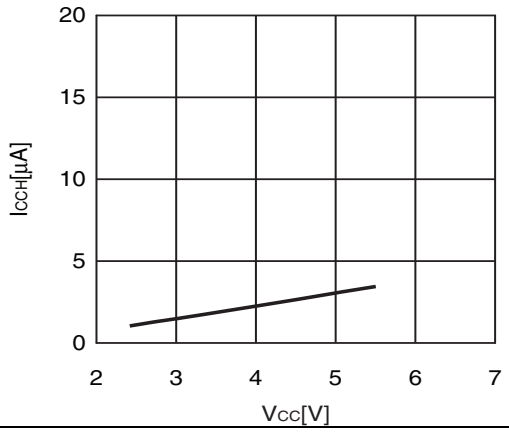
($V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = -40°C to +85°C)

| Parameter | Symbol | Pin name | Conditions | Value*2 | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCL clock “L” width | $t_{LOW}$ | SCL | R = 1.7 kΩ, C = 50 pF*1 | $(2 + nm / 2)t_{MCLK} - 20$ | — | ns | Master mode |
| SCL clock “H” width | $t_{HIGH}$ | SCL | | $(nm / 2)t_{MCLK} - 20$ | $(nm / 2)t_{MCLK} + 20$ | ns | Master mode |
| Start condition hold time | $t_{HD;STA}$ | SCL, SDA | | $(-1 + nm / 2)t_{MCLK} - 20$ | $(-1 + nm)t_{MCLK} + 20$ | ns | Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied. |
| Stop condition setup time | $t_{SU;STO}$ | SCL, SDA | | $(1 + nm / 2)t_{MCLK} - 20$ | $(1 + nm / 2)t_{MCLK} + 20$ | ns | Master mode |
| Start condition setup time | $t_{SU;STA}$ | SCL, SDA | | $(1 + nm / 2)t_{MCLK} - 20$ | $(1 + nm / 2)t_{MCLK} + 20$ | ns | Master mode |
| Bus free time between stop condition and start condition | $t_{BUF}$ | SCL, SDA | | $(2 nm + 4)t_{MCLK} - 20$ | — | ns | |
| Data hold time | $t_{HD;DAT}$ | SCL, SDA | | $3 t_{MCLK} - 20$ | — | ns | Master mode |
| Data setup time | $t_{SU;DAT}$ | SCL, SDA | | $(-2 + nm / 2)t_{MCLK} - 20$ | $(-1 + nm / 2)t_{MCLK} + 20$ | ns | Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied. |
| Setup time between clearing interrupt and SCL rising | $t_{SU;INT}$ | SCL | | $(nm / 2)t_{MCLK} - 20$ | $(1 + nm / 2)t_{MCLK} + 20$ | ns | Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓. |
| SCL clock “L” width | $t_{LOW}$ | SCL | | $4 t_{MCLK} - 20$ | — | ns | At reception |
| SCL clock “H” width | $t_{HIGH}$ | SCL | | $4 t_{MCLK} - 20$ | — | ns | At reception |

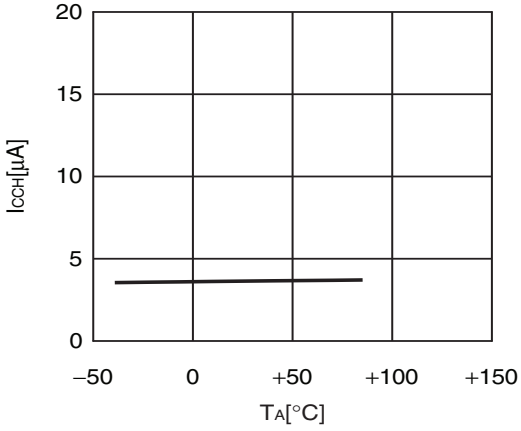
*(Continued)*

*(Continued)*

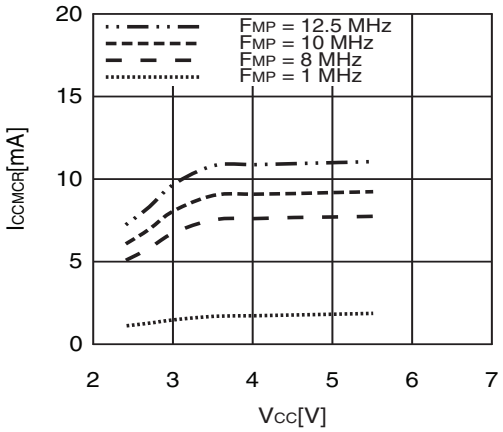
$I_{CCH}$ - $V_{CC}$
$T_A$ = +25°C, $F_{MPL}$ = (stop)
Substop mode with the external clock stopping



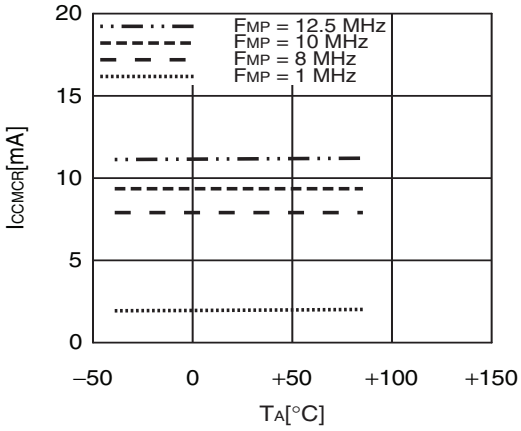

$I_{CCH}$ - $T_A$
$V_{CC}$ = 5.5 V, $F_{MPL}$ = (stop)
Substop mode with the external clock stopping



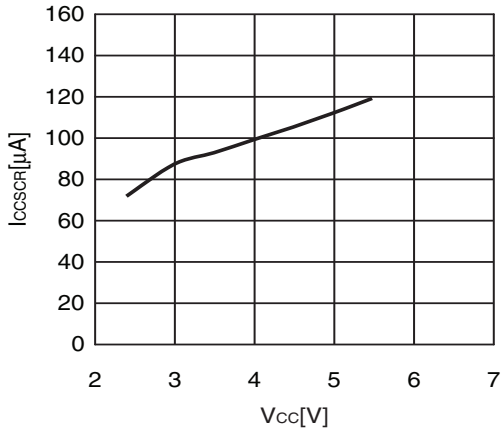

$I_{CCMCR}$ - $V_{CC}$
$T_A$ = +25°C, $F_{MP}$ = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



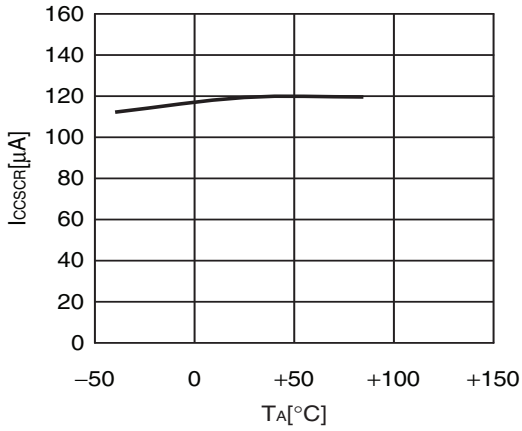

$I_{CCMCR}$ - $T_A$
$V_{CC}$ = 5.5 V, $F_{MP}$ = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating

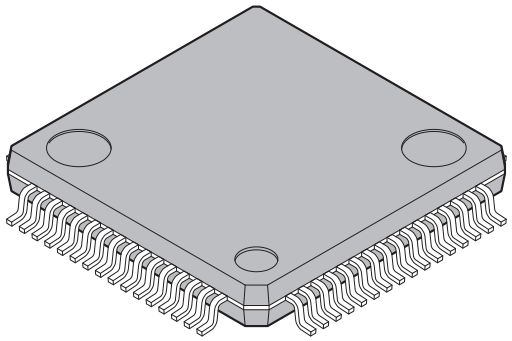



$I_{CCSCR}$ - $V_{CC}$
$T_A$ = +25°C, $F_{MPL}$ = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating



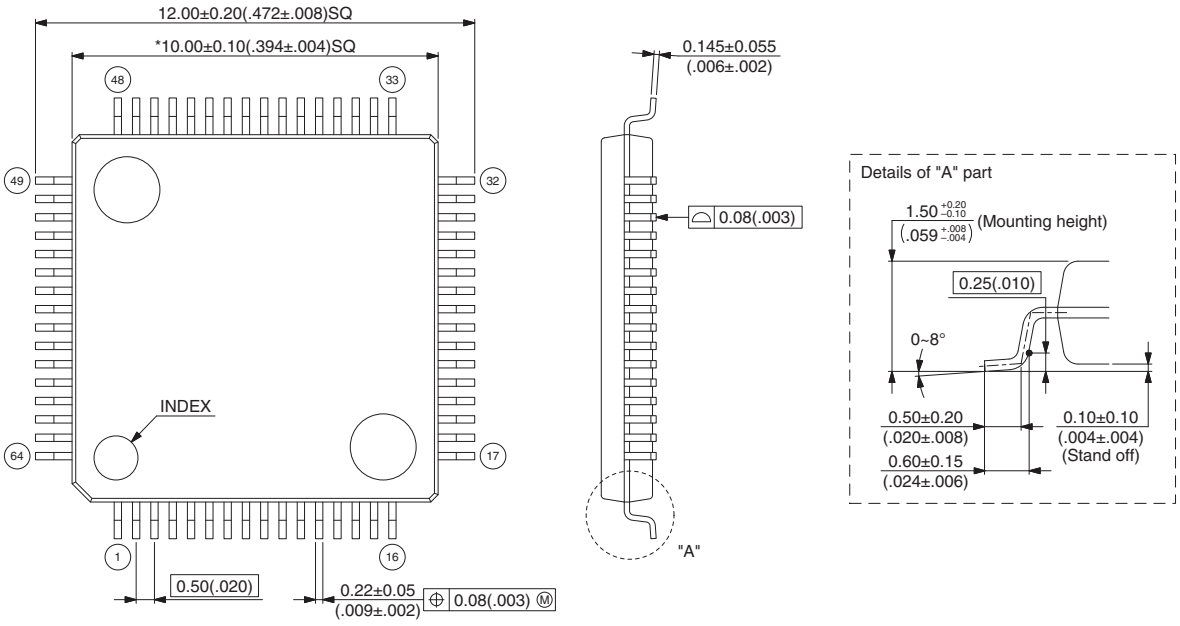

$I_{CCSCR}$ - $T_A$
$V_{CC}$ = 5.5 V, $F_{MPL}$ = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating



| 64-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width × package length | 10.00 mm × 10.00 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| (FPT-64P-M38) | Weight | 0.32 g |

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

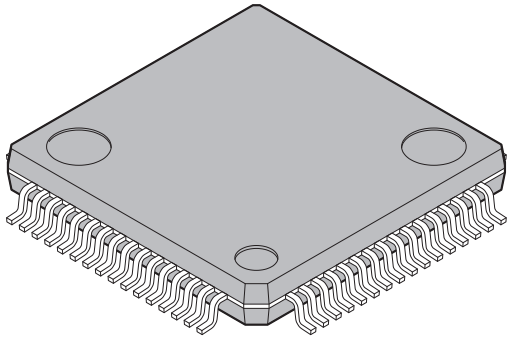





Dimensions in mm (inches).
Note: The values in parentheses are reference values.

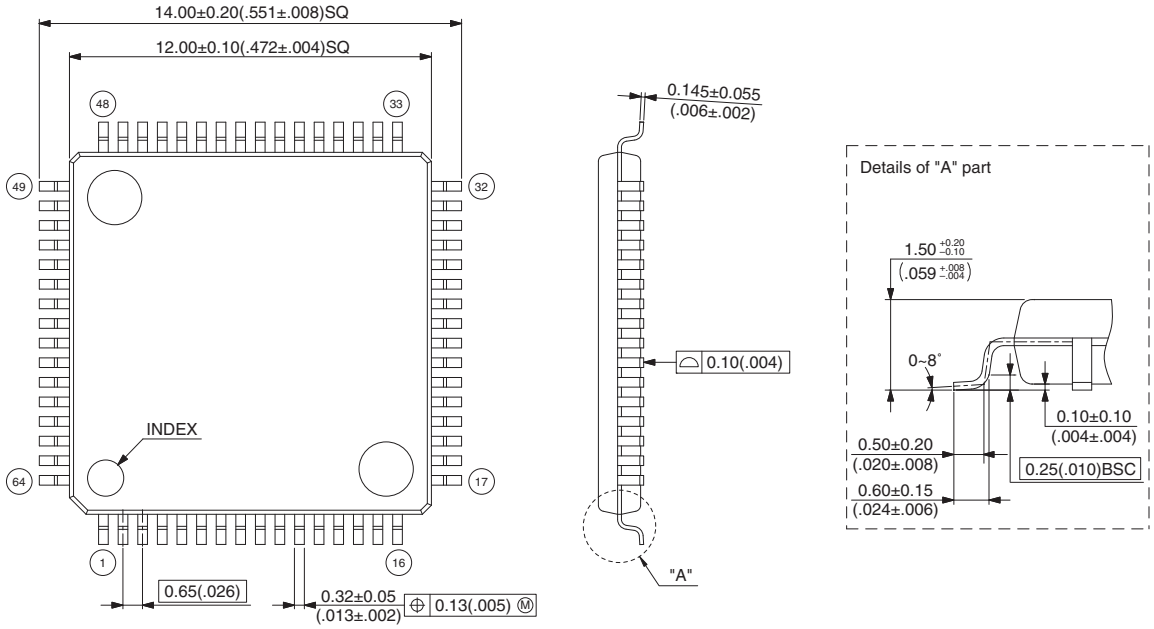
*(Continued)*

*(Continued)*

| 64-pin plastic LQFP | | |
|---|---|---|
|  (FPT-64P-M39) | Lead pitch | 0.65 mm |
| | Package width × package length | 12.00 mm × 12.00 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.47 g |
| | | |

64-pin plastic LQFP
(FPT-64P-M39)

Note 1) Pins width and pins thickness include plating thickness.






Dimensions in mm (inches).
Note: The values in parentheses are reference values.