Infineon Technologies - MB95F478HPMC1-G-SNE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.98K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f478hpmc1-g-sne2

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Part number / Package	MB95F414H	MB95F416H	MB95F418H	MB95F414K	MB95F416K	MB95F418K
8/16-bit composite timer	2 channels					
	• Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
LCD controller (LCDC)	• COM output: 4 or 8 (selectable) • SEG output: 36 or 40 (selectable) - If the number of COM outputs is 4, the maximum number of SEG outputs is 40, and the maximum number of pixels that can be displayed 160 (4×40). - If the number of COM outputs is 8, the maximum number of SEG outputs is 36, and the maximum number of pixels that can be displayed 288 (8×36). • LCD drive power supply (bias) pins: 5 (Max)					
	• Duty LCD mode • LCD standby mode • Blinking function • Internal divider resistor whose resistance value can be selected from 10 kΩ or 100 kΩ through software • Interrupt in sync with the LCD module frame frequency • Inverted display function					
16-bit reload timer	1 channel					
	• Two clock modes and two counter operating modes can be selected • Square waveform output • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Counter operating mode: reload mode or one-shot mode can be selected					
Event counter	By configuring the 16-bit reload timer and the 8/16-bit composite timer ch. 1, event counter function can be implemented. When the event counter function is used, the 16-bit reload timer and the 8/16-bit composite timer ch. 1 are unavailable.					
8/16-bit PPG	2 channels					
	• Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel” • Counter operating clock: Eight selectable clock sources					
Watch counter	• Count clock: Four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • Counter value can be set from 0 to 63. (Capable of counting for 1 minute when the clock source is 1 second and the counter value is to 60)					
External interrupt	8 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					
Watch prescaler	Eight different time intervals can be selected. (62.5 ms, 125 ms, 250 ms, 500 ms, 1 s, 2 s, 4 s, 8 s)					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-80P-M37					

MB95470H Series

Part number / Package	MB95F474H	MB95F476H	MB95F478H	MB95F474K	MB95F476K	MB95F478K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Program ROM capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	496 bytes	1008 bytes	2032 bytes	496 bytes	1008 bytes	2032 bytes
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 58 • CMOS I/O : 55 • N-ch open drain : 3			• I/O ports (Max) : 59 • CMOS I/O : 55 • N-ch open drain : 4		
Time-base timer	Interval time: 0.256 ms - 8.3 s (external clock frequency = 4 MHz)					
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
I^2C	1 channel					
	• Master/Slave sending and receiving • Bus error function and arbitration function • Detecting transmitting direction function • Start condition repeated generation and detection functions • Built-in wake-up function					
UART/SIO	3 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
8/10-bit A/D converter	8 channels					
	8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	2 channels					
	• Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					

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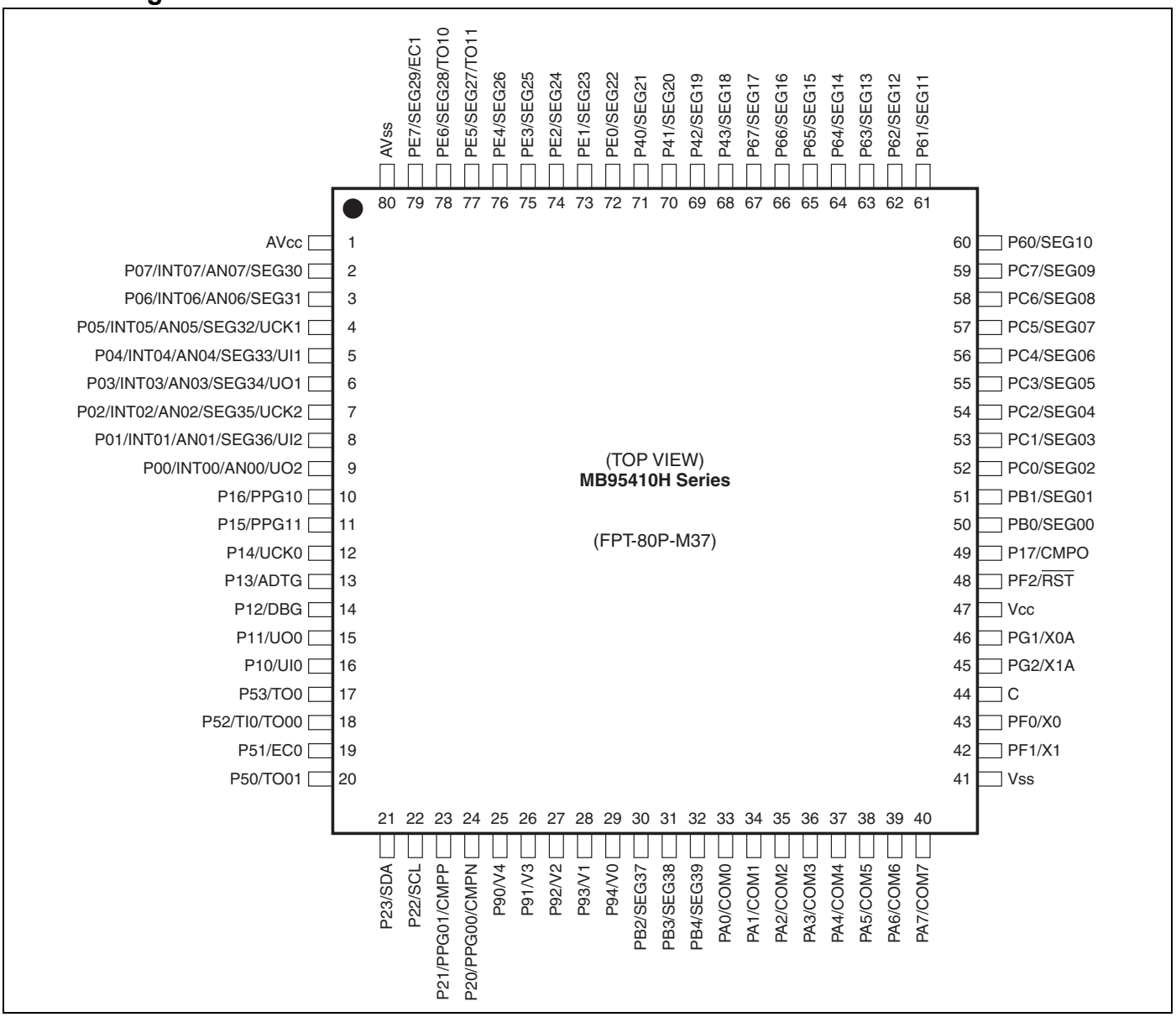
5. Pin Assignment



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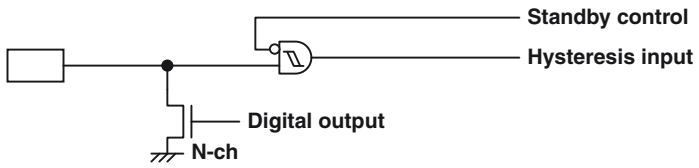
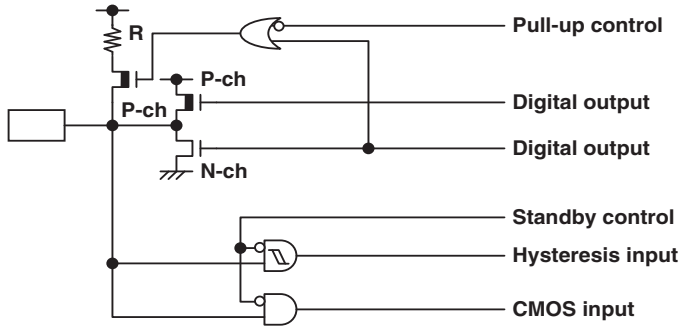
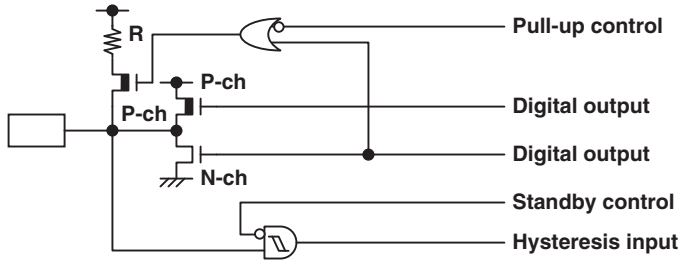
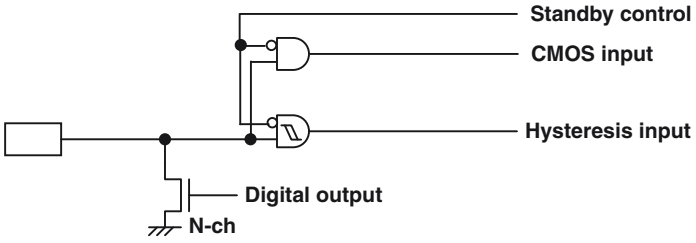
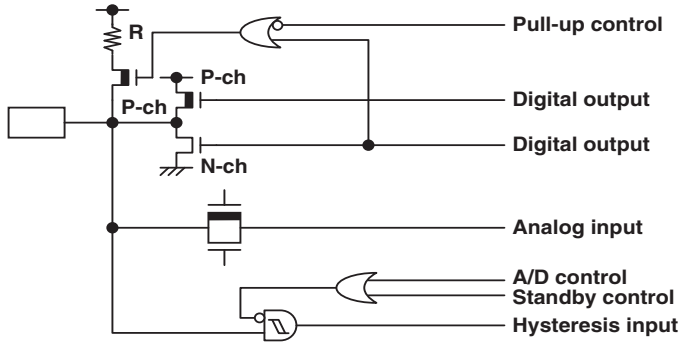
Type	Circuit	Remarks
D		• N-ch open drain output • Hysteresis input
G		• CMOS output • Hysteresis input • CMOS input • Pull-up control available
H		• CMOS output • Hysteresis input • Pull-up control available
I		• N-ch open drain output • CMOS input • Hysteresis input
J		• CMOS output • Hysteresis input • Analog input • Pull-up control available

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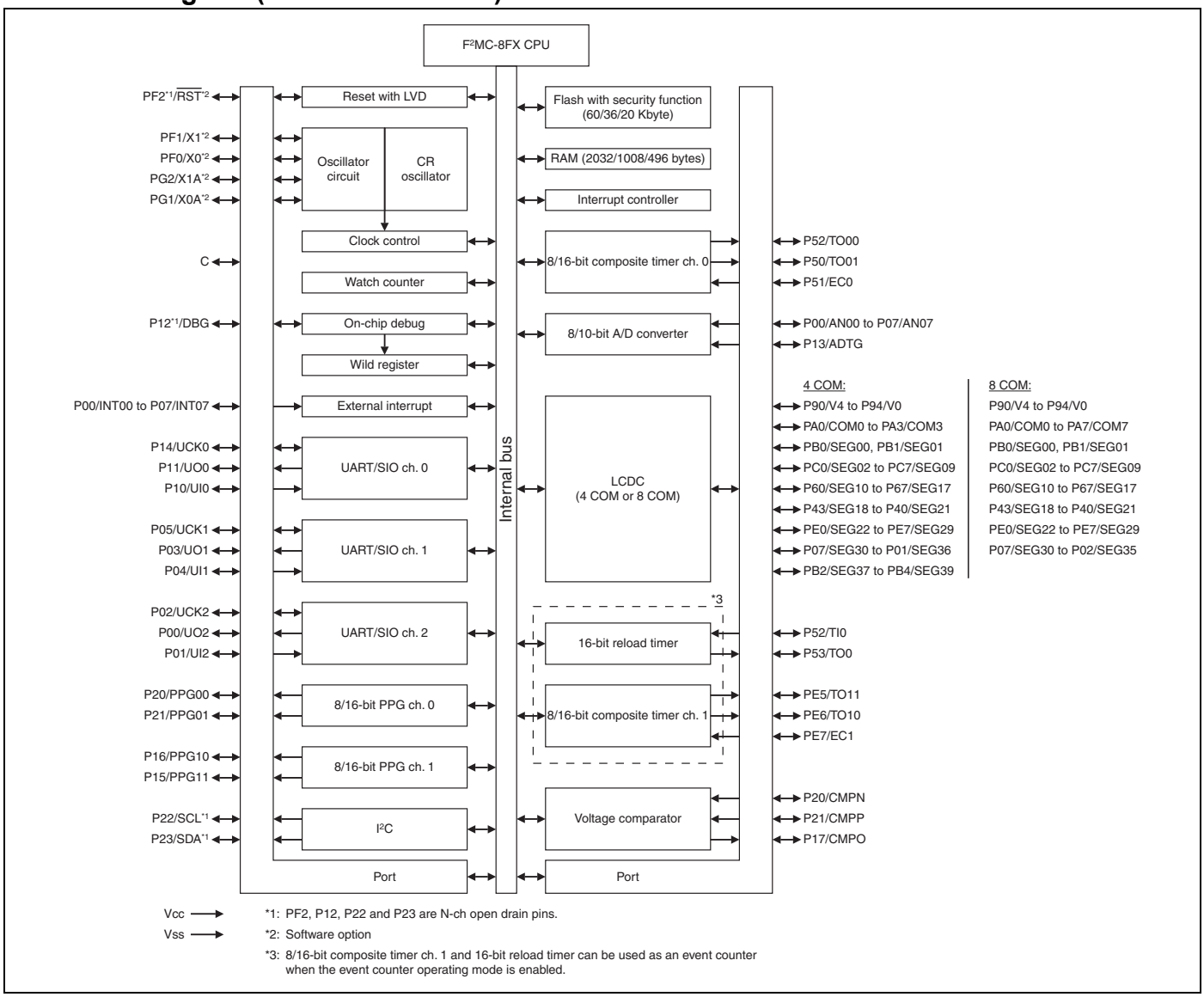
11. Block Diagram (MB95410H Series)



Address	Register abbreviation	Register name	R/W	Initial value
$005F_H$	RDR1	UART/SIO serial input data register ch. 1	R	00000000_B
0060_H	IBCR00	I^2C bus control register 0	R/W	00000001_B
0061_H	IBCR10	I^2C bus control register 1	R/W	00000000_B
0062_H	IBCR0	I^2C bus status register	R	00000000_B
0063_H	IDDR0	I^2C data register	R/W	00000000_B
0064_H	IAAR0	I^2C address register	R/W	00000000_B
0065_H	ICCR0	I^2C clock control register	R/W	00000000_B
0066_H	SMC12	UART/SIO serial mode control register 1 ch. 2	R/W	00000000_B
0067_H	SMC22	UART/SIO serial mode control register 2 ch. 2	R/W	00100000_B
0068_H	SSR2	UART/SIO serial status register ch. 2	R/W	00000001_B
0069_H	TDR2	UART/SIO serial output data register ch. 2	R/W	00000000_B
$006A_H$	RDR2	UART/SIO serial input data register ch. 2	R	00000000_B
$006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register upper	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register lower	R/W	00000000_B
0070_H	WCSR	Watch counter status register	R/W	00000000_B
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	00000000_B
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B

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17. Electrical Characteristics

17.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	−2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{CL}	—	15	mA	
“L” level average current	I_{CLAV}	—	4	mA	Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{CH}	—	−15	mA	
“H” level average current	I_{CHAV}	—	−4	mA	Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	−100	mA	
“H” level total average output current	ΣI_{OHAV}	—	−50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	T_{stg}	−55	+150	°C	

*1: These parameters are based on the condition that V_{SS} = 0.0 V.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

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17.3 DC Characteristics

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P01, P04, P10, P22, P23	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level (hysteresis input) is selected
	V_{IHS}	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P01, P04, P10, P22, P23	*1	V_{SS} − 0.3	—	0.3 V_{CC}	V	When CMOS input level (hysteresis input) is selected
	V_{ILS}	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, P22, P23, PF2	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P12, P22, P23, PF2	I_{OH} = −4 mA	V_{CC} − 0.5	—	—	V	

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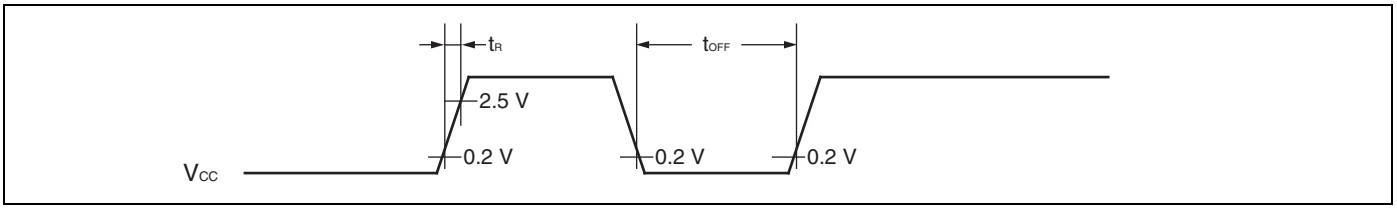
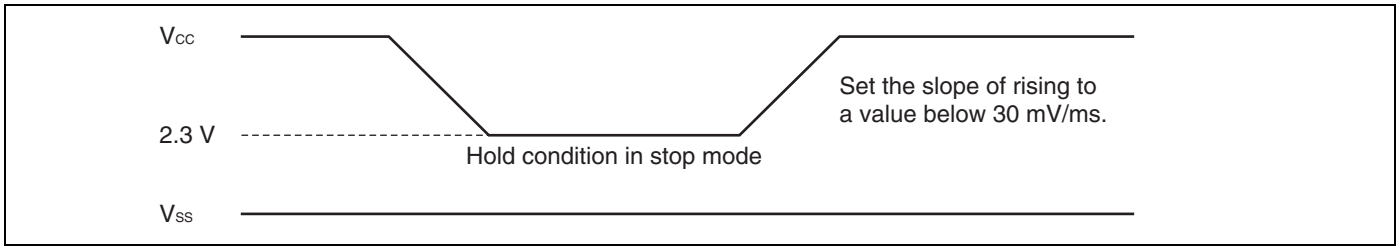
17.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

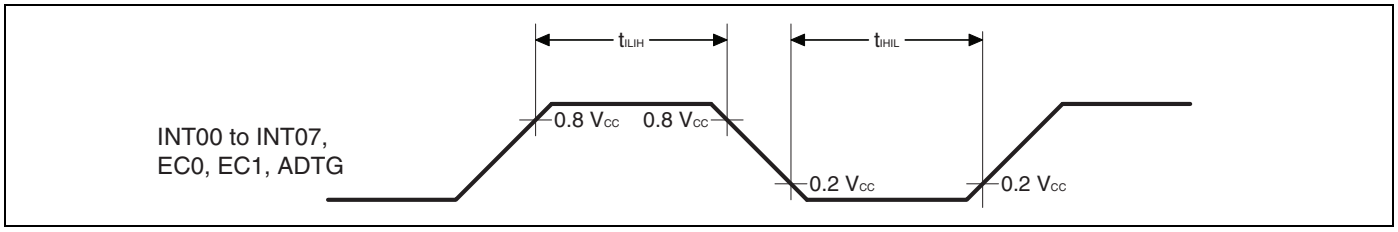


17.4.5 Peripheral Input Timing

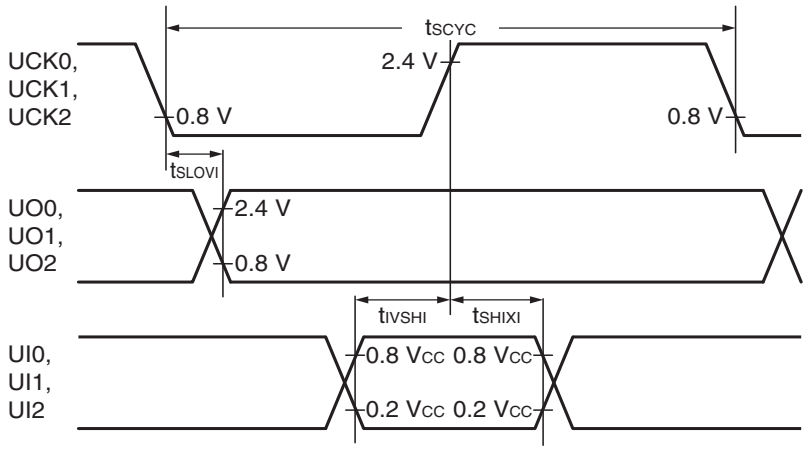
(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, ADTG	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

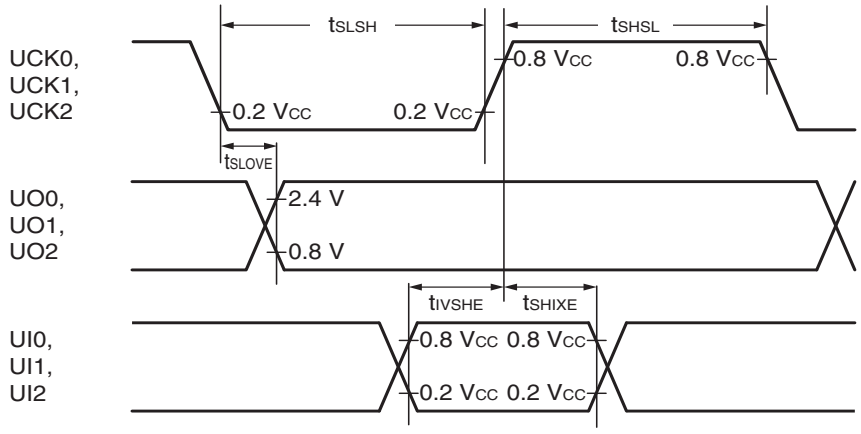
*: See “17.4.2. Source Clock/Machine Clock” for t_{MCLK}.



Internal shift clock mode



External shift clock mode



17.4.8 I^2C Timing

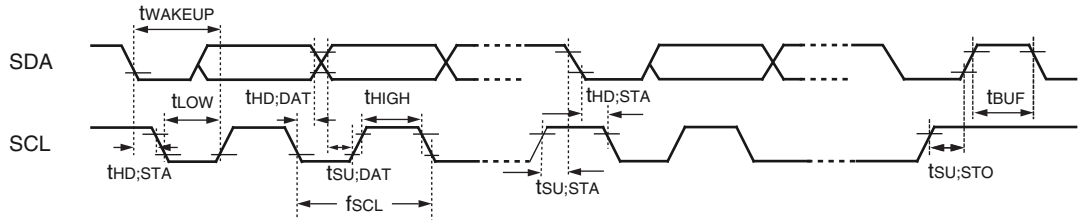
(V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) Start condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL, SDA		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL		4.0	—	0.6	—	µs
(Repeat) Start condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL, SDA		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HD;DAT}$	SCL, SDA		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SU;DAT}$	SCL, SDA		0.25	—	0.1	—	µs
Stop condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL, SDA		4.0	—	0.6	—	µs
Bus free time between stop condition and start condition	t_{BUF}	SCL, SDA		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” (t_{LOW}) does not extend.

*3: A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, provided that the condition of $t_{SU;DAT}$ ≥ 250 ns is fulfilled.



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(V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm / 2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL		$(nm / 2)t_{MCLK} - 20$	$(nm / 2)t_{MCLK} + 20$	ns	Master mode
Start condition hold time	$t_{HD;STA}$	SCL, SDA		$(-1 + nm / 2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
Stop condition setup time	$t_{SU;STO}$	SCL, SDA		$(1 + nm / 2)t_{MCLK} - 20$	$(1 + nm / 2)t_{MCLK} + 20$	ns	Master mode
Start condition setup time	$t_{SU;STA}$	SCL, SDA		$(1 + nm / 2)t_{MCLK} - 20$	$(1 + nm / 2)t_{MCLK} + 20$	ns	Master mode
Bus free time between stop condition and start condition	t_{BUF}	SCL, SDA		$(2 nm + 4)t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL, SDA		$3 t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		$(-2 + nm / 2)t_{MCLK} - 20$	$(-1 + nm / 2)t_{MCLK} + 20$	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL		$(nm / 2)t_{MCLK} - 20$	$(1 + nm / 2)t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓.
SCL clock “L” width	t_{LOW}	SCL		$4 t_{MCLK} - 20$	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL		$4 t_{MCLK} - 20$	—	ns	At reception

(Continued)

(Continued)

(V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
Start condition detection	$t_{HD;STA}$	SCL, SDA	R = 1.7 kΩ, C = 50 pF*1	2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Stop condition detection	$t_{SU;STO}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Restart condition detection condition	$t_{SU;STA}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL, SDA		2 t_{MCLK} − 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{LOW} − 3 t_{MCLK} − 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL, SDA		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{MCLK} − 20	—	ns	At reception
SDA↓→SCL↑ (at wakeup function)	t_{WAKEUP}	SCL, SDA		Oscillation stabilization wait time + 2 t_{MCLK} − 20	—	ns	

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2:
- See “17.4.2. Source Clock/Machine Clock” for t_{MCLK}.
- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I^2C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I^2C clock control register (ICCR0).
- The actual timing of I^2C is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS4 to CS0 bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98), (5, 22), (6, 22), (7, 22) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (8, 22) : 0.9 MHz < t_{MCLK} ≤ 16.25 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (1, 38), (6, 4), (7, 4), (8, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (5, 8) : 3.3 MHz < t_{MCLK} ≤ 16.25 MHz

17.5 A/D Converter

17.5.1 A/D Converter Electrical Characteristics

(AV_{CC} = V_{CC} = 4.0 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

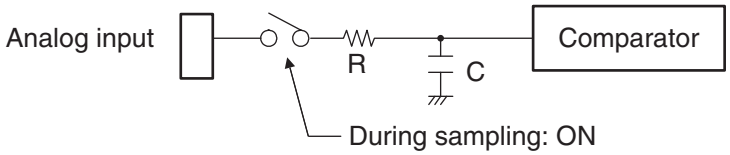
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		−3	—	+3	LSB	
Linearity error		−2.5	—	+2.5	LSB	
Differential linear error		−1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	AV_{CC} − 4.5 LSB	AV_{CC} − 2 LSB	AV_{CC} + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ V_{CC} < 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I_{AIN}	−0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	AV_{SS}	—	AV_{CC}	V	

17.5.2 Notes on Using the A/D Converter

External impedance of analog input and its sampling time

The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

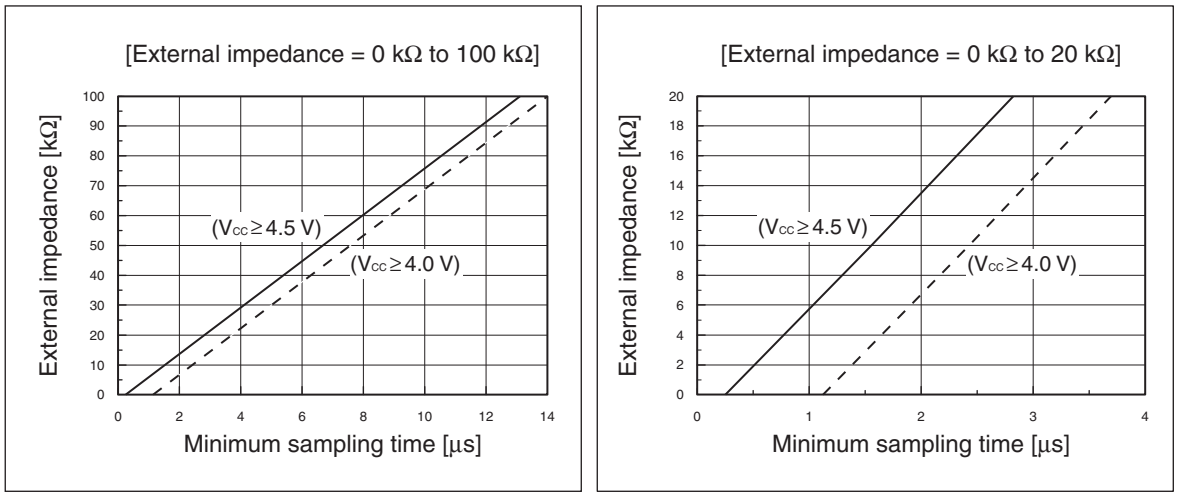
Analog input equivalent circuit



V_{CC}	R	C
4.5 V ≤ V_{CC} ≤ 5.5 V	1.95 kΩ (Max)	17 pF (Max)
4.0 V ≤ V_{CC} < 4.5 V	8.98 kΩ (Max)	17 pF (Max)

Note: The values are reference values.

Relationship between external impedance and minimum sampling time



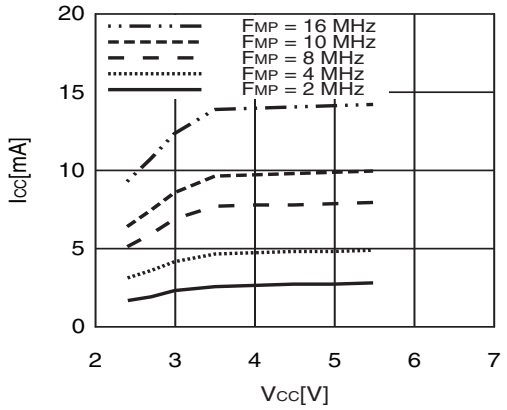
A/D conversion error

As $|V_{CC}–V_{SS}|$ decreases, the A/D conversion error increases proportionately.

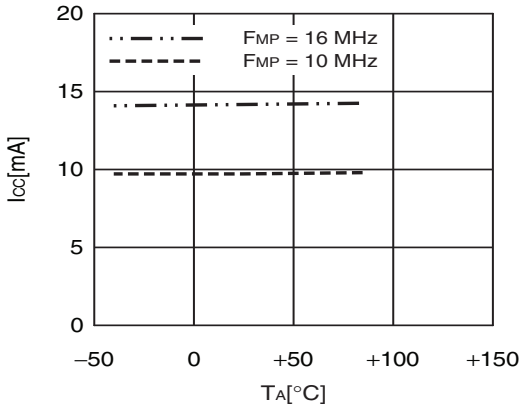
18. Sample Characteristics

Power supply current temperature characteristics

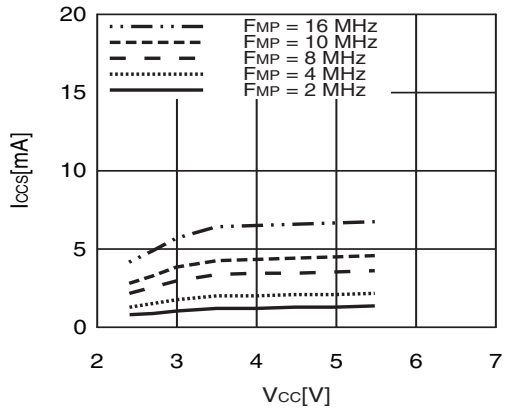
I_{CC} - V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



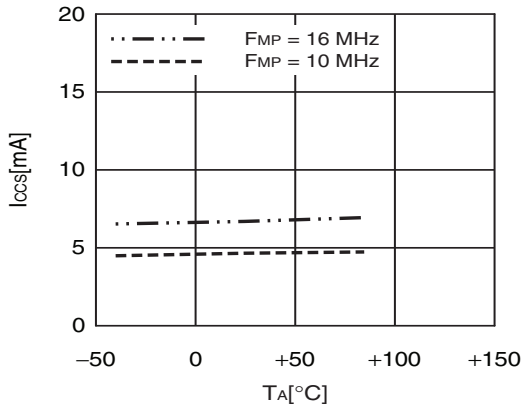
I_{CC} - T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



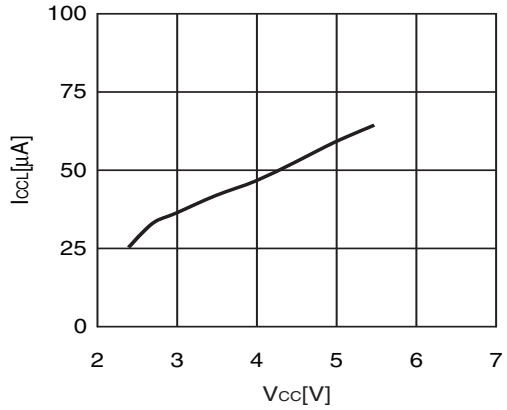
I_{CCS} - V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



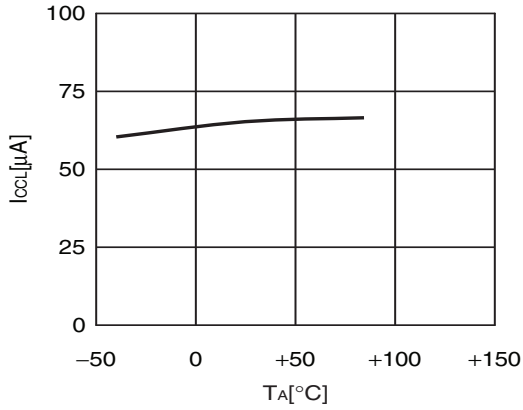
I_{CCS} - T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



I_{CCL} - V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



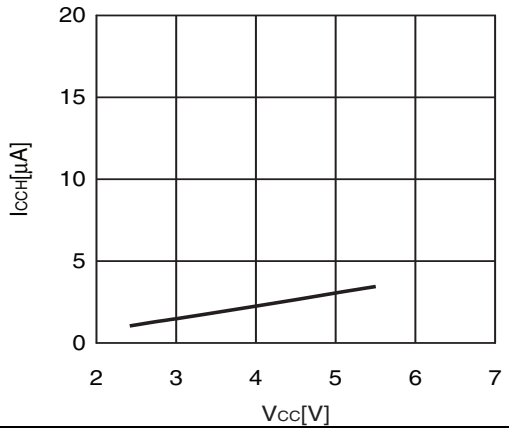
I_{CCL} - T_A
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



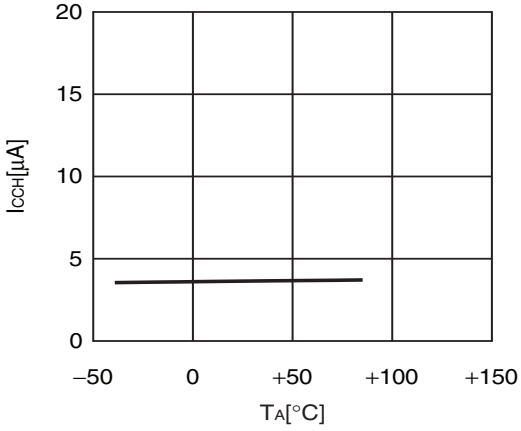
(Continued)

(Continued)

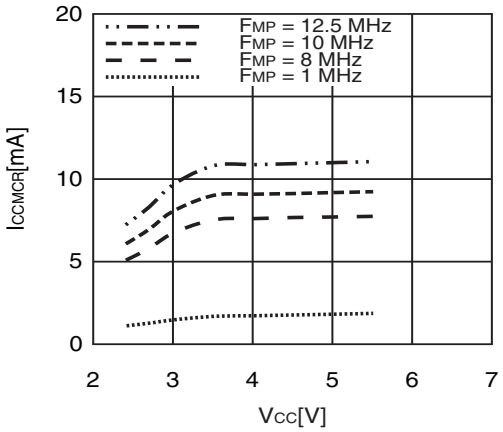
I_{CCH} - V_{CC}
T_A = +25°C, F_{MPL} = (stop)
Substop mode with the external clock stopping



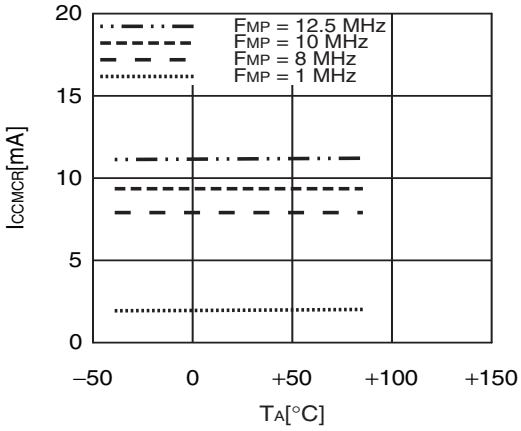
I_{CCH} - T_A
V_{CC} = 5.5 V, F_{MPL} = (stop)
Substop mode with the external clock stopping



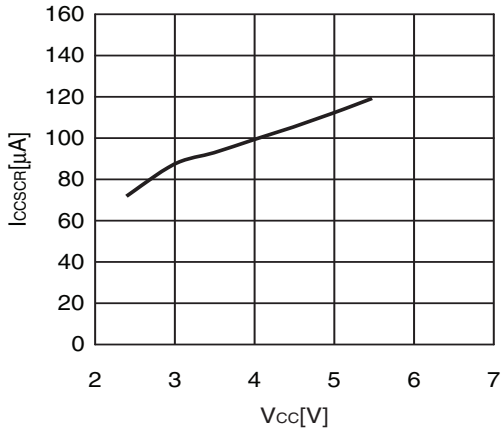
I_{CCMCR} - V_{CC}
T_A = +25°C, F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



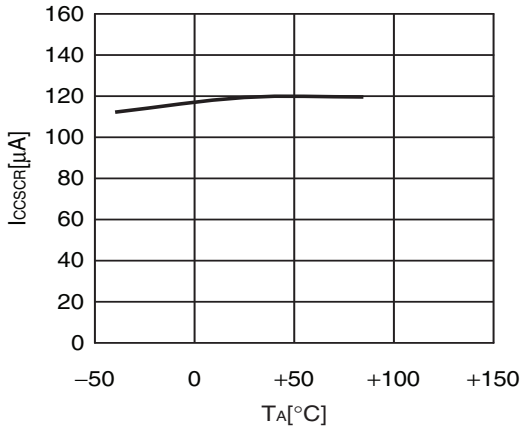
I_{CCMCR} - T_A
V_{CC} = 5.5 V, F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



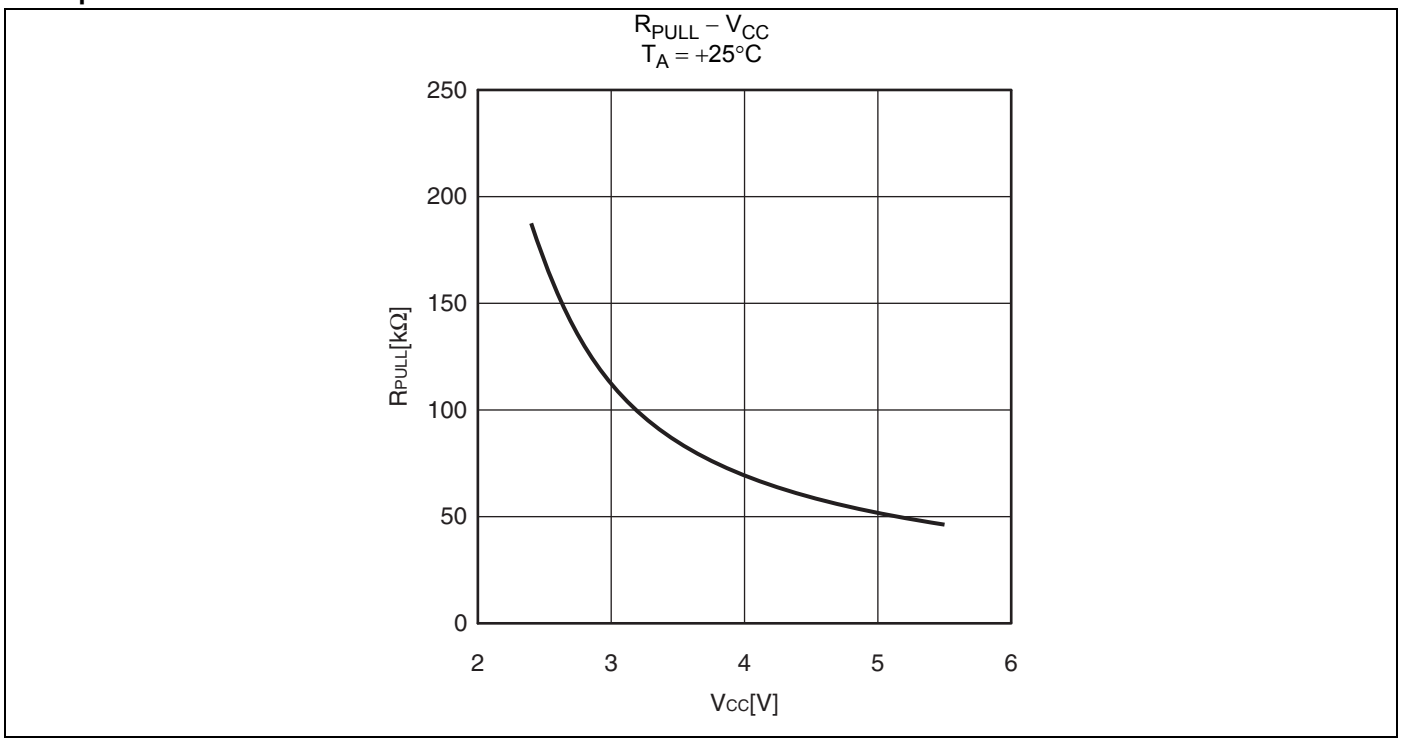
I_{CCSCR} - V_{CC}
T_A = +25°C, F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating

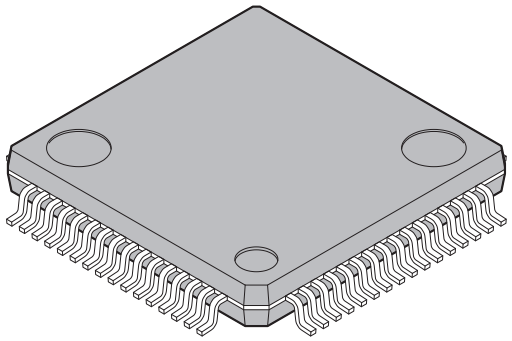


I_{CCSCR} - T_A
V_{CC} = 5.5 V, F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating



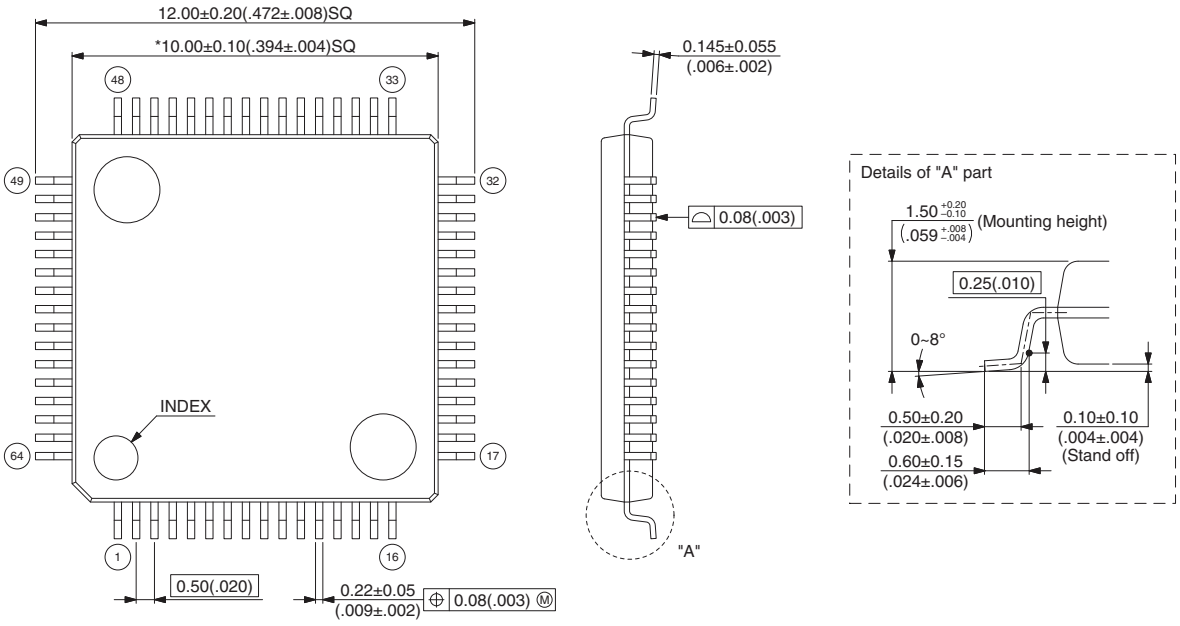
Pull-up characteristics



64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.00 mm × 10.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
(FPT-64P-M38)	Weight	0.32 g

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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