Infineon Technologies - MB95F478HPMC2-G-SNE2 Datasheet

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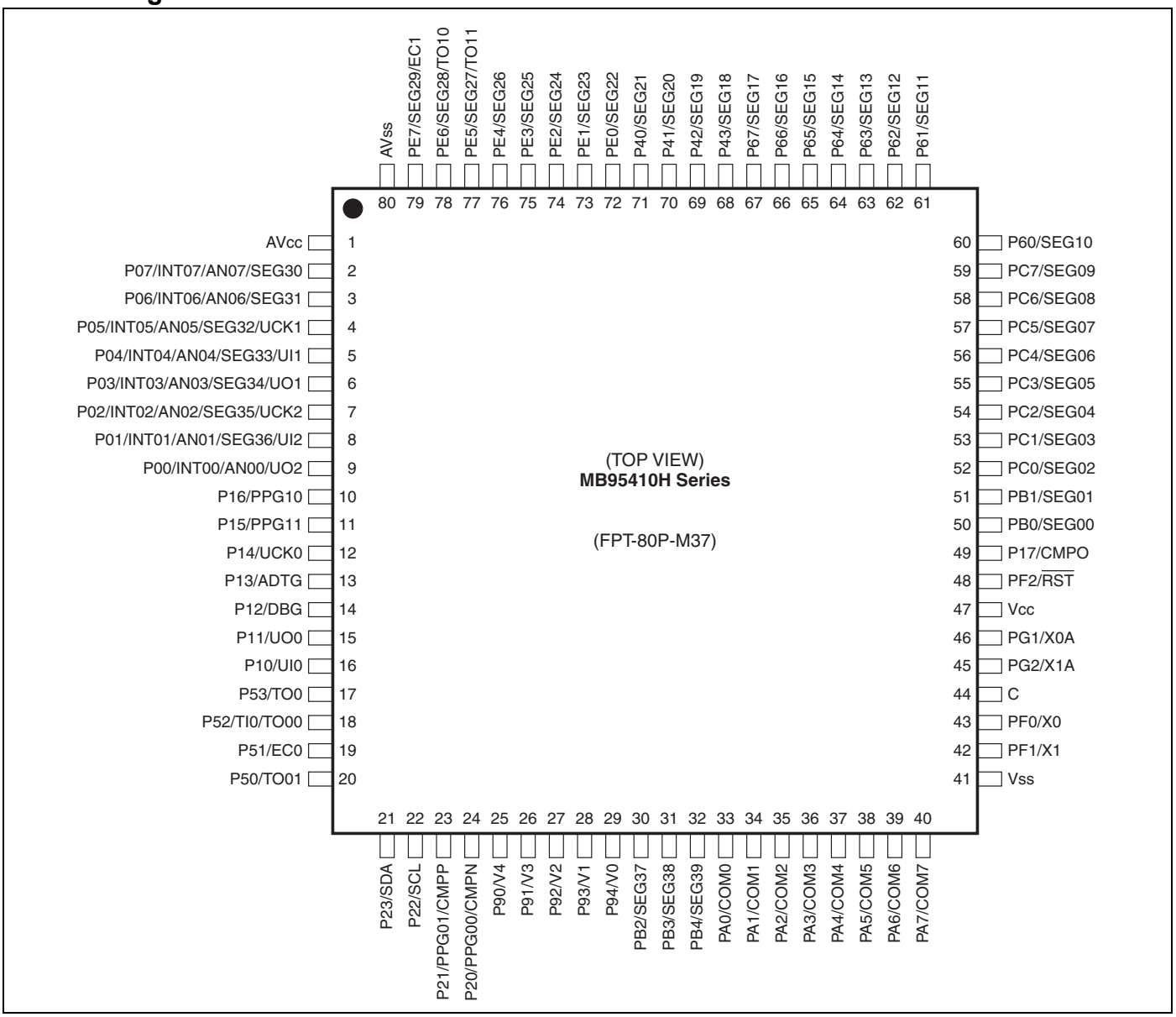
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.98K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f478hpmc2-g-sne2

5. Pin Assignment



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7. Pin Description (MB95470H Series)

Pin no.	Pin name	I/O circuit type*	Function
1	AV_{CC}	—	A/D converter power supply pin
2	P07	S	General-purpose I/O port
	INT07		External interrupt input pin
	AN07		A/D analog input pin
	SEG22		LCDC SEG output pin
3	P06	S	General-purpose I/O port
	INT06		External interrupt input pin
	AN06		A/D analog input pin
	SEG23		LCDC SEG output pin
4	P05	S	General-purpose I/O port
	INT05		External interrupt input pin
	AN05		A/D analog input pin
	SEG24		LCDC SEG output pin
	UCK1		UART/SIO ch. 1 clock I/O pin
5	P04	V	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D analog input pin
	SEG25		LCDC SEG output pin
	UI1		UART/SIO ch. 1 data input pin
6	P03	S	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D analog input pin
	SEG26		LCDC SEG output pin
	UO1		UART/SIO ch. 1 data output pin
7	P02	S	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D analog input pin
	SEG27		LCDC SEG output pin
	UCK2		UART/SIO ch. 2 clock I/O pin
8	P01	V	General-purpose I/O port
	INT01		External interrupt input pin
	AN01		A/D analog input pin
	SEG28		LCDC SEG output pin
	TO00		8/16-bit composite timer ch. 0 output pin
	UI2		UART/SIO ch. 2 data input pin

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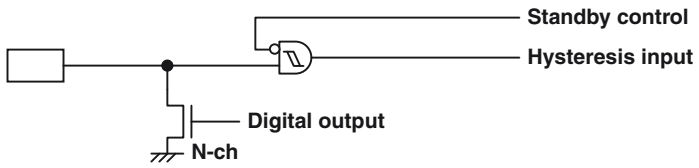
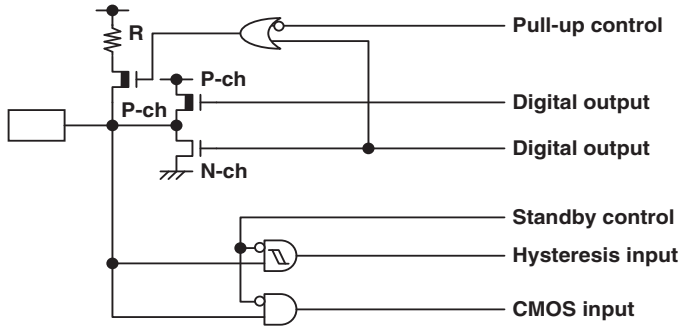
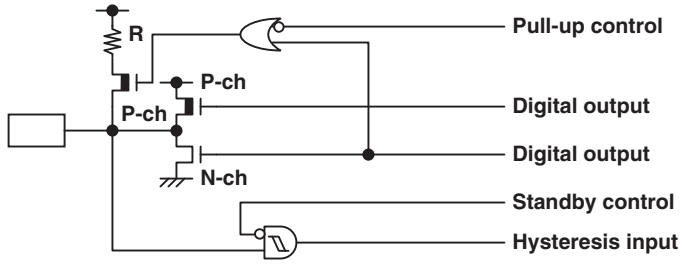
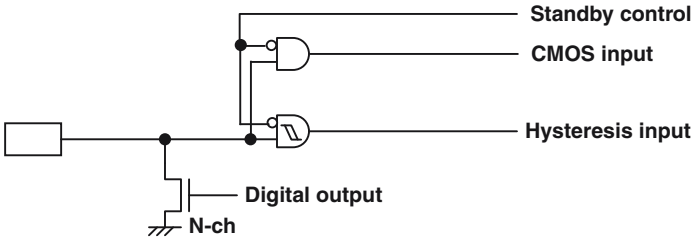
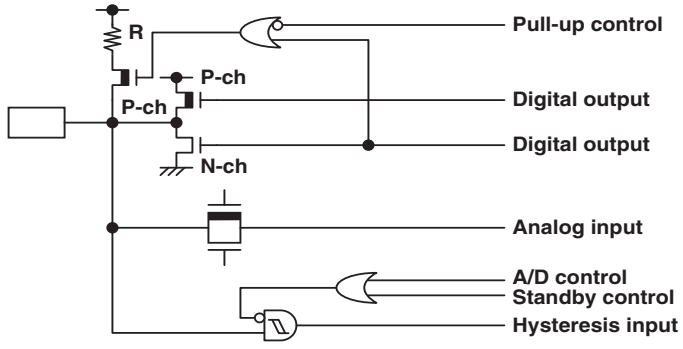
Type	Circuit	Remarks
D		• N-ch open drain output • Hysteresis input
G		• CMOS output • Hysteresis input • CMOS input • Pull-up control available
H		• CMOS output • Hysteresis input • Pull-up control available
I		• N-ch open drain output • CMOS input • Hysteresis input
J		• CMOS output • Hysteresis input • Analog input • Pull-up control available

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9. Notes on Device Handling

Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "17.1 Absolute Maximum Ratings" of “17. Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

10. Pin Connection

Treatment of unused input pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The DBG pin should not stay at “L” level after power-on until the reset output is released.

$\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin directly to an external pull-up resistor.

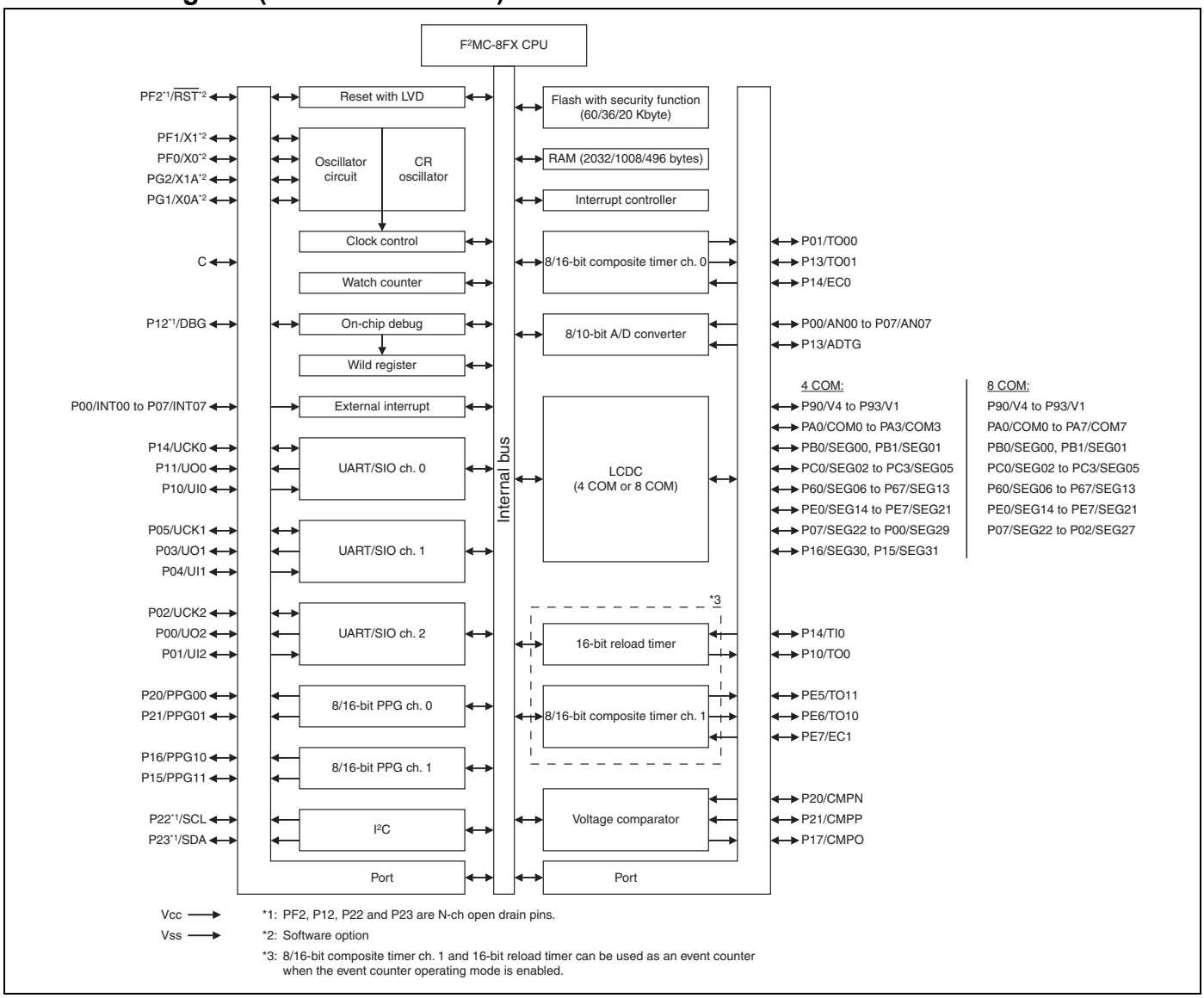
To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{\text{RST}}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The PF2/$\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output function of the PF2/$\overline{\text{RST}}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function or the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

Analog power supply

Always set the same potential to AV_{CC} and V_{CC} pins. When V_{CC} is larger than AV_{CC}, the current may flow through the AN00 to AN07 pins.

12. Block Diagram (MB95470H Series)

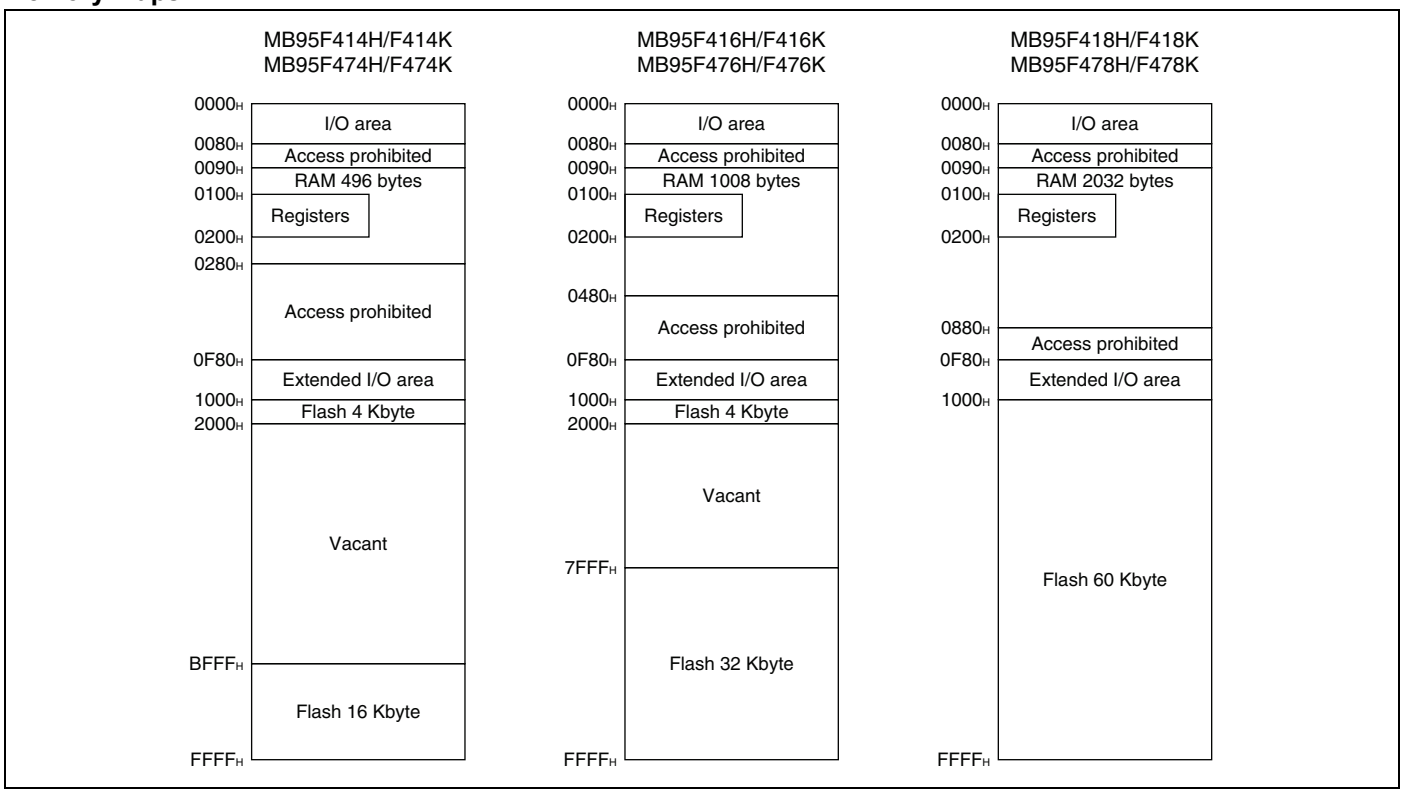


13. CPU Core

Memory Space

The memory space of the MB95410H/470H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95410H/470H Series are shown below.

Memory Maps



14. I/O Map (MB95410H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	PLLC	PLL control register	R/W	00000000_B
0007_H	SYCC	System clock control register	R/W	$XXXXXX11_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	$000XXXXX_B$
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	00000000_B
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$	PDR2	Port 2 data register	R/W	00000000_B
$000F_H$	DDR2	Port 2 direction register	R/W	00000000_B
0010_H, 0011_H	—	(Disabled)	—	—
0012_H	PDR4	Port 4 data register	R/W	00000000_B
0013_H	DDR4	Port 4 direction register	R/W	00000000_B
0014_H	PDR5	Port 5 data register	R/W	00000000_B
0015_H	DDR5	Port 5 direction register	R/W	00000000_B
0016_H	PDR6	Port 6 data register	R/W	00000000_B
0017_H	DDR6	Port 6 direction register	R/W	00000000_B
0018_H to $001B_H$	—	(Disabled)	—	—
$001C_H$	PDR9	Port 9 data register	R/W	00000000_B
$001D_H$	DDR9	Port 9 direction register	R/W	00000000_B
$001E_H$	PDRA	Port A data register	R/W	00000000_B
$001F_H$	DDRA	Port A direction register	R/W	00000000_B
0020_H	PDRB	Port B data register	R/W	00000000_B
0021_H	DDRB	Port B direction register	R/W	00000000_B
0022_H	PDRC	Port C data register	R/W	00000000_B
0023_H	DDRC	Port C direction register	R/W	00000000_B
0024_H, 0025_H	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$002D_H$	PUL1	Port 1 pull-up register	R/W	00000000_B
$002E_H$	PUL2	Port 2 pull-up register	R/W	00000000_B
$002F_H$ to 0034_H	—	(Disabled)	—	—
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000_B
0038_H	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	00000000_B
0039_H	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	00000000_B
$003A_H$	PC01	8/16-bit PPG01 control register	R/W	00000000_B
$003B_H$	PC00	8/16-bit PPG00 control register	R/W	00000000_B
$003C_H$	PC11	8/16-bit PPG11 control register	R/W	00000000_B
$003D_H$	PC10	8/16-bit PPG10 control register	R/W	00000000_B
$003E_H$	TMCSRH0	16-bit reload timer control status register upper	R/W	00000000_B
$003F_H$	TMCSRL0	16-bit reload timer control status register lower	R/W	00000000_B
0040_H to 0047_H	—	(Disabled)	—	—
0048_H	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000_B
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$ to $004E_H$	—	(Disabled)	—	—
$004F_H$	LCDCC2	LCDC control register 2	R/W	00010100_B
0050_H	CMR0	Voltage comparator control register	R/W	$000X0001_B$
0051_H to 0055_H	—	(Disabled)	—	—
0056_H	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	00000000_B
0057_H	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	00100000_B
0058_H	SSR0	UART/SIO serial status register ch. 0	R/W	00000001_B
0059_H	TDR0	UART/SIO serial output data register ch. 0	R/W	00000000_B
$005A_H$	RDR0	UART/SIO serial input data register ch. 0	R	00000000_B
$005B_H$	SMC11	UART/SIO serial mode control register 1 ch. 1	R/W	00000000_B
$005C_H$	SMC21	UART/SIO serial mode control register 2 ch. 1	R/W	00100000_B
$005D_H$	SSR1	UART/SIO serial status register ch. 1	R/W	00000001_B
$005E_H$	TDR1	UART/SIO serial output data register ch. 1	R/W	00000000_B

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Address	Register abbreviation	Register name	R/W	Initial value
$0FAC_H$	PSSR2	UART/SIO dedicated baud rate generator prescaler select register ch. 2	R/W	00000000_B
$0FAD_H$	BRSR2	UART/SIO dedicated baud rate generator baud rate setting register ch. 2	R/W	00000000_B
$0FAE_H$	—	(Disabled)	—	—
$0FAF_H$	AIDRL	A/D input disable register (lower)	R/W	00000000_B
$0FB0_H$	LCDCC1	LCDC control register 1	R/W	00000000_B
$0FB1_H$	—	(Disabled)	—	—
$0FB2_H$	LCDCE1	LCDC enable register 1	R/W	00111100_B
$0FB3_H$	LCDCE2	LCDC enable register 2	R/W	00000000_B
$0FB4_H$	LCDCE3	LCDC enable register 3	R/W	00000000_B
$0FB5_H$	LCDCE4	LCDC enable register 4	R/W	00000000_B
$0FB6_H$	LCDCE5	LCDC enable register 5	R/W	00000000_B
$0FB7_H$	LCDCE6	LCDC enable register 6	R/W	00000000_B
$0FB8_H$	—	(Disabled)	—	—
$0FB9_H$	LCDCB1	LCDC blinking setting register 1	R/W	00000000_B
$0FBA_H$	LCDCB2	LCDC blinking setting register 2	R/W	00000000_B
$0FBB_H$, $0FBC_H$	—	(Disabled)	—	—
$0FBD_H$ to $0FD8_H$	LCDRAM	LCDC display RAM (28 bytes)	R/W	00000000_B
$0FD9_H$ to $0FE1_H$	—	(Disabled)	—	—
$0FE2_H$	EVCR	Event counter control register	R/W	00000000_B
$0FE3_H$	WCDR	Watch counter data register	R/W	00111111_B
$0FE4_H$	CRTH	Main CR clock trimming register (upper)	R/W	$0XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (lower)	R/W	$00XXXXXX_B$
$0FE6_H$, $0FE7_H$	—	(Disabled)	—	—
$0FE8_H$	SYSC	System configuration register	R/W	11000011_B
$0FE9_H$	CMCR	Clock monitoring control register	R/W	$XX000000_B$
$0FEA_H$	CMDR	Clock monitoring data register	R	00000000_B
$0FEB_H$	WDTH	Watchdog timer selection ID register (upper)	R	$XXXXXXXX_B$
$0FEC_H$	WDTL	Watchdog timer selection ID register (lower)	R	$XXXXXXXX_B$

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17.3 DC Characteristics

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P01, P04, P10, P22, P23	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level (hysteresis input) is selected
	V_{IHS}	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P01, P04, P10, P22, P23	*1	V_{SS} − 0.3	—	0.3 V_{CC}	V	When CMOS input level (hysteresis input) is selected
	V_{ILS}	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, P22, P23, PF2	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P12, P22, P23, PF2	I_{OH} = −4 mA	V_{CC} − 0.5	—	—	V	

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17.4 AC Characteristics

17.4.1 Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

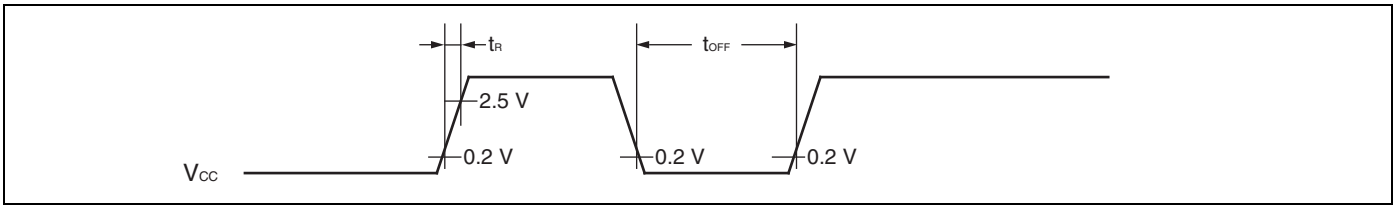
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1: open	1	—	12	MHz	When the main external clock is used
		X0, X1	*	1	—	32.5	MHz	
			—	3	—	8.13	MHz	Main PLL multiplied by 2
			—	3	—	6.5	MHz	Main PLL multiplied by 2.5
			—	3	—	4.06	MHz	Main PLL multiplied by 4
	F_{CRH}	—	—	12.25	12.5	12.75	MHz	Operating conditions: • The main CR clock is used. • T_A = −10°C to +85°C
				9.8	10	10.2	MHz	
				7.84	8	8.16	MHz	
				0.98	1	1.02	MHz	
		—	—	12.1875	12.5	12.8125	MHz	Operating conditions: • The main CR clock is used. • T_A = −40°C to −10°C
				9.75	10	10.25	MHz	
				7.8	8	8.2	MHz	
				0.975	1	1.025	MHz	
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub-oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	200	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1: open	83.4	—	1000	ns	When the external clock is used
		X0, X1	*	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1} t_{WL1}	X0	X1: open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	*	12.4	—	—	ns	
	t_{WH2} t_{WL2}	X0A	—	—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0	X1: open	—	—	5	ns	When the external clock is used
		X0, X1	*	—	—	5	ns	
CR oscillation start time	t_{CRHWK}	—	—	—	—	80	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	10	µs	When the sub-CR clock is used

*: The external clock signal is input to X0 and the inverted external clock signal to X1.

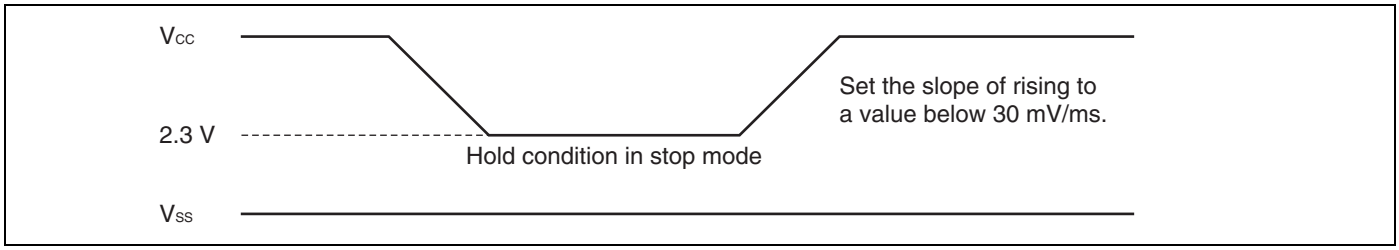
17.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

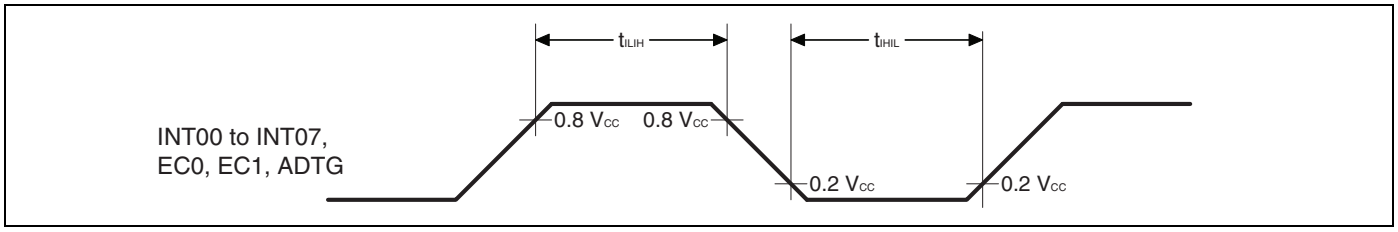


17.4.5 Peripheral Input Timing

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, ADTG	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

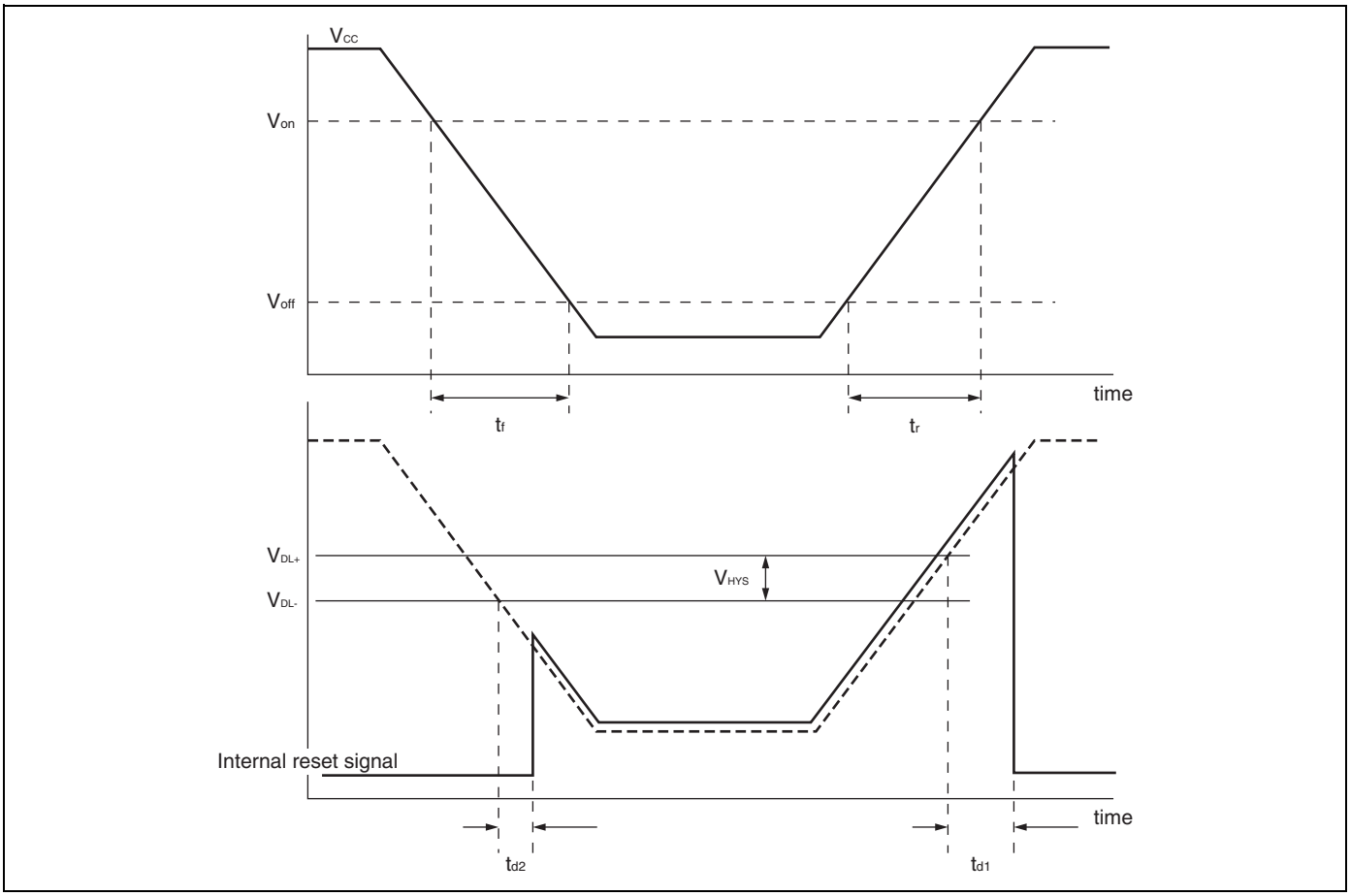
*: See “17.4.2. Source Clock/Machine Clock” for t_{MCLK}.



17.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V_{DL-}	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	3000	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	300	µs	
Reset detection delay time	t_{d2}	—	—	20	µs	



17.5 A/D Converter

17.5.1 A/D Converter Electrical Characteristics

(AV_{CC} = V_{CC} = 4.0 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

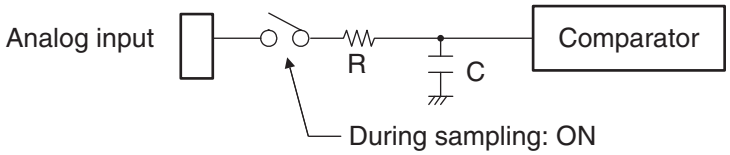
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		−3	—	+3	LSB	
Linearity error		−2.5	—	+2.5	LSB	
Differential linear error		−1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	AV_{CC} − 4.5 LSB	AV_{CC} − 2 LSB	AV_{CC} + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ V_{CC} < 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I_{AIN}	−0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	AV_{SS}	—	AV_{CC}	V	

17.5.2 Notes on Using the A/D Converter

External impedance of analog input and its sampling time

The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

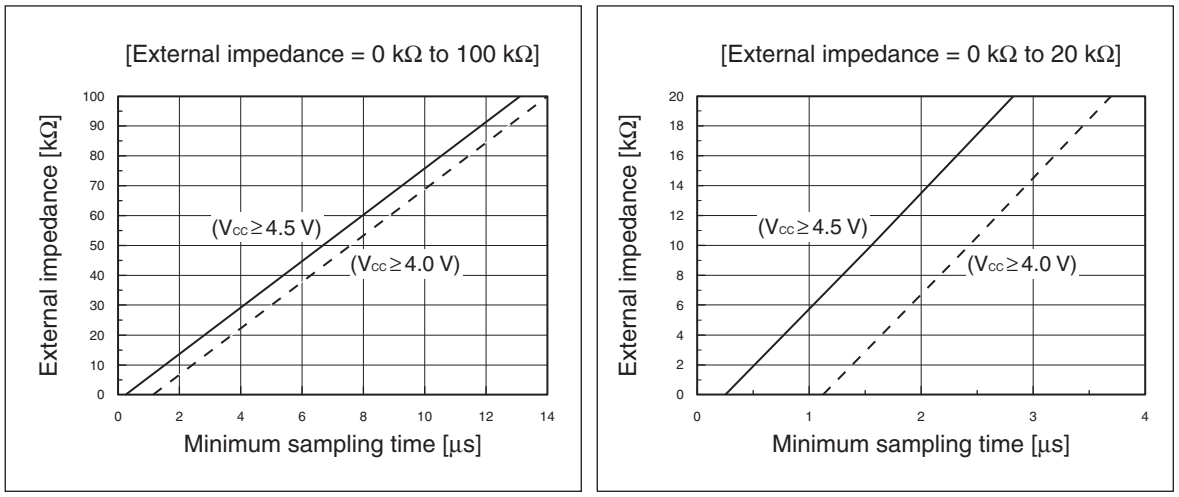
Analog input equivalent circuit



V_{CC}	R	C
4.5 V ≤ V_{CC} ≤ 5.5 V	1.95 kΩ (Max)	17 pF (Max)
4.0 V ≤ V_{CC} < 4.5 V	8.98 kΩ (Max)	17 pF (Max)

Note: The values are reference values.

Relationship between external impedance and minimum sampling time



A/D conversion error

As $|V_{CC}–V_{SS}|$ decreases, the A/D conversion error increases proportionately.

17.6 Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2*1	0.5*2	s	The time of writing 00_H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5*1	7.5*2	s	The time of writing 00_H prior to erasure is excluded.
Byte writing time	—	21	6100*2	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	3.0	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85°C

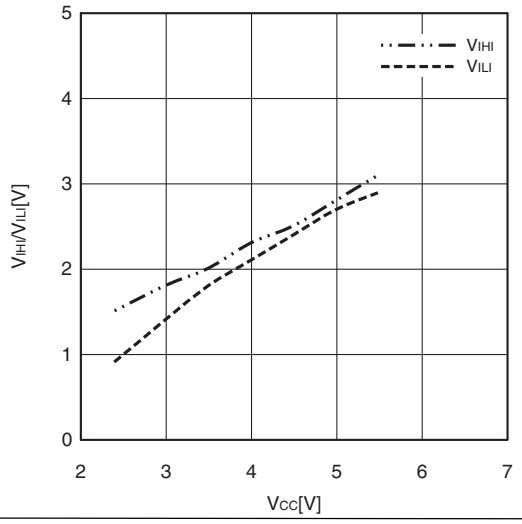
*1: T_A = +25°C, V_{CC} = 5.0 V, 100000 cycles

*2: T_A = +85°C, V_{CC} = 3.0 V, 100000 cycles

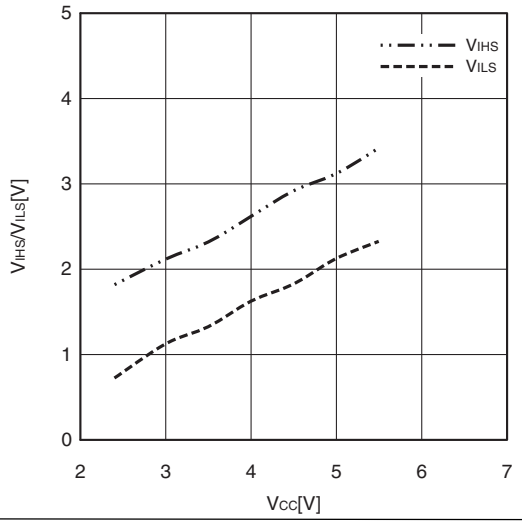
*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C).

Input voltage characteristics

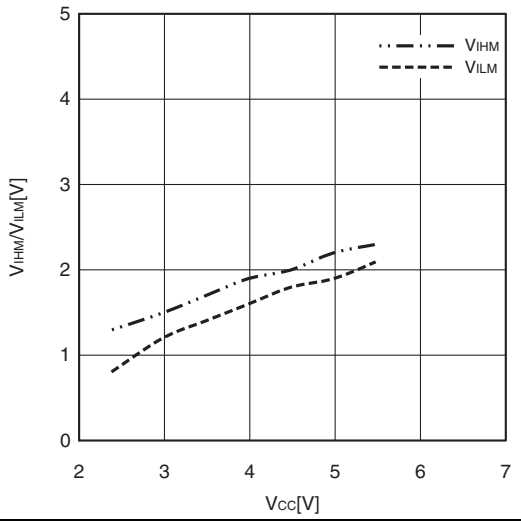
V_{IHI} - V_{CC} and V_{ILI} - V_{CC}
T_A = +25°C

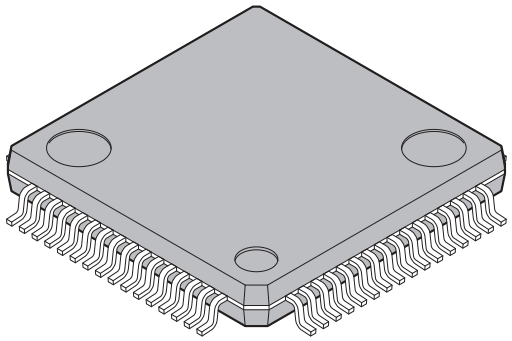


V_{IHS} - V_{CC} and V_{ILS} - V_{CC}
T_A = +25°C



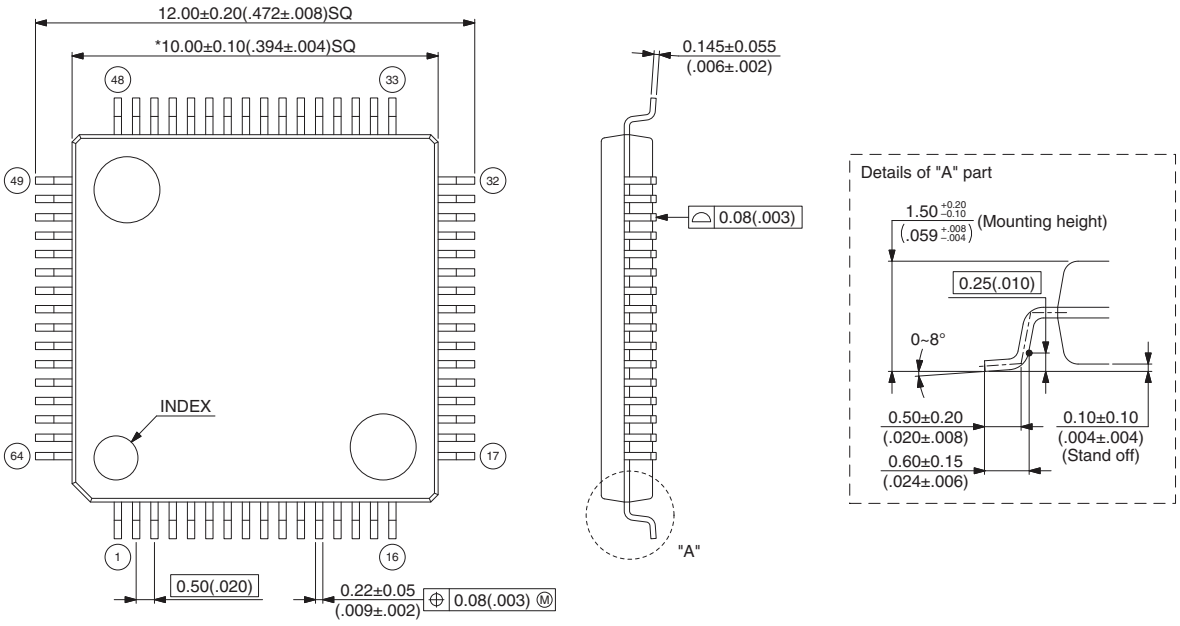
V_{IHM} - V_{CC} and V_{ILM} - V_{CC}
T_A = +25°C



64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.00 mm × 10.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
(FPT-64P-M38)	Weight	0.32 g

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

22. Major Changes

Spansion Publication Number: DS702-00004-1v0-E

Page	Section	Details
1	—	Changed the family name. F^2MC-8FX → New 8FX
49 to 51	Electrical Characteristics 3. DC Characteristics	Changed the values of the following power supply current parameters: I_{CC}, I_{CCS}, I_{CCL}, I_{CCLS}, I_{CCT}, I_{CCMPLL}, I_{CCMCR}, I_{CCSCR}, I_{CCTS}, I_{CCH}, I_A, I_V, I_{LVD}.
52	Electrical Characteristics 4. AC Characteristics (1) Clock Timing	Changed the values of the clock frequency (F_{CRH}).
64	Electrical Characteristics 4. AC Characteristics (8) I^2c Timing	Changed the settings related to the machine clock shown in *2.
71 to 76	Sample Characteristics	Added “Sample Characteristics”.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB95410H/470H Series New 8FX 8-bit Microcontrollers Document Number: 002-07475				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	AKIH	05/17/2011	Migrated to Cypress and assigned document number 002-07475. No change to document contents or format
*A	5198834	AKIH	04/04/2016	Updated to Cypress format.