Infineon Technologies - MB95F478KPMC1-G-SNE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.98K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f478kpmc1-g-sne2

Low-voltage detection reset circuit

Built-in low-voltage detector

Clock supervisor counter

Built-in clock supervisor counter function

Programmable port input voltage level

CMOS input level / hysteresis input level

Dual operation Flash memory

The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

Protects the content of the Flash memory

2. Oscillation Stabilization Wait Time

The main CR clock oscillation stabilization wait time is fixed to the maximum value. Below is the maximum value.

Oscillation stabilization wait time	Remarks
$(2^{10} - 2) / F_{CRH}$	Approx. 128 µs (when the main CR clock is 8 MHz)

The main PLL clock oscillation stabilization wait time is fixed to the maximum value. Below is the maximum value.

Oscillation stabilization wait time	Remarks
$(2^{14} - 2) / F_{CH}$	Approx. 14.1 ms (when the main PLL clock is 4 MHz)

3. Packages And Corresponding Products

Part number / Package	MB95F414H	MB95F416H	MB95F418H	MB95F414K	MB95F416K	MB95F418K
FPT-80P-M37	O					

Part number / Package	MB95F474H	MB95F476H	MB95F478H	MB95F474K	MB95F476K	MB95F478K
FPT-64P-M38	O					
FPT-64P-M39	O					

O: Available

4. Differences among Products and Notes on Product Selection

Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see “17. Electrical Characteristics”.

Package

For details of information on each package, see “3. Packages And Corresponding Products” and “21. Package Dimension”.

Operating voltage

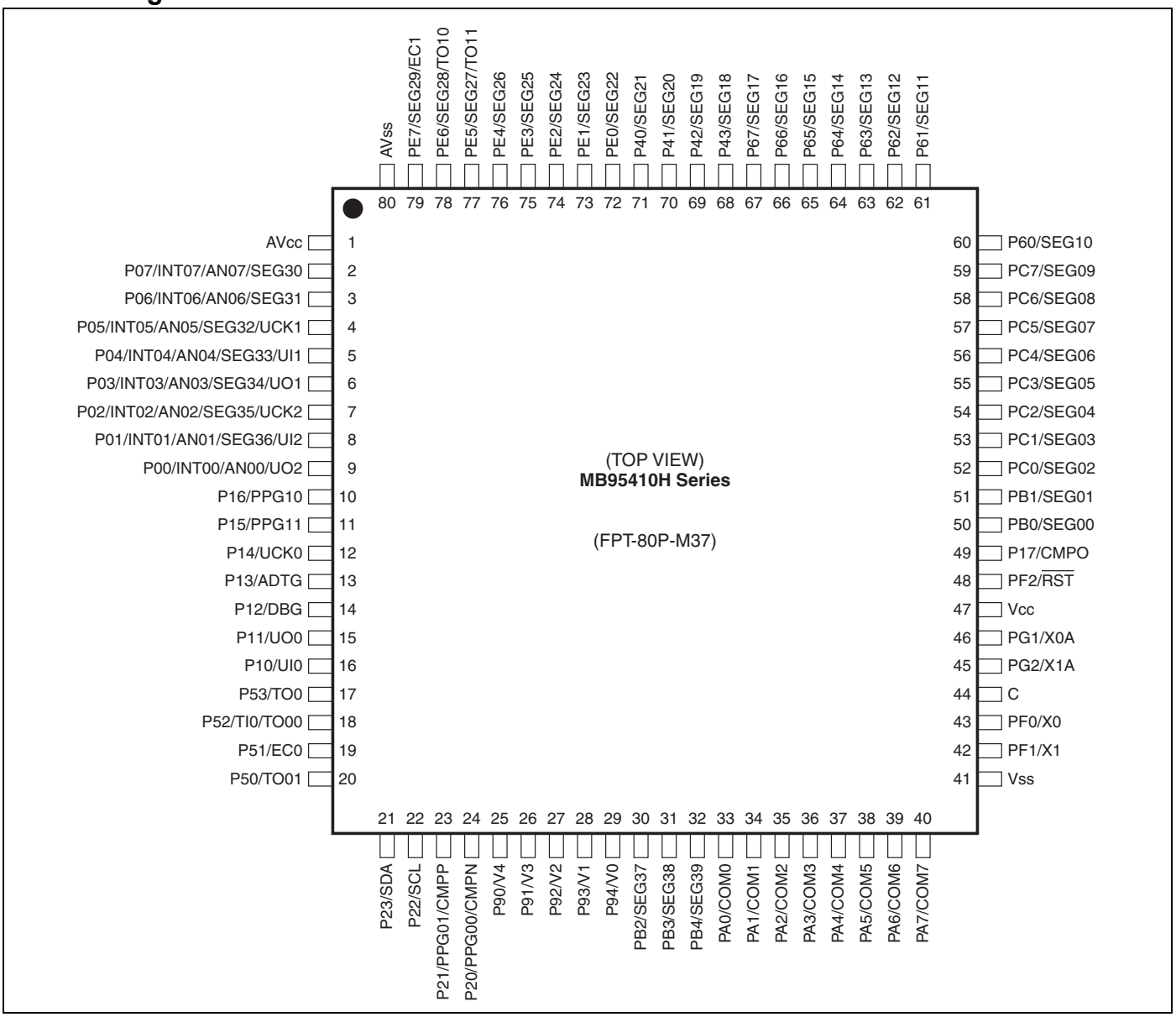
The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see “17. Electrical Characteristics”.

On-chip debug function

The on-chip debug function requires that V_{CC}, V_{SS} and 1 serial-wire be connected to an evaluation tool. For details of the connection method, refer to “Chapter 31 Example Of Serial Programming Connection” in the hardware manual of the MB95410H/470H Series.

5. Pin Assignment



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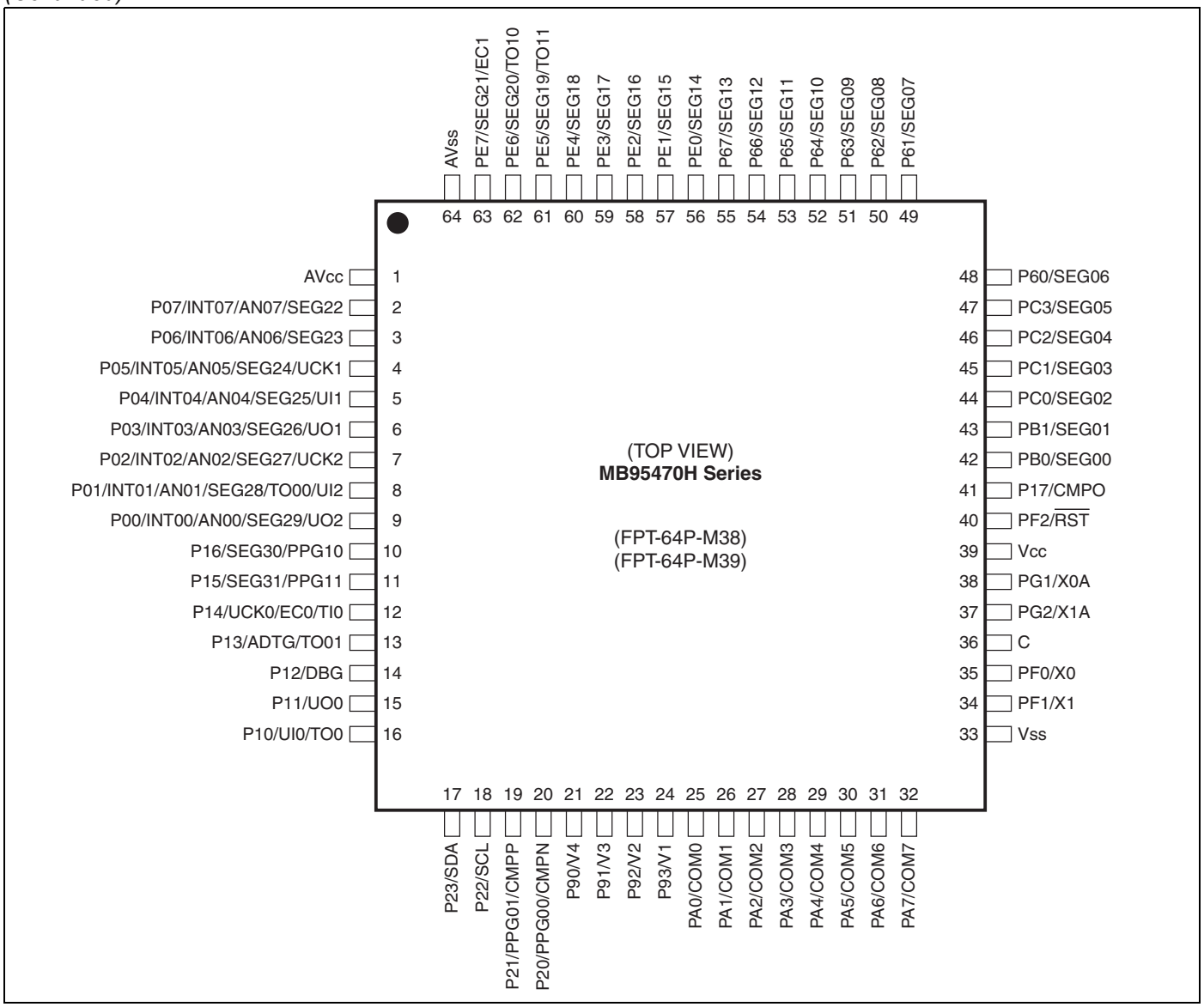
AVss
PE7/SEG21/EC1
PE6/SEG20/TO10
PE5/SEG19/TO11
PE4/SEG18
PE3/SEG17
PE2/SEG16
PE1/SEG15
PE0/SEG14
P67/SEG13
P66/SEG12
P65/SEG11
P64/SEG10
P63/SEG09
P62/SEG08
P61/SEG07
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
AVcc 1
P07/INT07/AN07/SEG22 2
P06/INT06/AN06/SEG23 3
P05/INT05/AN05/SEG24/UCK1 4
P04/INT04/AN04/SEG25/UI1 5
P03/INT03/AN03/SEG26/UO1 6
P02/INT02/AN02/SEG27/UCK2 7
P01/INT01/AN01/SEG28/TO00/UI2 8
P00/INT00/AN00/SEG29/UO2 9
P16/SEG30/PPG10 10
P15/SEG31/PPG11 11
P14/UCK0/EC0/TI0 12
P13/ADTG/TO01 13
P12/DBG 14
P11/UO0 15
P10/UI0/TO0 16
(TOP VIEW)
MB95470H Series
(FPT-64P-M38)
(FPT-64P-M39)
48 P60/SEG06
47 PC3/SEG05
46 PC2/SEG04
45 PC1/SEG03
44 PC0/SEG02
43 PB1/SEG01
42 PB0/SEG00
41 P17/CMPO
40 PF2/RST
39 Vcc
38 PG1/X0A
37 PG2/X1A
36 C
35 PF0/X0
34 PF1/X1
33 Vss
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
P23/SDA
P22/SCL
P21/PPG01/CMPP
P20/PPG00/CMPN
P90/V4
P91/V3
P92/V2
P93/V1
PA0/COM0
PA1/COM1
PA2/COM2
PA3/COM3
PA4/COM4
PA5/COM5
PA6/COM6
PA7/COM7

Pin no.	Pin name	I/O circuit type*	Function
9	P00	W	General-purpose I/O port
	INT00		External interrupt input pin
	AN00		A/D analog input pin
	UO2		UART/SIO ch. 2 data output pin
10	P16	Y	General-purpose I/O port
	PPG10		8/16-bit PPG ch. 1 output pin
11	P15	Y	General-purpose I/O port
	PPG11		8/16-bit PPG ch. 1 output pin
12	P14	H	General-purpose I/O port
	UCK0		UART/SIO ch. 0 clock I/O pin
13	P13	H	General-purpose I/O port
	ADTG		A/D trigger input (ADTG) pin
14	P12	D	General-purpose I/O port
	DBG		DBG input pin
15	P11	H	General-purpose I/O port
	UO0		UART/SIO ch. 0 data output pin
16	P10	G	General-purpose I/O port
	UI0		UART/SIO ch. 0 data input pin
17	P53	H	General-purpose I/O port
	TO0		16-bit reload timer output pin
18	P52	H	General-purpose I/O port
	TI0		16-bit reload timer input pin
	TO00		8/16-bit composite timer ch. 0 output pin
19	P51	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
20	P50	H	General-purpose I/O port
	TO01		8/16-bit composite timer ch. 0 output pin
21	P23	I	General-purpose I/O port
	SDA		I^2C data I/O pin
22	P22	I	General-purpose I/O port
	SCL		I^2C clock I/O pin
23	P21	T	General-purpose I/O port
	PPG01		8/16-bit PPG ch. 0 output pin
	CMPP		Voltage comparator input pin
24	P20	T	General-purpose I/O port
	PPG00		8/16-bit PPG ch. 0 output pin
	CMPN		Voltage comparator input pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
25	P90	R	General-purpose I/O port
	V4		LCDC drive power supply pin
26	P91	R	General-purpose I/O port
	V3		LCDC drive power supply pin
27	P92	R	General-purpose I/O port
	V2		LCDC drive power supply pin
28	P93	R	General-purpose I/O port
	V1		LCDC drive power supply pin
29	P94	R	General-purpose I/O port
	V0		LCDC drive power supply pin
30	PB2	M	General-purpose I/O port
	SEG37		LCDC SEG output pin
31	PB3	M	General-purpose I/O port
	SEG38		LCDC SEG output pin
32	PB4	M	General-purpose I/O port
	SEG39		LCDC SEG output pin
33	PA0	M	General-purpose I/O port
	COM0		LCDC COM output pin
34	PA1	M	General-purpose I/O port
	COM1		LCDC COM output pin
35	PA2	M	General-purpose I/O port
	COM2		LCDC COM output pin
36	PA3	M	General-purpose I/O port
	COM3		LCDC COM output pin
37	PA4	M	General-purpose I/O port
	COM4		LCDC COM output pin
38	PA5	M	General-purpose I/O port
	COM5		LCDC COM output pin
39	PA6	M	General-purpose I/O port
	COM6		LCDC COM output pin
40	PA7	M	General-purpose I/O port
	COM7		LCDC COM output pin
41	V_{SS}	—	Power supply pin (GND)
42	PF1	B	General-purpose I/O port
	X1		Main clock oscillation pin
43	PF0	B	General-purpose I/O port
	X0		Main clock oscillation pin

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Pin no.	Pin name	I/O circuit type*	Function
79	PE7	M	General-purpose I/O port
	SEG29		LCDC SEG output pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
80	AV_{SS}	—	A/D converter power supply pin (GND)

*: For the I/O circuit types, see “8. I/O Circuit Type”.

7. Pin Description (MB95470H Series)

Pin no.	Pin name	I/O circuit type*	Function
1	AV_{CC}	—	A/D converter power supply pin
2	P07	S	General-purpose I/O port
	INT07		External interrupt input pin
	AN07		A/D analog input pin
	SEG22		LCDC SEG output pin
3	P06	S	General-purpose I/O port
	INT06		External interrupt input pin
	AN06		A/D analog input pin
	SEG23		LCDC SEG output pin
4	P05	S	General-purpose I/O port
	INT05		External interrupt input pin
	AN05		A/D analog input pin
	SEG24		LCDC SEG output pin
	UCK1		UART/SIO ch. 1 clock I/O pin
5	P04	V	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D analog input pin
	SEG25		LCDC SEG output pin
	UI1		UART/SIO ch. 1 data input pin
6	P03	S	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D analog input pin
	SEG26		LCDC SEG output pin
	UO1		UART/SIO ch. 1 data output pin
7	P02	S	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D analog input pin
	SEG27		LCDC SEG output pin
	UCK2		UART/SIO ch. 2 clock I/O pin
8	P01	V	General-purpose I/O port
	INT01		External interrupt input pin
	AN01		A/D analog input pin
	SEG28		LCDC SEG output pin
	TO00		8/16-bit composite timer ch. 0 output pin
	UI2		UART/SIO ch. 2 data input pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
21	P90	R	General-purpose I/O port
	V4		LCDC drive power supply pin
22	P91	R	General-purpose I/O port
	V3		LCDC drive power supply pin
23	P92	R	General-purpose I/O port
	V2		LCDC drive power supply pin
24	P93	R	General-purpose I/O port
	V1		LCDC drive power supply pin
25	PA0	M	General-purpose I/O port
	COM0		LCDC COM output pin
26	PA1	M	General-purpose I/O port
	COM1		LCDC COM output pin
27	PA2	M	General-purpose I/O port
	COM2		LCDC COM output pin
28	PA3	M	General-purpose I/O port
	COM3		LCDC COM output pin
29	PA4	M	General-purpose I/O port
	COM4		LCDC COM output pin
30	PA5	M	General-purpose I/O port
	COM5		LCDC COM output pin
31	PA6	M	General-purpose I/O port
	COM6		LCDC COM output pin
32	PA7	M	General-purpose I/O port
	COM7		LCDC COM output pin
33	V_{SS}	—	Power supply pin (GND)
34	PF1	B	General-purpose I/O port
	X1		Main clock oscillation pin
35	PF0	B	General-purpose I/O port
	X0		Main clock oscillation pin
36	C	—	Capacitor connection pin
37	PG2	C	General-purpose I/O port
	X1A		Subclock oscillation pin (32 kHz)
38	PG1	C	General-purpose I/O port
	X0A		Subclock oscillation pin (32 kHz)
39	V_{CC}	—	Power supply pin
40	PF2	A	General-purpose I/O port
	RST		Reset pin Dedicated reset pin for MB95F474H/F476H/F478H

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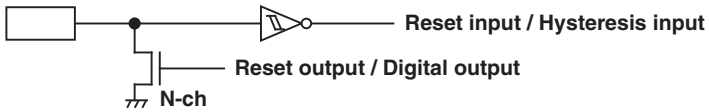
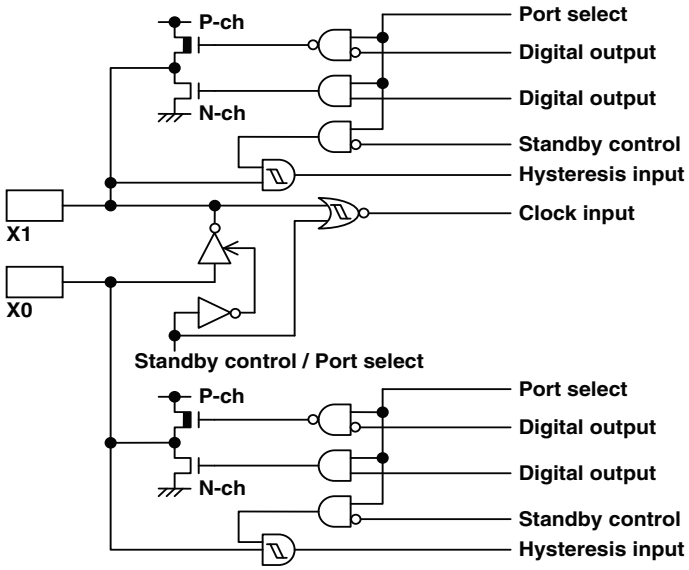
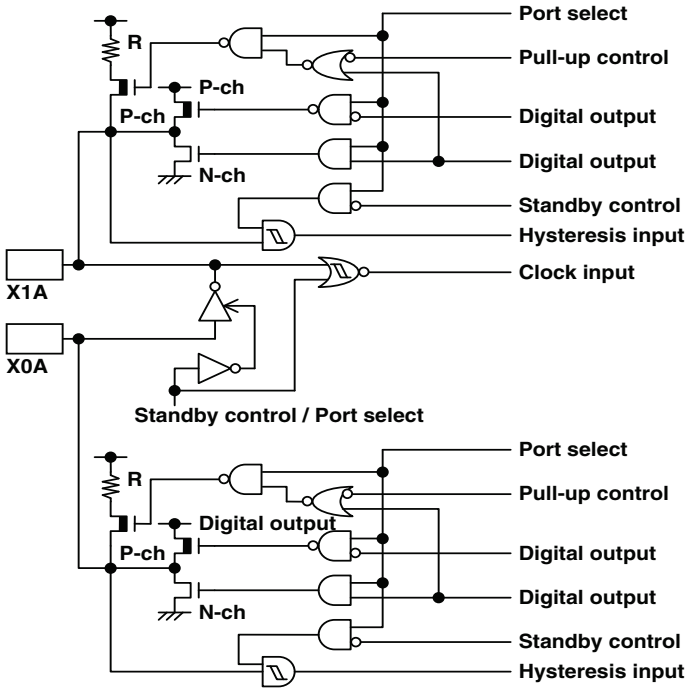
8. I/O Circuit Type

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 10 MΩ • CMOS output • Hysteresis input • Pull-up control available

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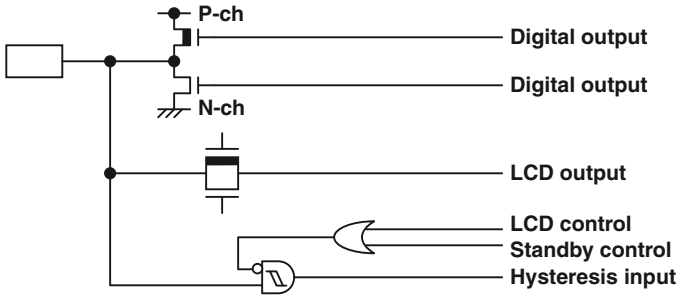
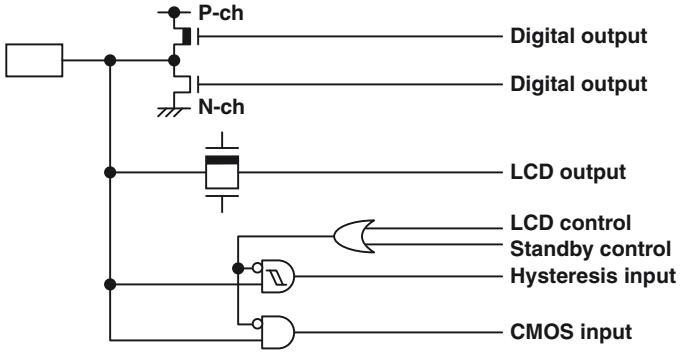
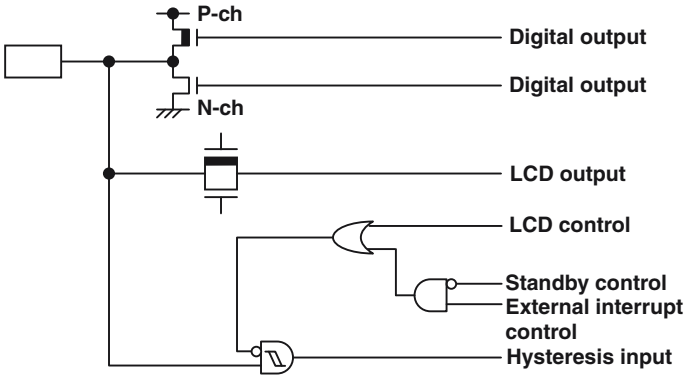
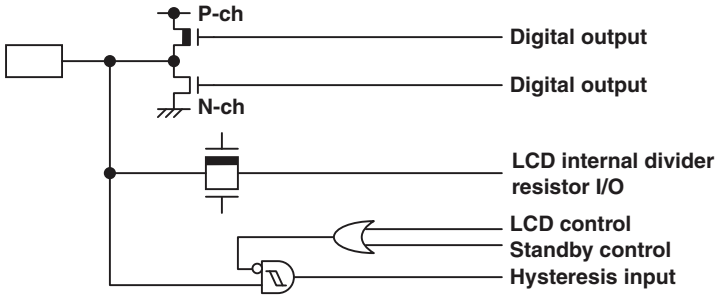
Type	Circuit	Remarks
M		• CMOS output • LCD output • Hysteresis input
N		• CMOS output • LCD output • Hysteresis input • CMOS input
Q		• CMOS output • LCD output • Hysteresis input
R		• CMOS output • LCD power supply • Hysteresis input

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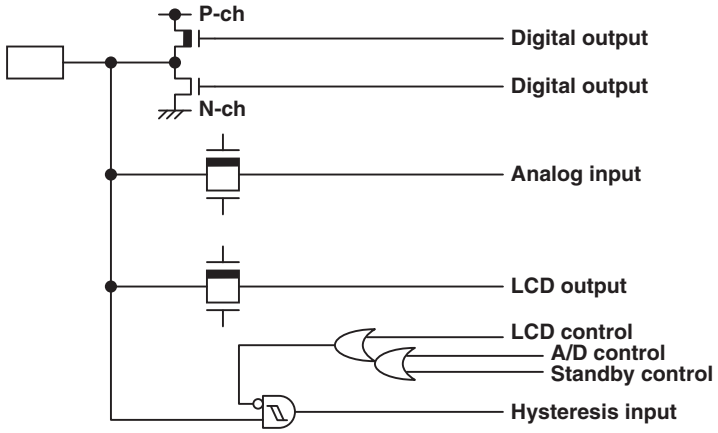
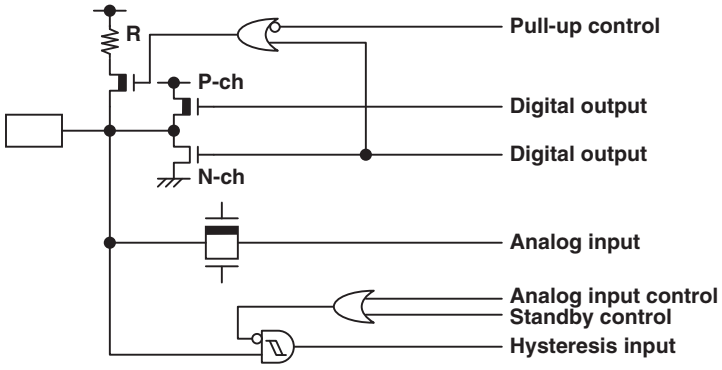
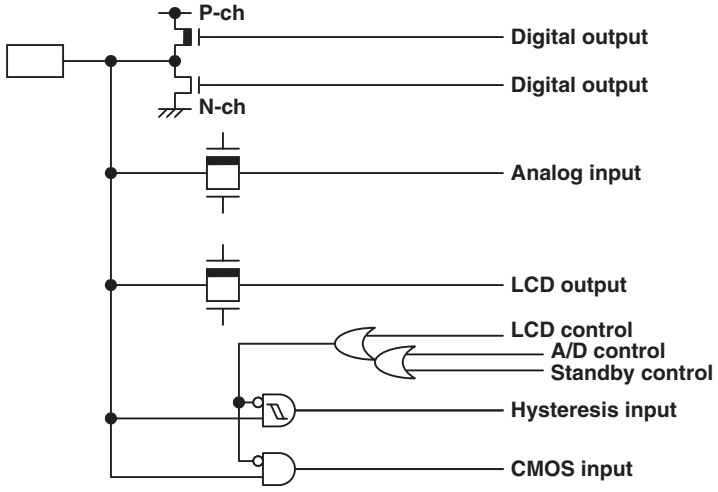
Type	Circuit	Remarks
S		• CMOS output • LCD output • Hysteresis input • Analog input
T		• CMOS output • Hysteresis input • Analog input • Pull-up control available
V		• CMOS output • LCD output • Hysteresis input • Analog input • CMOS input

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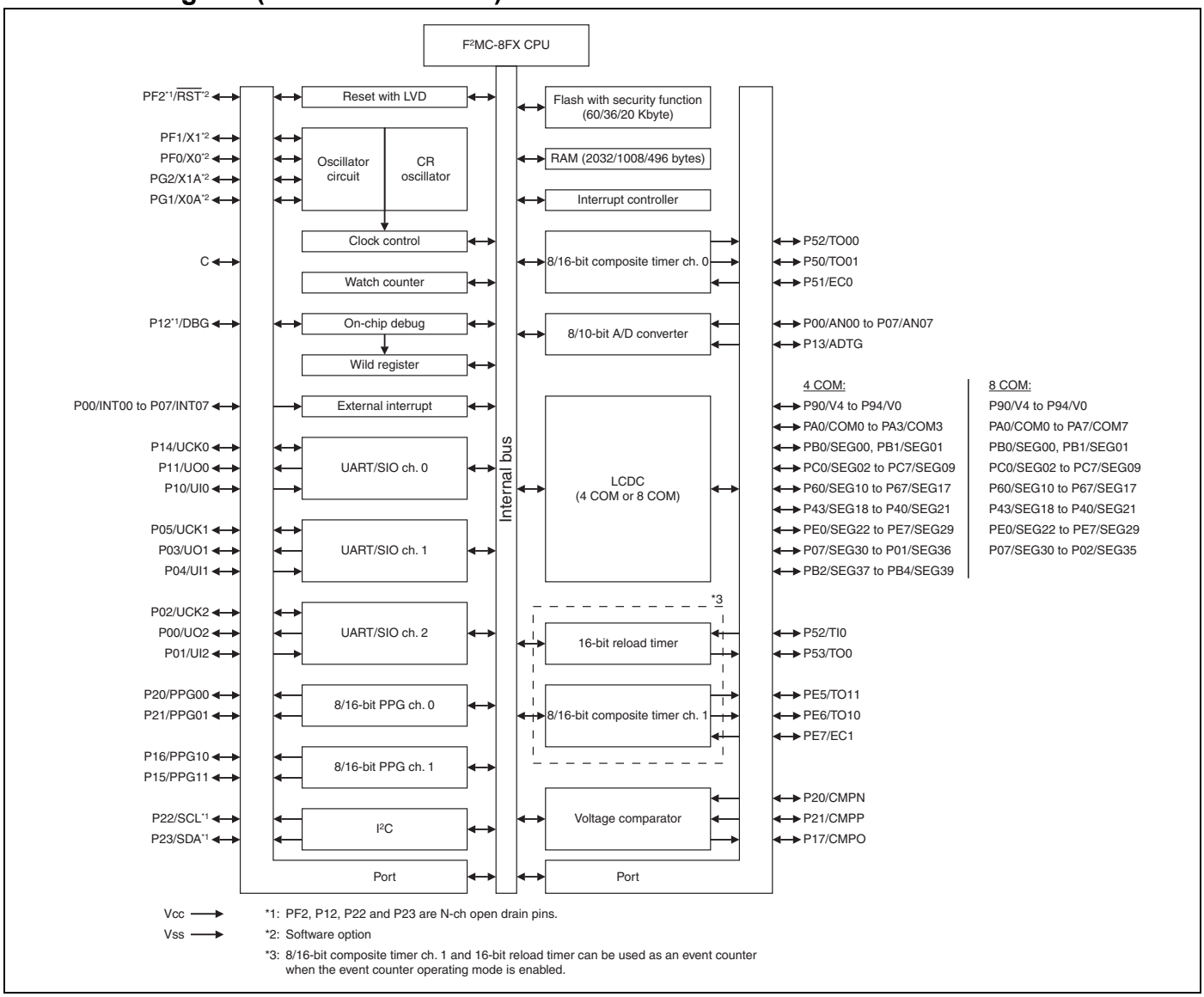
11. Block Diagram (MB95410H Series)



Address	Register abbreviation	Register name	R/W	Initial value
$002D_H$	PUL1	Port 1 pull-up register	R/W	00000000_B
$002E_H$	PUL2	Port 2 pull-up register	R/W	00000000_B
$002F_H$ to 0034_H	—	(Disabled)	—	—
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000_B
0038_H	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	00000000_B
0039_H	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	00000000_B
$003A_H$	PC01	8/16-bit PPG01 control register	R/W	00000000_B
$003B_H$	PC00	8/16-bit PPG00 control register	R/W	00000000_B
$003C_H$	PC11	8/16-bit PPG11 control register	R/W	00000000_B
$003D_H$	PC10	8/16-bit PPG10 control register	R/W	00000000_B
$003E_H$	TMCSRH0	16-bit reload timer control status register upper	R/W	00000000_B
$003F_H$	TMCSRL0	16-bit reload timer control status register lower	R/W	00000000_B
0040_H to 0047_H	—	(Disabled)	—	—
0048_H	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000_B
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$ to $004E_H$	—	(Disabled)	—	—
$004F_H$	LCDCC2	LCDC control register 2	R/W	00010100_B
0050_H	CMR0	Voltage comparator control register	R/W	$000X0001_B$
0051_H to 0055_H	—	(Disabled)	—	—
0056_H	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	00000000_B
0057_H	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	00100000_B
0058_H	SSR0	UART/SIO serial status register ch. 0	R/W	00000001_B
0059_H	TDR0	UART/SIO serial output data register ch. 0	R/W	00000000_B
$005A_H$	RDR0	UART/SIO serial input data register ch. 0	R	00000000_B
$005B_H$	SMC11	UART/SIO serial mode control register 1 ch. 1	R/W	00000000_B
$005C_H$	SMC21	UART/SIO serial mode control register 2 ch. 1	R/W	00100000_B
$005D_H$	SSR1	UART/SIO serial status register ch. 1	R/W	00000001_B
$005E_H$	TDR1	UART/SIO serial output data register ch. 1	R/W	00000000_B

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17. Electrical Characteristics

17.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	−2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{CL}	—	15	mA	
“L” level average current	I_{CLAV}	—	4	mA	Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{CH}	—	−15	mA	
“H” level average current	I_{CHAV}	—	−4	mA	Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	−100	mA	
“H” level total average output current	ΣI_{OHAV}	—	−50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	T_{stg}	−55	+150	°C	

*1: These parameters are based on the condition that V_{SS} = 0.0 V.

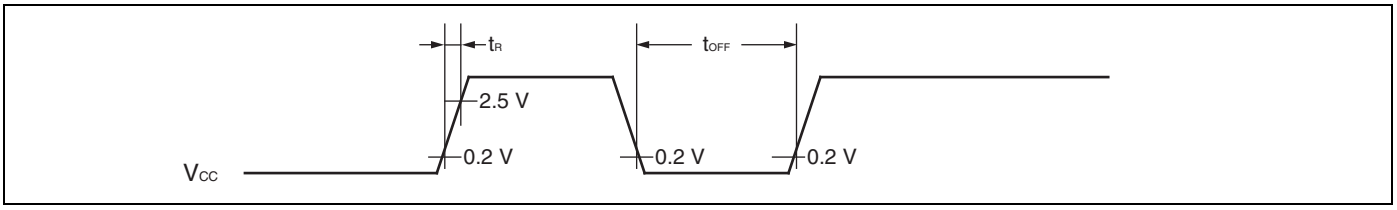
*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

(Continued)

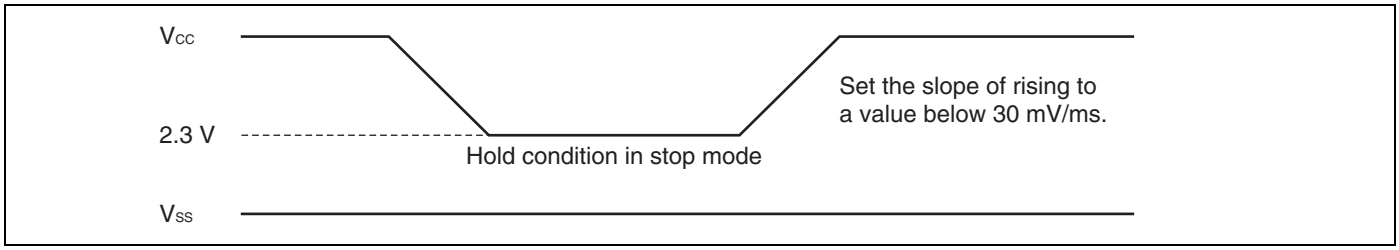
17.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

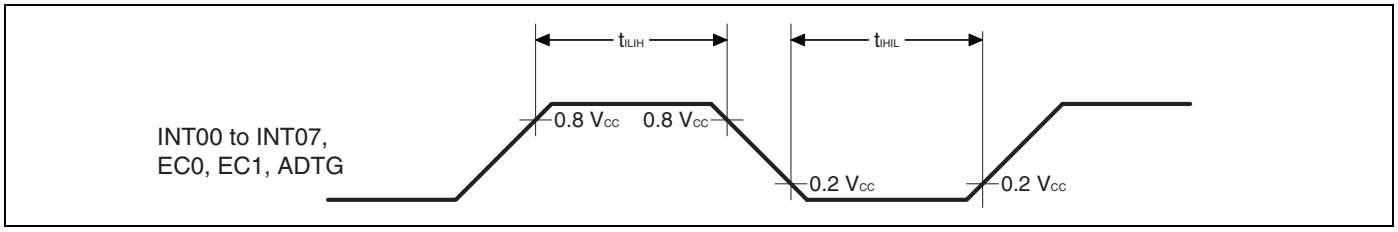


17.4.5 Peripheral Input Timing

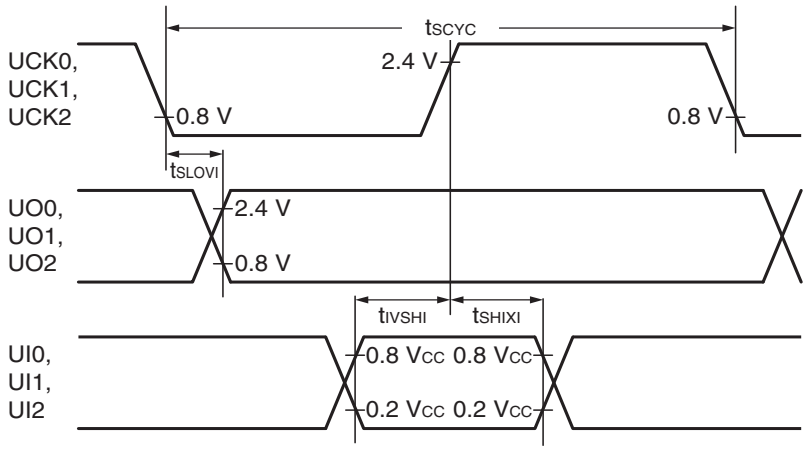
(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, ADTG	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

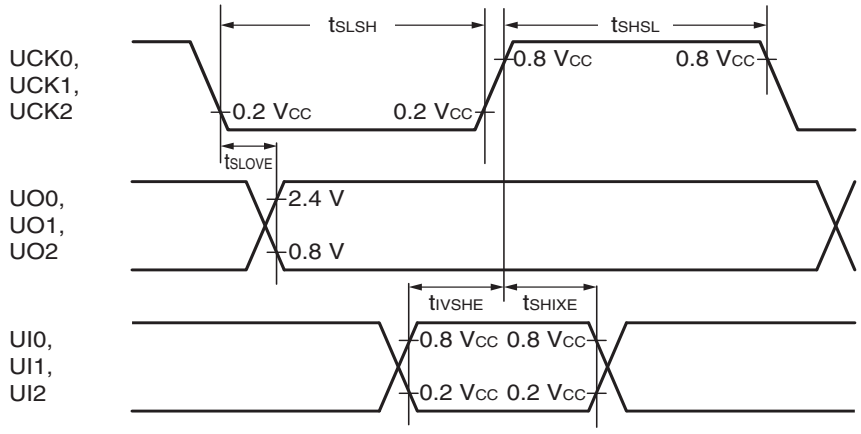
*: See “17.4.2. Source Clock/Machine Clock” for t_{MCLK}.



Internal shift clock mode



External shift clock mode



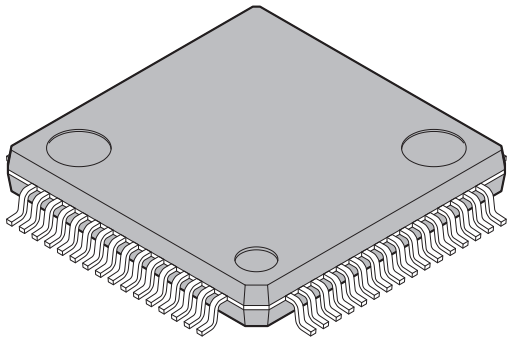
(Continued)

(V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
Start condition detection	$t_{HD;STA}$	SCL, SDA	R = 1.7 kΩ, C = 50 pF*1	2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Stop condition detection	$t_{SU;STO}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Restart condition detection condition	$t_{SU;STA}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL, SDA		2 t_{MCLK} − 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{LOW} − 3 t_{MCLK} − 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL, SDA		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{MCLK} − 20	—	ns	At reception
SDA↓→SCL↑ (at wakeup function)	t_{WAKEUP}	SCL, SDA		Oscillation stabilization wait time + 2 t_{MCLK} − 20	—	ns	

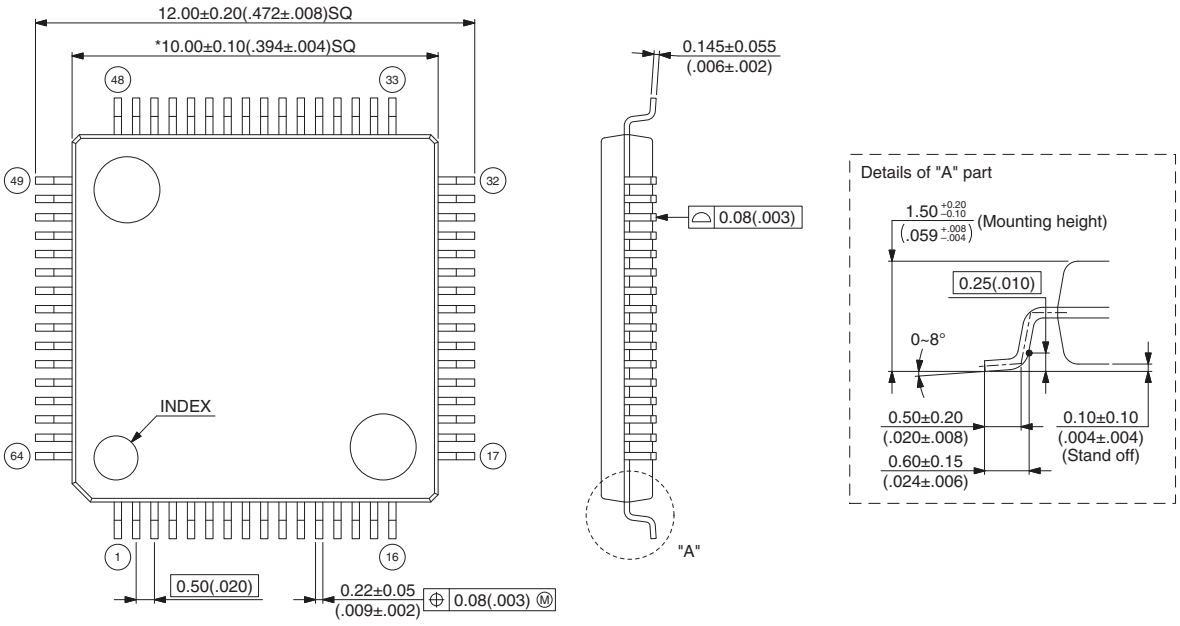
*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2:
- See “17.4.2. Source Clock/Machine Clock” for t_{MCLK}.
- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I^2C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I^2C clock control register (ICCR0).
- The actual timing of I^2C is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS4 to CS0 bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98), (5, 22), (6, 22), (7, 22) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (8, 22) : 0.9 MHz < t_{MCLK} ≤ 16.25 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (1, 38), (6, 4), (7, 4), (8, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (5, 8) : 3.3 MHz < t_{MCLK} ≤ 16.25 MHz

64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.00 mm × 10.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
(FPT-64P-M38)	Weight	0.32 g

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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