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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	·
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21345-12pvxe

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



CY8C21345/CY8C21645 CY8C22345/CY8C22345H/CY8C22645

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Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful for complete systems. Additional resources include a MAC, low voltage detection, and power on reset. The merits of each system resource are:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Additional digital resources and clocks dedicated to and optimized for CapSense.

- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The I²C module provides 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power on reset (POR) circuit eliminates the need for a system supervisor.
- An internal voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

RTC hardware block.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have varying numbers of digital and analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC families covered by this datasheet are highlighted in the table.

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66 ^[2]	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4 ^[3]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94 ^[2]	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A ^[2]	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45 ^[2]	up to 38	2	8	up to 38	0	4	6 ^[3]	1 K	16 K
CY8C21x45 ^[2]	up to 24	1	4	up to 24	0	4	6 ^[3]	512	8 K
CY8C21x34 ^[2]	up to 28	1	4	up to 28	0	2	4 [3]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4 [3]	256	4 K
CY8C20x34 ^[2]	up to 28	0	0	up to 28	0	0	3 ^[3, 4]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3 ^[3, 4]	up to 2 K	up to 32 K

Table 1. PSoC Device Characteristics

Notes

2. Automotive qualified devices available in this group.

3. Limited analog functionality.

4. Two analog blocks and one $\mathsf{CapSense}^{\texttt{®}}$ block.



Getting Started

For in depth information, along with detailed programming details, see the *PSoC[®]* Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer[™] is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - □ Hardware and software I²C slaves and masters
 - □ Full-speed USB 2.0
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.



C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC[®] device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

- 1. Select User Modules.
- 2. Configure user modules.
- 3. Organize and connect.
- 4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.



Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	00	RW		40			80			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PR13IC0	0E	RW		4E			8E			CE	
PRI3IC1	UF	RW	0100004	4F	DIA/		8F			CF	DIA
PR14DM0	10	RW	CMPOCR1	50	RW		90		GDI_U_IN	D0	RW
PR14DM1	11	RW	CMPUCR2	51	RW		91		GDI_E_IN	D1	RW
PR14IC0	12	RW		52	DW/		92			D2	RW
11(14)(1	13	L A A A	CMP1CR1	53	RW		93		001_L_00	D3	r.vv
	14		CMP1CR2	55	RW		94			D4 D5	
	15		GIVIF TORZ	56	11.00		95			DG	
	10		VDAC51CR0	57	RW		97			D7	
	18		CSCMPCR0	58	#		98		MUX CR0	D8	RW
	19		CSCMPGOEN	59	 RW		99		MUX_CR1	D9	RW
	1A		CSLUTCR0	5A	RW		9A		MUX CR2	DA	RW
	1B		CMPCOLMUX	5B	RW		9B		MUX CR3	DB	RW
	1C		CMPPWMCR	5C	RW		9C		DAC_CR1#	DC	RW
	1D		CMPFLTCR	5D	RW		9D		OSC_GO_EN	DD	RW
	1E		CMPCLK1	5E	RW		9E		OSC_CR4	DE	RW
	1F		CMPCLK0	5F	RW		9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	R
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	V2BG_TR	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	W
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	W
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DBC02CR1	2B	RW	CLK_CR3	6B	RW	SADC_CR3TRIM	AB	RW	ECO_IR	EB	W
	20	RW		6C	RVV	SADU_CR4	AC	RW	WUX_CR4	EC	RW
DCC03IN	2D	KW	TMP_DR1	6D	KW DM	1200_AD	AD	KW		ED	
DEC03CD1	2E 2E	RW DW/	TMP_DR2	0E 6E	RVV DW/		AE				
DBCUSCKI	20	RW DW/	INF_UK3	70	RVV	PDIOPI	AF PO	D\4/		EF	
DBC10FN	30	RW/		70		RDIOSYN	BU B1	RW/		FU F1	
DBC100U	31	RW/	ACE00CR1	72	R\//	RDIOIS	B2	RW/		F2	
DBC10CR1	32	RW/	ACE00CR2	72	RW	RDIOI TO	B3	RW		F3	
DBC10CIX1	3/	RW/	ACLOUCINZ	73	11.00	RDIOLT1	B/	RW		F/	
DBC11IN	35	RW/		75		RDIOROO	B5	RW/		F5	
DBC110U	36	RW	ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE01CR2	77	RW	RDIODSM	B7	RW	CPU F	F7	RI
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A	-	RDI1IS	BA	RW	FLS PR1	FA	RW
DBC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		- 7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW	DAC_CR0#	FD	RW
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DBC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#
Blank fields are Res	arved and mu	et not ho	accossod			# Accoss is hit spor	fic				



DC Operational Amplifier Specifications

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25°C, unless specified otherwise, and are for design guidance only.

Table 11. DC Operational Amplifier Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{OSOA}	Input offset voltage (absolute value)	_	2.5	15	mV	
I _{SOA}	Supply current (absolute value) A-grade devices E-grade devices	-		30 35	μA μA	
TCV _{OSOA}	Average input offset voltage drift	_	10	-	μV/°C	
I _{EBOA} ^[7]	Input leakage current (Port 0 analog pins)	_	200	-	pА	Gross tested to 1 µA
C _{INOA}	Input capacitance (Port 0 analog pins)	_	4.5	9.5	pF	Package and pin dependent. T _A = 25 °C
V _{CMOA}	Common mode voltage range	0.5	_	V _{DD} – 1	V	

DC IDAC Specifications

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 12. DC IDAC Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
IDAC _{GAIN}	IDAC gain	-	75.4	218	nA/bit	IDAC gain at 1x current gain
		-	335	693	nA/bit	IDAC gain at 4x current gain
		-	1160	2410	nA/bit	IDAC gain at 16x current gain
		-	2340	5700	nA/bit	IDAC gain at 32x current gain
	Monotonicity	No	-	-	-	IDAC gain is non-monotonous at step intervals of (0x10)
IDAC _{GAIN_VAR}	IDAC gain variation over temperature –40 °C to 85 °C	-	3.22	-	nA	at 1x current gain
		-	18.1	-	nA	at 4x current gain
		-	59.9	-	nA	at 16x current gain
		-	120	-	nA	at 32x current gain
I _{IDAC}	IDAC current at maximum code	-	19.2	-	μA	at 1x current gain
	(0xFF)	-	85.4	-	μA	at 4x current gain
		-	295	-	μA	at 16x current gain
		_	596	_	μA	at 32x current gain

Note

7. Atypical behavior: IEBOA of Port 0 Pin 0 is below 1 nA at 25 °C; 50 nA over temperature. Use Port 0 Pins 1 – 7 for the lowest leakage of 200 nA.



DC POR and LVD Specifications

Table 15 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 15. DC POR and LVD Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{PPOR1} V _{PPOR2}	V _{DD} value for PPOR trip PORLEV[1:0] = 01b PORLEV[1:0] = 10b		2.82 4.55	2.95 4.73	V V	V_{DD} must be greater than or equal to 3.0 V during startup, reset from the XRES pin, or reset from Watchdog.
$\begin{array}{c} V_{LVD2} \\ V_{LVD3} \\ V_{LVD4} \\ V_{LVD5} \\ V_{LVD6} \\ V_{LVD7} \end{array}$	V _{DD} value for LVD trip VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.95 3.06 4.37 4.50 4.62 4.71	3.02 3.13 4.48 4.64 4.73 4.81	3.09 3.20 4.55 4.75 4.83 4.95	V V V V V V	



DC Programming Specifications

Table 16 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 16. DC Programming Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{DDP}	V _{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V _{DDLV}	Low V _{DD} for verify A-grade devices E-grade devices	3.0 4.7	3.1 4.8	3.2 4.9	V V	This specification applies to the functional requirements of external programmer tools
V _{DDHV}	High V _{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
V _{DDIWRITE}	Supply voltage for flash write operation A-grade devices E-grade devices	3.0 4.75		5.25 5.25	V V	This specification applies to this device when it is executing internal flash writes
I _{DDP}	Supply current during programming or verify	-	5	25	mA	
V _{ILP}	Input low voltage during programming or verify	-	-	0.8	V	
V _{IHP}	Input high voltage during programming or verify	2.2	-	-	V	
I _{ILP}	Input current when applying V _{ILP} to P1[0] or P1[1] during programming or verify	Ι	-	0.2	mA	Driving internal pull-down resistor
I _{IHP}	Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify	_	_	1.5	mA	Driving internal pull-down resistor
V _{OLV}	Output low voltage during programming or verify	-	-	0.75	V	
V _{OHV}	Output high voltage during programming or verify	V _{DD} – 1.0	-	V _{DD}	V	
Flash _{ENPB}	Flash endurance (per block) ^[8, 9] A-grade devices E-grade devices	1,000 100			-	Erase/write cycles per block
Flash _{ENT}	Flash endurance (total) ^[9, 10] CY8C21x45 A-grade devices CY8C22x45 A-grade devices CY8C21x45 E-grade devices CY8C22x45 E-grade devices	128,000 256,000 12,800 25,600		- - - -	_ _ _	Erase/write cycles
Flash _{DR}	Flash data retention ^[9] A-grade devices E-grade devices	10 10			Years Years	

Notes

The erase/write cycle limit per block (Flash_{ENPB}) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.

9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.

10. The maximum total number of allowed erase/write cycles is the minimum Flash ENPB value multiplied by the number of flash blocks in the device.



AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Function	Description	Min	Тур	Max	Units	Notes
All functions	Block Input Clock Frequency					
	$V_{DD} \ge 4.75 \text{ V}$	-	-	50.4 ^[15]	MHz	
	V _{DD} < 4.75 V	-	-	25.2 ^[15]	MHz	
Timer	Input Clock Frequency					
	No Capture, $V_{DD} \ge 4.75 \text{ V}$	-	-	50.4 ^[15]	MHz	
	No Capture, V _{DD} < 4.75 V	-	-	25.2 ^[15]	MHz	
	With Capture	-	-	25.2 ^[15]	MHz	
	Capture Pulse Width	50 ^[14]	-	-	ns	
Counter	Input Clock Frequency					
	No Enable Input, $V_{DD} \ge 4.75 \text{ V}$	-	-	50.4 ^[15]	MHz	
	No Enable Input, V_{DD} < 4.75 V	-	-	25.2 ^[15]	MHz	
	With Enable Input	-	-	25.2 ^[15]	MHz	
	Enable Input Pulse Width	50 ^[14]	-	-	ns	
Dead Band	Kill Pulse Width					
	Asynchronous Restart Mode	20	-	-	ns	
	Synchronous Restart Mode	50 ^[14]	-	-	ns	
	Disable Mode	50 ^[14]	-	-	ns	
	Input Clock Frequency			-	1	
	$V_{DD} \ge 4.75 \text{ V}$	-	-	50.4 ^[15]	MHz	
	V _{DD} < 4.75 V	-	-	25.2 ^[15]	MHz	
CRCPRS	Input Clock Frequency			-	1	
(PRS Mode)	$V_{DD} \ge 4.75 \text{ V}$	-	-	50.4 ^[15]	MHz	
	V _{DD} < 4.75 V	-	-	25.2 ^[15]	MHz	
CRCPRS (CRC Mode)	Input Clock Frequency	-	-	25.2 ^[15]	MHz	
SPIM	Input Clock Frequency	-	_	8.4 ^[15]	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input Clock (SCLK) Frequency	-	-	4.2 ^[15]	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated Between Transmissions	50 ^[14]	-	-	ns	

Table 20. AC Digital Block Specifications

Note

14.50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).



Table 20. AC Digital Block Specifications (continued)

Function	Description	Min	Тур	Max	Units	Notes		
Transmitter	Input Clock Frequency					The baud rate is equal to the inpu		
	$V_{DD} \ge 4.75 \text{ V}, 2 \text{ Stop Bits}$	-	-	50.4 ^[15]	MHz	clock frequency divided by 8.		
	$V_{DD} \ge 4.75 \text{ V}, 1 \text{ Stop Bit}$	_	_	25.2 ^[15]	MHz			
	V _{DD} < 4.75 V	_	_	25.2 ^[15]	MHz			
Receiver	Input Clock Frequency					The baud rate is equal to the input		
	$V_{DD} \ge 4.75 \text{ V}, 2 \text{ Stop Bits}$	-	-	50.4 ^[15]	MHz	clock frequency divided by 8.		
	$V_{DD} \ge 4.75 \text{ V}, 1 \text{ Stop Bit}$	_	-	25.2 ^[15]	MHz			
	V _{DD} < 4.75 V	-	-	25.2 ^[15]	MHz			

15. Accuracy derived from IMO with appropriate trim for $V_{\mbox{\scriptsize DD}}$ range.



AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 21. AC External Clock Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
FOSCEXT	Frequency	0.093	-	24.6	MHz	
-	High period	20.0	-	5300	ns	
-	Low period	20.0	-	-	ns	
-	Power-up IMO to switch	150	-	-	μs	

AC SAR10 ADC Specifications

Table 22 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 85 °C, or 3.0 V to 3.6 V and -40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and -40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 22. AC SAR10 ADC Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{INADC}	SAR ADC input clock frequency	_	-	2	MHz	The sample rate of the SAR10 ADC is equal to F _{INADC} divided by 13.



Development Tool Selection

This section presents the development tools available for the automotive CY8C21x45 and CY8C22x45 families.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the contents of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- ICE-Cube unit
- 28-pin PDIP emulation pod for CY8C29466-24PXI
- 28-pin CY8C29466-24PXI PDIP PSoC device samples (two)
- PSoC Designer software CD
- ISSP cable
- MiniEval socket programming and evaluation board
- Backward compatibility cable (for connecting to legacy pods)
- Universal 110/220 power supply (12 V)
- European plug adapter
- USB 2.0 cable
- Getting Started guide
- Development kit registration form

CY3280-22X45 Universal CapSense Controller Board

The CY3280-22X45 controller board is an additional controller board for the CY3280-BK1 Universal CapSense Controller Kit. The Universal CapSense Controller kit is designed for easy prototyping and debug of CapSense designs with pre-defined control circuitry and plug-in hardware. The CY3280-22X45 kit contains no plug-in hardware. Therefore, it is only usable if plug-in hardware is purchased as part of the CY3280-BK1 kit or other separate kits. The kit includes:

- CY3280-22X45 universal CapSense controller board
- CY3280-22X45 universal CapSense controller board CD
- DC power supply
- Printed documentation

CY3280-CPM1 CapSensePlus Module

The CY3280-CPM1 CapSensePlus Module is a plug-in module board for the CY3280-22X45 CapSense controller board kit. This plug-in module has no capacitive sensors on it. Instead, it has other general circuitry (such as a seven-segment display, potentiometer, LEDs, buttons, thermistor) that can be used to develop applications that require capacitive sensing along with other additional functionality. To use this kit, a CY3280-22X45 kit is required.

Evaluation Tools

All evaluation tools can be purchased from the Cypress online store. The online store also has the most up-to-date information on kit contents, descriptions, and availability.

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-pin CY8C29466-24PXI PDIP PSoC device sample (two)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable



Packaging Information

This section provides the packaging specifications for the automotive CY8C21x45 and CY8C22x45 PSoC devices. The thermal impedances for each package and the typical package capacitance on crystal pins are given.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Package Dimensions





DIMENSIONS IN MILLIMETERS MIN. MAX.



51-85079 *E



Figure 13. 48-pin SSOP (300 Mils) Carrier Tape, 51-51104

NOTES:

- 1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
- CAMBER IN COMPLIANCE WITH EIA 481
 POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE



51-51104 *E

Table 30. Tape and Reel Specifications

Package	Cover Tape Width (mm)	Hub Size (inches)	Minimum Leading Empty Pockets	Minimum Trailing Empty Pockets	Standard Full Reel Quantity
28-pin SSOP	13.3	7	42	25	1000
48-pin SSOP	25.5	4	32	19	1000



Tube Information

Figure 14. 28-pin SSOP, 32-pin SOIC (450 Mils Body) Shipping Tube, 51-51029



- NOTE: 1. MARK "ANTISTATIC" WITH 3.0mm HIGH AND 25.4±0.5mm LENGTH IN BLUE COLOR 2. ALL DIMENSIONS ARE IN MILLIMETERS. 3. TUBE MATERIAL : PAR 48 5. WHITE PLUG NEED COMPLETELY INSERT TO TUBE BEFORE SHIPPING AND THE TIP ALIGN WITH TUBE EDGE. 6. THE BLUE PLUG ENCLOSE TOGETHER WITH THE SHIPMENT. 7. 25 UNTS PER TUBE. 8. TUBE PART NUMBER WITH SLOT : STB450-R , STB450-BL



51-51029 *E



Document Conventions

Units of Measure

Table 32 lists the units of measure that are used in this document.

Table 32. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kВ	1024 bytes	ms	millisecond
°C	degree Celsius	mV	millivolt
kHz	kilohertz	nA	nanoampere
kΩ	kilohm	ns	nanosecond
LSbit	least-significant bit	W	ohm
MHz	megahertz	%	percent
μA	microampere	pF	picofarad
μs	microsecond	ps	picosecond
μV	microvolt	pА	picoampere
mA	milliampere	V	volt
mm	millimeter	W	watt

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimals.

Glossary

active high	 A logic signal having its asserted state as the logic 1 state. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	 The frequency range of a message or information processing system measured in hertz. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value.
	2. The amount by which the average of a set of values departs from a reference value.
	3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.



Glossary (continued)

external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I ² C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams.
	The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the <i>slave device</i> .
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.



Glossary (continued)

modulator	A device that imposes a signal on a carrier.
noise	 A disturbance that affects a signal and that may distort the information carried by the signal. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC [®]	Cypress Semiconductor's PSoC [®] is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	 Pertaining to a process in which all events occur one after the other. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.



Errata

This section describes the errata for the CY8C21x45, CY8C22x45 family of PSoC devices. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CY8C21345	All Variants
CY8C21645	All Variants
CY8C22345	All Variants
CY8C22645	All Variants

CY8C21x45, CY8C22x45 Qualification Status

Product Status: In Production

Errata Summary

The following table defines the errata applicable for this PSoC family device.

Items	Part Number	Silicon Revision	Fix Status
1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC	All CY8C21x45, CY8C22x45 devices affected	All	Silicon fix not planned. Use workaround.
2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	All CY8C21x45, CY8C22x45 devices affected	All	Silicon fix not planned. Use workaround.

1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC

Problem Definition

In free running mode, there can be a variation of up to 7 LSB in the digital output of SAR10 ADC.

Parameters Affected

Code Variation. This is not a specified parameter.

It is defined as the number of unique output codes generated by the ADC for a given constant input voltage, in addition to the correct code. For example, for an input voltage of 2.000 V, the expected code is 190hex and the ADC generates three codes: 191hex, 190hex, and 192hex. The code variation is 2 LSB.

Trigger Condition(S)

SAR10 ADC is configured in the free running mode. When ADC is operated in free running mode, for a constant input voltage output of ADC can have a variation of up to 7LSB. This can be resolved by using the averaging technique or by disabling the free running mode before reading the data and enabling again after reading the data.

Scope of Impact

Inaccurate output is possible.

Workaround

This issue can be averted by using one or both of the following workarounds. Consult a Cypress representative for additional assistance.

- Use the averaging technique. That is, take multiple samples of the input, and use a digital averaging filter.
- Disable the free running mode before reading data out, and enable the free running mode after completing the read operation.

Fix Status

No silicon fix is planned.



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