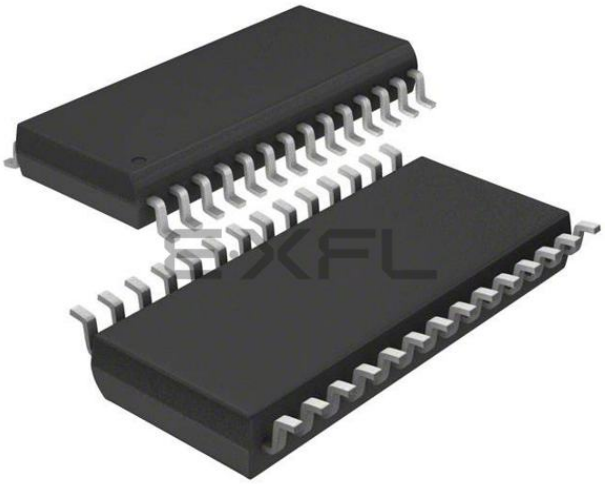


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | M8C |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 24 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.75V ~ 5.25V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21345-12pvxet |

**C Language Compilers**. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

*Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

*Online Help System*

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

*In-Circuit Emulator*

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

## Designing with PSoC Designer

The development process for the PSoC® device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

### Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

### Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

## Pinouts

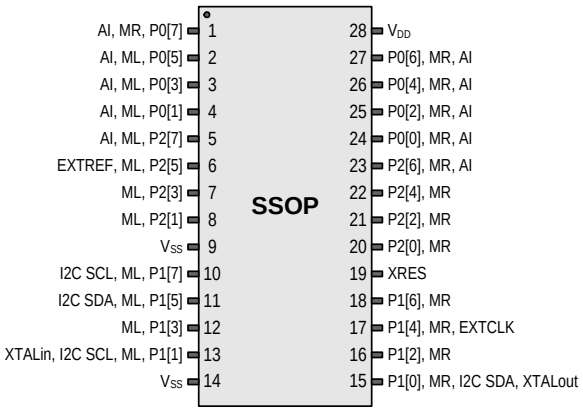
The automotive CY8C21x45 and CY8C22x45 PSoC devices are available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog mux bus. However, $V_{SS}$, $V_{DD}$, and XRES are not capable of digital I/O.

### 28-pin Part Pinout

**Table 2. 28-pin Part Pinout (SSOP)**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I, MR | P0[7] | Analog column mux input, $C_{MOD}$ capacitor pin |
| 2 | I/O | I, ML | P0[5] | Analog column mux input, $C_{MOD}$ capacitor pin |
| 3 | I/O | I, ML | P0[3] | Analog column mux input |
| 4 | I/O | I, ML | P0[1] | Analog column mux input |
| 5 | I/O | I, ML | P2[7] | Direct input to analog block |
| 6 | I/O | ML | P2[5] | Optional SAR ADC external reference (EXTREF) |
| 7 | I/O | ML | P2[3] | |
| 8 | I/O | ML | P2[1] | |
| 9 | Power | | $V_{SS}$ | Ground connection |
| 10 | I/O | ML | P1[7] | $I^2C$ serial clock (SCL) |
| 11 | I/O | ML | P1[5] | $I^2C$ serial data (SDA) |
| 12 | I/O | ML | P1[3] | |
| 13 | I/O | ML | P1[1] | Crystal input (XTALin), $I^2C$ SCL, ISSP-SCLK[5] |
| 14 | Power | | $V_{SS}$ | Ground connection |
| 15 | I/O | MR | P1[0] | Crystal output (XTALout), $I^2C$ SDA, ISSP-SDATA[5] |
| 16 | I/O | MR | P1[2] | |
| 17 | I/O | MR | P1[4] | Optional external clock input (EXTCLK) |
| 18 | I/O | MR | P1[6] | |
| 19 | Input | | XRES | Active high external reset with internal pull-down |
| 20 | I/O | MR | P2[0] | |
| 21 | I/O | MR | P2[2] | |
| 22 | I/O | MR | P2[4] | |
| 23 | I/O | I, MR | P2[6] | Direct input to analog block |
| 24 | I/O | I, MR | P0[0] | Analog column mux input |
| 25 | I/O | I, MR | P0[2] | Analog column mux input |
| 26 | I/O | I, MR | P0[4] | Analog column mux input |
| 27 | I/O | I, MR | P0[6] | Analog column mux input |
| 28 | Power | | $V_{DD}$ | Supply voltage |

**Figure 3. CY8C21345 and CY8C22345 28-pin PSoC Device**




**LEGEND**: A = Analog, I = Input, O = Output, MR= Right analog mux bus input, ML= Left analog mux bus input.

**Note**
5. These are the ISSP pins, which are not High Z after exiting a reset state. See the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for details.

**Table 3. 48-pin Part Pinout (SSOP)** (continued)

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 43 | I/O | I, MR | P2[6] | Direct input to analog block |
| 44 | I/O | I, MR | P0[0] | Analog column mux input |
| 45 | I/O | I, MR | P0[2] | Analog column mux input |
| 46 | I/O | I, MR | P0[4] | Analog column mux input |
| 47 | I/O | I, MR | P0[6] | Analog column mux input |
| 48 | Power | | $V_{DD}$ | Supply voltage |

**LEGEND**: A = Analog, I = Input, O = Output, MR= Right analog mux bus input, ML= Left analog mux bus input

## Registers

This section lists the registers of this PSoC device family by mapping tables. For detailed register information, refer to the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices.

### Register Conventions

The register conventions specific to this section are listed in the following table.

**Table 4. Abbreviations**

| Convention | Description |
|---|---|
| RW | Read and write register or bit(s) |
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

### Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are Reserved and must not be accessed.

**Table 5. Register Map Bank 0 Table: User Space**

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0GS | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1GS | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DR | 08 | RW | | 48 | | | 88 | | PWMVREF0 | C8 | # |
| PRT2IE | 09 | RW | | 49 | | | 89 | | PWMVREF1 | C9 | # |
| PRT2GS | 0A | RW | | 4A | | | 8A | | IDAC_MODE | CA | RW |
| PRT2DM2 | 0B | RW | | 4B | | | 8B | | PWM_SRC | CB | # |
| PRT3DR | 0C | RW | | 4C | | | 8C | | TS_CR0 | CC | RW |
| PRT3IE | 0D | RW | | 4D | | | 8D | | TS_CMPH | CD | RW |
| PRT3GS | 0E | RW | | 4E | | | 8E | | TS_CMPL | CE | RW |
| PRT3DM2 | 0F | RW | | 4F | | | 8F | | TS_CR1 | CF | RW |
| PRT4DR | 10 | RW | CSD0_DR0_L | 50 | R | | 90 | | CUR PP | D0 | RW |
| PRT4IE | 11 | RW | CSD0_DR1_L | 51 | W | | 91 | | STK_PP | D1 | RW |
| PRT4GS | 12 | RW | CSD0_CNT_L | 52 | R | | 92 | | | D2 | |
| PRT4DM2 | 13 | RW | CSD0_CR0 | 53 | # | | 93 | | IDX_PP | D3 | RW |
| | 14 | | CSD0_DR0_H | 54 | R | | 94 | | MVR_PP | D4 | RW |
| | 15 | | CSD0_DR1_H | 55 | W | | 95 | | MVW_PP | D5 | RW |
| | 16 | | CSD0_CNT_H | 56 | R | | 96 | | I2C0_CFG | D6 | RW |
| | 17 | | CSD0_CR1 | 57 | RW | | 97 | | I2C0_SCR | D7 | # |
| | 18 | | CSD1_DR0_L | 58 | R | | 98 | | I2C0_DR | D8 | RW |
| | 19 | | CSD1_DR1_L | 59 | W | | 99 | | I2C0_MSCR | D9 | # |
| | 1A | | CSD1_CNT_L | 5A | R | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | CSD1_CR0 | 5B | # | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | CSD1_DR0_H | 5C | R | | 9C | | INT_CLR2 | DC | RW |
| | 1D | | CSD1_DR1_H | 5D | W | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | CSD1_CNT_H | 5E | R | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | CSD1_CR1 | 5F | RW | | 9F | | INT_MSK2 | DF | RW |
| DBC00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBC00DR1 | 21 | W | AMUX_CFG | 61 | RW | | A1 | | INT_MSK1 | E1 | RW |
| DBC00DR2 | 22 | RW | PWM_CR | 62 | RW | | A2 | | INT_VC | E2 | RC |
| DBC00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBC01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | | | |
| DBC01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | | | |
| DBC01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC _CR0 | E6 | RW |
| DBC01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCC02DR0 | 28 | # | ADC0_CR | 68 | # | | A8 | | MUL0_X | E8 | W |
| DCC02DR1 | 29 | W | ADC1_CR | 69 | # | | A9 | | MUL0_Y | E9 | W |
| DCC02DR2 | 2A | RW | SADC_DH | 6A | RW | | AA | | MUL0_DH | EA | R |
| DCC02CR0 | 2B | # | SADC_DL | 6B | RW | | AB | | MUL0_DL | EB | R |
| DCC03DR0 | 2C | # | TMP_DR0 | 6C | RW | | AC | | ACC0_DR1 | EC | RW |
| DCC03DR1 | 2D | W | TMP_DR1 | 6D | RW | | AD | | ACC0_DR0 | ED | RW |
| DCC03DR2 | 2E | RW | TMP_DR2 | 6E | RW | | AE | | ACC0_DR3 | EE | RW |
| DCC03CR0 | 2F | # | TMP_DR3 | 6F | RW | | AF | | ACC0_DR2 | EF | RW |
| DBC10DR0 | 30 | # | | 70 | | RDI0RI | B0 | RW | | F0 | |
| DBC10DR1 | 31 | W | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| DBC10DR2 | 32 | RW | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| DBC10CR0 | 33 | # | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBC11DR0 | 34 | # | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| DBC11DR1 | 35 | W | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| DBC11DR2 | 36 | RW | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| DBC11CR0 | 37 | # | ACE01CR2 | 77 | RW | RDI0DSM | B7 | RW | CPU_F | F7 | RL |
| DCC12DR0 | 38 | # | | 78 | | RDI1RI | B8 | RW | | F8 | |
| DCC12DR1 | 39 | W | | 79 | | RDI1SYN | B9 | RW | | F9 | |
| DCC12DR2 | 3A | RW | | 7A | | RDI1IS | BA | RW | | FA | |
| DCC12CR0 | 3B | # | | 7B | | RDI1LT0 | BB | RW | | FB | |
| DCC13DR0 | 3C | # | | 7C | | RDI1LT1 | BC | RW | IDACR_D | FC | RW |
| DCC13DR1 | 3D | W | | 7D | | RDI1RO0 | BD | RW | IDACL_D | FD | RW |
| DCC13DR2 | 3E | RW | | 7E | | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| DCC13CR0 | 3F | # | | 7F | | RDI1DSM | BF | RW | CPU_SCR0 | FF | # |

**Blank fields are Reserved and must not be accessed.** **# Access is bit specific.**

## DC Electrical Characteristics

*DC Chip Level Specifications*

Table 9 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 9. DC Chip Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage<br>A-grade devices<br>E-grade devices | <br>3.0<br>4.75 | <br>–<br>– | <br>5.25<br>5.25 | <br>V<br>V | See Table 15 on page 19 |
| $I_{DD}$ | Supply current<br>A-grade devices, 3.0 V ≤ $V_{DD}$ ≤ 3.6 V<br>A-grade devices, 4.75 V ≤ $V_{DD}$ ≤ 5.25 V<br>E-grade devices | <br>–<br>–<br>– | <br>4<br>7<br>8 | <br>7<br>12<br>15 | <br>mA<br>mA<br>mA | CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, Analog blocks disabled |
| $I_{SB}$ | Sleep (mode) current<br>A-grade devices, 3.0 V ≤ $V_{DD}$ ≤ 3.6 V<br>A-grade devices, 4.75 V ≤ $V_{DD}$ ≤ 5.25 V<br>E-grade devices | <br>–<br>–<br>– | <br>3<br>4<br>4 | <br>12<br>25<br>25 | <br>µA<br>µA<br>µA | Everything disabled except ILO, POR, LVD, Sleep Timer, and WDT circuits |
| $I_{SBXTL}$ | Sleep (mode) current with ECO<br>A-grade devices, 3.0 V ≤ $V_{DD}$ ≤ 3.6 V<br>A-grade devices, 4.75 V ≤ $V_{DD}$ ≤ 5.25 V<br>E-grade devices | <br>–<br>–<br>– | <br>4<br>5<br>5 | <br>13<br>26<br>26 | <br>µA<br>µA<br>µA | Everything disabled except ECO, POR, LVD, Sleep Timer, and WDT circuits |
| $V_{REF}$ | Reference voltage (Bandgap) | 1.275 | 1.30 | 1.325 | V | Trimmed for appropriate $V_{DD}$ setting. |

*DC GPIO Specifications*

Table 10 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 10. DC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull-down resistor | 4 | 5.6 | 8 | kΩ | Also applies to the internal pull-down resistor on the XRES pin |
| $V_{OH}$ | High output level | $V_{DD}$ – 1.0 | – | – | V | $I_{OH}$ = 10 mA, $V_{DD}$ = 4.75 to 5.25 V (80 mA maximum combined $I_{OH}$ budget) |
| $V_{OL}$ | Low output level | – | – | 0.75 | V | $I_{OL}$ = 25 mA, $V_{DD}$ = 4.75 to 5.25 V (100 mA maximum combined $I_{OL}$ budget) |
| | | – | – | 0.65 | V | $I_{OL}$ = 5 mA, $V_{DD}$ = 3.0 to 3.6 V |
| $I_{OH}$ | High-level source current | 10 | – | – | mA | $V_{OH} \geq V_{DD}$ – 1.0 V, see the limitations of the total current in the note for $V_{OH}$. |
| $I_{OL}$ | Low-level sink current | 25 | – | – | mA | $V_{OL} \leq 0.75$ V, see the limitations of the total current in the note for $V_{OL}$. |
| $V_{IL}$ | Input low level | – | – | 0.8 | V | |
| $V_{IH}$ | Input high level | 2.1 | – | | V | |
| $V_H$ | Input hysteresis | – | 60 | – | mV | |
| $I_{IL}$ | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 μA |
| $C_{IN}$ | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent. $T_A$ = 25 °C |
| $C_{OUT}$ | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent. $T_A$ = 25 °C |

*DC Operational Amplifier Specifications*

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25°C, unless specified otherwise, and are for design guidance only.

**Table 11. DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input offset voltage (absolute value) | – | 2.5 | 15 | mV | |
| $I_{SOA}$ | Supply current (absolute value)<br>A-grade devices<br>E-grade devices | <br>–<br>– | <br>–<br>– | <br>30<br>35 | <br>µA<br>µA | |
| $TCV_{OSOA}$ | Average input offset voltage drift | – | 10 | – | µV/°C | |
| $I_{EBOA}$[7] | Input leakage current (Port 0 analog pins) | – | 200 | – | pA | Gross tested to 1 µA |
| $C_{INOA}$ | Input capacitance (Port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. $T_A$ = 25 °C |
| $V_{CMOA}$ | Common mode voltage range | 0.5 | – | $V_{DD}$ – 1 | V | |

*DC IDAC Specifications*

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 12. DC IDAC Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $IDAC_{GAIN}$ | IDAC gain | – | 75.4 | 218 | nA/bit | IDAC gain at 1x current gain |
| | | – | 335 | 693 | nA/bit | IDAC gain at 4x current gain |
| | | – | 1160 | 2410 | nA/bit | IDAC gain at 16x current gain |
| | | – | 2340 | 5700 | nA/bit | IDAC gain at 32x current gain |
| | Monotonicity | No | – | – | – | IDAC gain is non-monotonous at step intervals of (0x10) |
| $IDAC_{GAIN\_VAR}$ | IDAC gain variation over temperature –40 °C to 85 °C | – | 3.22 | – | nA | at 1x current gain |
| | | – | 18.1 | – | nA | at 4x current gain |
| | | – | 59.9 | – | nA | at 16x current gain |
| | | – | 120 | – | nA | at 32x current gain |
| $I_{IDAC}$ | IDAC current at maximum code (0xFF) | – | 19.2 | – | µA | at 1x current gain |
| | | – | 85.4 | – | µA | at 4x current gain |
| | | – | 295 | – | µA | at 16x current gain |
| | | – | 596 | – | µA | at 32x current gain |

**Note**
7. Atypical behavior: $I_{EBOA}$ of Port 0 Pin 0 is below 1 nA at 25 °C; 50 nA over temperature. Use Port 0 Pins 1 – 7 for the lowest leakage of 200 nA.

*DC Programming Specifications*

Table 16 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 16. DC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{DDP}$ | $V_{DD}$ for programming and erase | 4.5 | 5 | 5.5 | V | This specification applies to the functional requirements of external programmer tools |
| $V_{DDLV}$ | Low $V_{DD}$ for verify<br>A-grade devices<br>E-grade devices | <br>3.0<br>4.7 | <br>3.1<br>4.8 | <br>3.2<br>4.9 | <br>V<br>V | This specification applies to the functional requirements of external programmer tools |
| $V_{DDHV}$ | High $V_{DD}$ for verify | 5.1 | 5.2 | 5.3 | V | This specification applies to the functional requirements of external programmer tools |
| $V_{DDIWRITE}$ | Supply voltage for flash write operation<br>A-grade devices<br>E-grade devices | <br>3.0<br>4.75 | <br>–<br>– | <br>5.25<br>5.25 | <br>V<br>V | This specification applies to this device when it is executing internal flash writes |
| $I_{DDP}$ | Supply current during programming or verify | – | 5 | 25 | mA | |
| $V_{ILP}$ | Input low voltage during programming or verify | – | – | 0.8 | V | |
| $V_{IHP}$ | Input high voltage during programming or verify | 2.2 | – | – | V | |
| $I_{ILP}$ | Input current when applying $V_{ILP}$ to P1[0] or P1[1] during programming or verify | – | – | 0.2 | mA | Driving internal pull-down resistor |
| $I_{IHP}$ | Input current when applying $V_{IHP}$ to P1[0] or P1[1] during programming or verify | – | – | 1.5 | mA | Driving internal pull-down resistor |
| $V_{OLV}$ | Output low voltage during programming or verify | – | – | 0.75 | V | |
| $V_{OHV}$ | Output high voltage during programming or verify | $V_{DD}$ – 1.0 | – | $V_{DD}$ | V | |
| $Flash_{ENPB}$ | Flash endurance (per block) [8, 9]<br>A-grade devices<br>E-grade devices | <br>1,000<br>100 | <br>–<br>– | <br>–<br>– | <br>–<br>– | Erase/write cycles per block |
| $Flash_{ENT}$ | Flash endurance (total) [9, 10]<br>CY8C21x45 A-grade devices<br>CY8C22x45 A-grade devices<br>CY8C21x45 E-grade devices<br>CY8C22x45 E-grade devices | <br>128,000<br>256,000<br>12,800<br>25,600 | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | Erase/write cycles |
| $Flash_{DR}$ | Flash data retention [9]<br>A-grade devices<br>E-grade devices | <br>10<br>10 | <br>–<br>– | <br>–<br>– | <br>Years<br>Years | |

**Notes**

8. The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
10. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.

## AC Electrical Characteristics

*AC Chip Level Specifications*

The following tables list the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 17. AC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{IMO24}$ | Internal main oscillator frequency for 24 MHz<br>A-grade devices, 4.75 V ≤ $V_{DD}$ ≤ 5.25 V<br>A-grade devices, 3.0 V ≤ $V_{DD}$ ≤ 3.6 V<br>E-grade devices | <br>22.8<br>22.5<br>22.3 | <br>24<br>24<br>24 | <br>25.2 [11]<br>25.5 [11]<br>25.7 [11] | <br>MHz<br>MHz<br>MHz | Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 7 on page 14. |
| $F_{IMO6}$ | Internal main oscillator frequency for 6 MHz<br>A-grade devices<br>E-grade devices | <br>5.5<br>5.5 | <br>6<br>6 | <br>6.5 [11]<br>6.5 [11] | <br>MHz<br>MHz | Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 7 on page 14. |
| $F_{CPU1}$ | CPU frequency (5 V $V_{DD}$ operation)<br>A-grade devices<br>E-grade devices | <br>0.089<br>0.089 | <br>–<br>– | <br>25.2 [11]<br>12.6 [11] | <br>MHz<br>MHz | SLIMO mode = 0. |
| $F_{CPU2}$ | CPU frequency (3.3 V $V_{DD}$ operation) | 0.089 | – | 12.6 [11] | MHz | A-grade devices only.<br>SLIMO mode = 0. |
| $F_{BLK5}$ | Digital PSoC block frequency (5 V $V_{DD}$ operation)<br>A-grade devices<br>E-grade devices | <br>0<br>0 | <br>48<br>24 | <br>50.4 [11, 12]<br>25.2 [11, 12] | <br>MHz<br>MHz | Refer to Table 20 on page 24. |
| $F_{BLK33}$ | Digital PSoC block frequency (3.3 V $V_{DD}$ operation) | 0 | 24 | 24.6 [11] | MHz | A-grade devices only |
| $F_{32K1}$ | ILO frequency | 15 | 32 | 75 | kHz | This specification applies when the ILO has been trimmed. |
| $F_{32KU}$ | ILO untrimmed frequency | 5 | – | 100 | kHz | After a reset and before the M8C processor starts to execute, the ILO is not trimmed. |
| $t_{XRST}$ | External reset pulse width | 10 | – | – | µs | |
| DC24M | 24 MHz duty cycle | 40 | 50 | 60 | % | |
| $DC_{ILO}$ | ILO duty cycle | 20 | 50 | 80 | % | |
| Fout48M | 48 MHz output frequency | 45.6 | 48.0 | 50.4 [11] | MHz | |
| $F_{MAX}$ | Maximum frequency of signal on row input or row output | – | – | 12.6 | MHz | |
| $SR_{POWERUP}$ | Power supply slew rate | – | – | 250 | V/ms | $V_{DD}$ slew rate during power-up. |
| $t_{POWERUP}$ | Time between end of POR state and CPU code execution | – | 16 | 100 | ms | Power-up from 0 V. |

**Notes**
11. Accuracy derived from IMO with appropriate trim for $V_{DD}$ range
12. Refer to the individual user module data sheets for information on maximum frequencies for user modules.

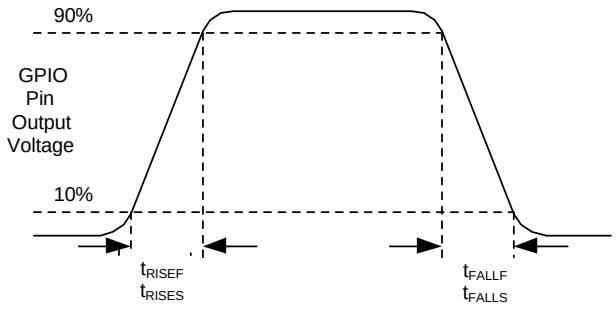
*AC GPIO Specifications*

Table 18 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 18. AC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO operating frequency | 0 | – | 12.6 | MHz | Normal strong mode |
| $t_{RISEF}$ | Rise time, normal strong mode, Cload = 50 pF<br>A-grade devices<br>E-grade devices | <br>3<br>3 | <br>–<br>– | <br>18<br>24 | <br>ns<br>ns | Refer to Figure 8 |
| $t_{FALLF}$ | Fall time, normal strong mode, Cload = 50 pF<br>A-grade devices<br>E-grade devices | <br>2<br>2 | <br>–<br>– | <br>18<br>28 | <br>ns<br>ns | Refer to Figure 8 |
| $t_{RISES}$ | Rise time, slow strong mode, Cload = 50 pF<br>A-grade devices<br>E-grade devices | <br>7<br>7 | <br>27<br>32 | <br>–<br>– | <br>ns<br>ns | Refer to Figure 8 |
| $t_{FALLS}$ | Fall time, slow strong mode, Cload = 50 pF<br>A-grade devices<br>E-grade devices | <br>7<br>7 | <br>22<br>28 | <br>–<br>– | <br>ns<br>ns | Refer to Figure 8 |

**Figure 8. GPIO Timing Diagram**




*AC Operational Amplifier Specifications*

Table 19 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 19. AC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{COMP}$ | Comparator mode response time, 50 mV | – | – | 100 | ns | |

**Table 20. AC Digital Block Specifications** (continued)

| Function | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Transmitter | Input Clock Frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75$ V, 2 Stop Bits | – | – | 50.4 [15] | MHz | |
| | $V_{DD} \geq 4.75$ V, 1 Stop Bit | – | – | 25.2 [15] | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 25.2 [15] | MHz | |
| Receiver | Input Clock Frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75$ V, 2 Stop Bits | – | – | 50.4 [15] | MHz | |
| | $V_{DD} \geq 4.75$ V, 1 Stop Bit | – | – | 25.2 [15] | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 25.2 [15] | MHz | |

**Note**
15. Accuracy derived from IMO with appropriate trim for $V_{DD}$ range.

*AC Programming Specifications*

Table 23 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 23. AC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{RSCLK}$ | Rise time of SCLK | 1 | – | 20 | ns | |
| $t_{FSCLK}$ | Fall time of SCLK | 1 | – | 20 | ns | |
| $t_{SSCLK}$ | Data setup time to falling edge of SCLK | 40 | – | – | ns | |
| $t_{HSCLK}$ | Data hold time from falling edge of SCLK | 40 | – | – | ns | |
| $F_{SCLK}$ | Frequency of SCLK | 0 | – | 8 | MHz | |
| $F_{SCLK3}$ | Frequency of SCLK | 0 | – | 6 | MHz | $V_{DD} \leq 3.6$ V |
| $t_{ERASEB}$ | Flash erase time (block) | – | 10 | 40 [16] | ms | |
| $t_{WRITE}$ | Flash block write time | – | 40 | 160 [16] | ms | |
| $t_{DSCLK}$ | Data out delay from falling edge of SCLK | – | – | 55 | ns | $V_{DD} > 3.6$ V, 30 pF load |
| $t_{DSCLK3}$ | Data out delay from falling edge of SCLK | – | – | 65 | ns | 3.0 V $\leq V_{DD} \leq$ 3.6 V, 30 pF load |
| $t_{PRGH}$ | Total flash block program time ($t_{ERASEB} + t_{WRITE}$), hot | – | – | 100 [16] | ms | $T_J \geq 0$ °C |
| $t_{PRGC}$ | Total flash block program time ($t_{ERASEB} + t_{WRITE}$), cold | – | – | 200 [16] | ms | $T_J < 0$ °C |

**Note**
16. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.

## Development Tool Selection

This section presents the development tools available for the automotive CY8C21x45 and CY8C22x45 families.

### Software

*PSoC Designer*

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

*PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

### Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

*CY3215-DK Basic Development Kit*

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the contents of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- ICE-Cube unit
- 28-pin PDIP emulation pod for CY8C29466-24PXI
- 28-pin CY8C29466-24PXI PDIP PSoC device samples (two)
- PSoC Designer software CD
- ISSP cable
- MiniEval socket programming and evaluation board
- Backward compatibility cable (for connecting to legacy pods)
- Universal 110/220 power supply (12 V)
- European plug adapter
- USB 2.0 cable
- Getting Started guide
- Development kit registration form

*CY3280-22X45 Universal CapSense Controller Board*

The CY3280-22X45 controller board is an additional controller board for the CY3280-BK1 Universal CapSense Controller Kit. The Universal CapSense Controller kit is designed for easy prototyping and debug of CapSense designs with pre-defined control circuitry and plug-in hardware. The CY3280-22X45 kit contains no plug-in hardware. Therefore, it is only usable if plug-in hardware is purchased as part of the CY3280-BK1 kit or other separate kits. The kit includes:

- CY3280-22X45 universal CapSense controller board
- CY3280-22X45 universal CapSense controller board CD
- DC power supply
- Printed documentation

*CY3280-CPM1 CapSensePlus Module*

The CY3280-CPM1 CapSensePlus Module is a plug-in module board for the CY3280-22X45 CapSense controller board kit. This plug-in module has no capacitive sensors on it. Instead, it has other general circuitry (such as a seven-segment display, potentiometer, LEDs, buttons, thermistor) that can be used to develop applications that require capacitive sensing along with other additional functionality. To use this kit, a CY3280-22X45 kit is required.

### Evaluation Tools

All evaluation tools can be purchased from the Cypress online store. The online store also has the most up-to-date information on kit contents, descriptions, and availability.

*CY3210-PSoCEval1*

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-pin CY8C29466-24PXI PDIP PSoC device sample (two)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

## Ordering Information

The following table lists the key package features and ordering codes of the automotive CY8C21x45 and CY8C22x45 device families.

**Table 26. PSoC Device Family Key Features and Ordering Information**

| Package | Ordering Code | Flash (Bytes) | SRAM (Bytes) | Temperature Range | Digital Blocks | Analog Blocks | Digital I/O Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---|---|---|---|---|---|---|---|---|---|---|
| 28-pin (210-Mil) SSOP | CY8C21345-24PVXA | 8 K | 512 | –40 °C to +85 °C | 4 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP (Tape and Reel) | CY8C21345-24PVXAT | 8 K | 512 | –40 °C to +85 °C | 4 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP | CY8C21345-12PVXE | 8 K | 512 | –40 °C to +125 °C | 4 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP (Tape and Reel) | CY8C21345-12PVXET | 8 K | 512 | –40 °C to +125 °C | 4 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP | CY8C22345-24PVXA | 16 K | 1 K | –40 °C to +85 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP (Tape and Reel) | CY8C22345-24PVXAT | 16 K | 1 K | –40 °C to +85 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP | CY8C22345H-24PVXA | 16 K | 1 K | –40 °C to +85 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP (Tape and Reel) | CY8C22345H-24PVXAT | 16 K | 1 K | –40 °C to +85 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP | CY8C22345-12PVXE | 16 K | 1 K | –40 °C to +125 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 28-pin (210-Mil) SSOP (Tape and Reel) | CY8C22345-12PVXET | 16 K | 1 K | –40 °C to +125 °C | 8 | 6 | 24 | 24 | 0 | Yes |
| 48-pin (300-Mil) SSOP | CY8C21645-24PVXA | 8 K | 512 | –40 °C to +85 °C | 4 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP (Tape and Reel) | CY8C21645-24PVXAT | 8 K | 512 | –40 °C to +85 °C | 4 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP | CY8C21645-12PVXE | 8 K | 512 | –40 °C to +125 °C | 4 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP (Tape and Reel) | CY8C21645-12PVXET | 8 K | 512 | –40 °C to +125 °C | 4 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP | CY8C22645-24PVXA | 16 K | 1 K | –40 °C to +85 °C | 8 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP (Tape and Reel) | CY8C22645-24PVXAT | 16 K | 1 K | –40 °C to +85 °C | 8 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP | CY8C22645-12PVXE | 16 K | 1 K | –40 °C to +125 °C | 8 | 6 | 38 | 38 | 0 | Yes |
| 48-pin (300-Mil) SSOP (Tape and Reel) | CY8C22645-12PVXET | 16 K | 1 K | –40 °C to +125 °C | 8 | 6 | 38 | 38 | 0 | Yes |

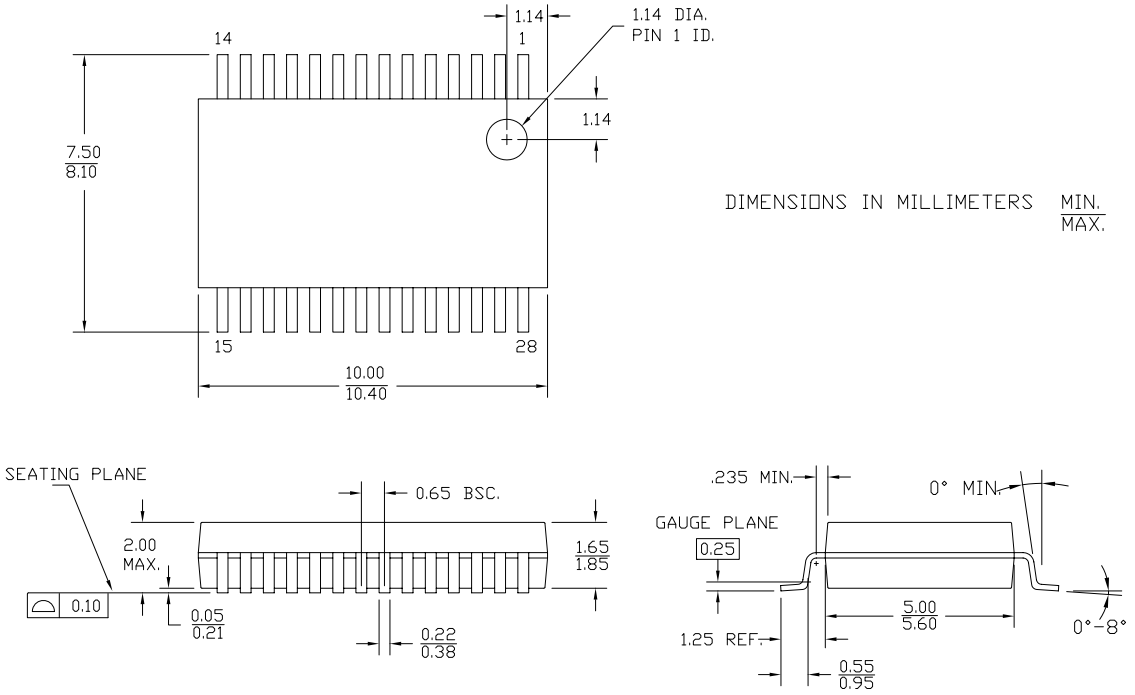
## Packaging Information

This section provides the packaging specifications for the automotive CY8C21x45 and CY8C22x45 PSoC devices. The thermal impedances for each package and the typical package capacitance on crystal pins are given.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

### Package Dimensions

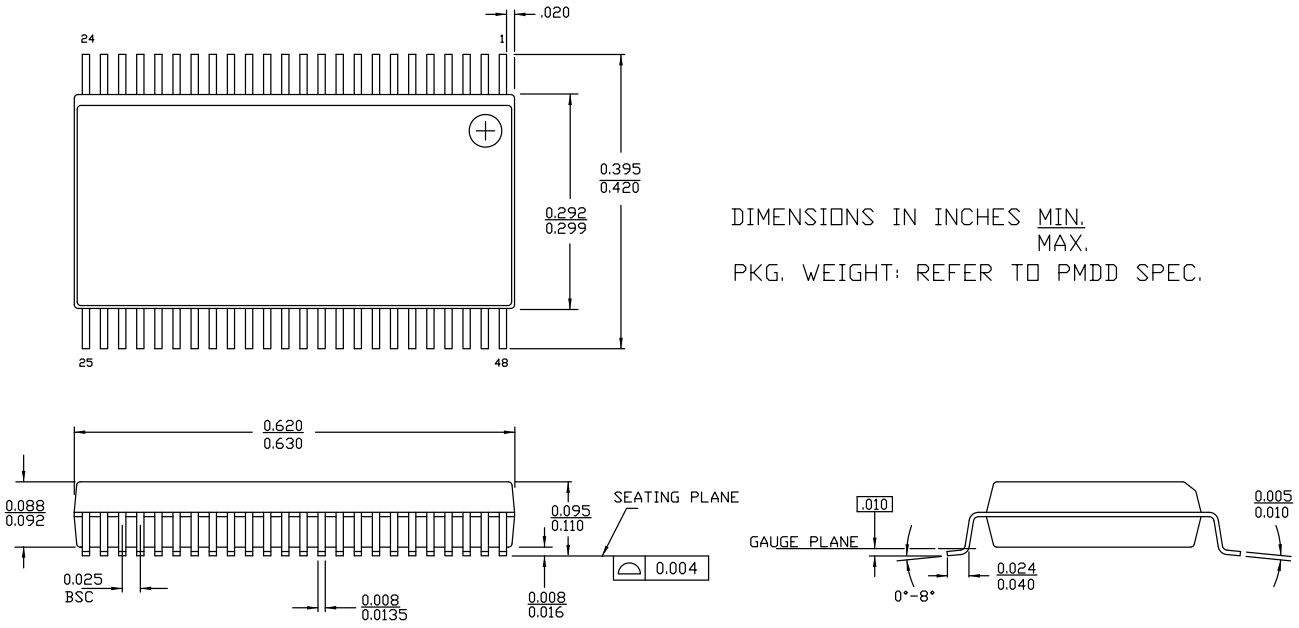
**Figure 10. 28-pin SSOP (210 Mils) Package Outline, 51-85079**




51-85079 *E

## Packaging Information (continued)

**Figure 11. 48-pin SSOP (300 Mils) Package Outline, 51-85061**




### Thermal Impedances

**Table 27. Thermal Impedances per Package**

| Package | Typical $\theta_{JA}$ [22] |
|---|---|
| 28-pin SSOP | 97.6 °C/W |
| 48-pin SSOP | 69 °C/W |

### Capacitance on Crystal Pins

**Table 28. Typical Package Capacitance on Crystal Pins**

| Package | Package Capacitance |
|---|---|
| 28-pin SSOP | 2.8 pF |
| 48-pin SSOP | 3.3 pF |

### Solder Reflow Specifications

Table 29 shows the solder reflow temperature limits that must not be exceeded.

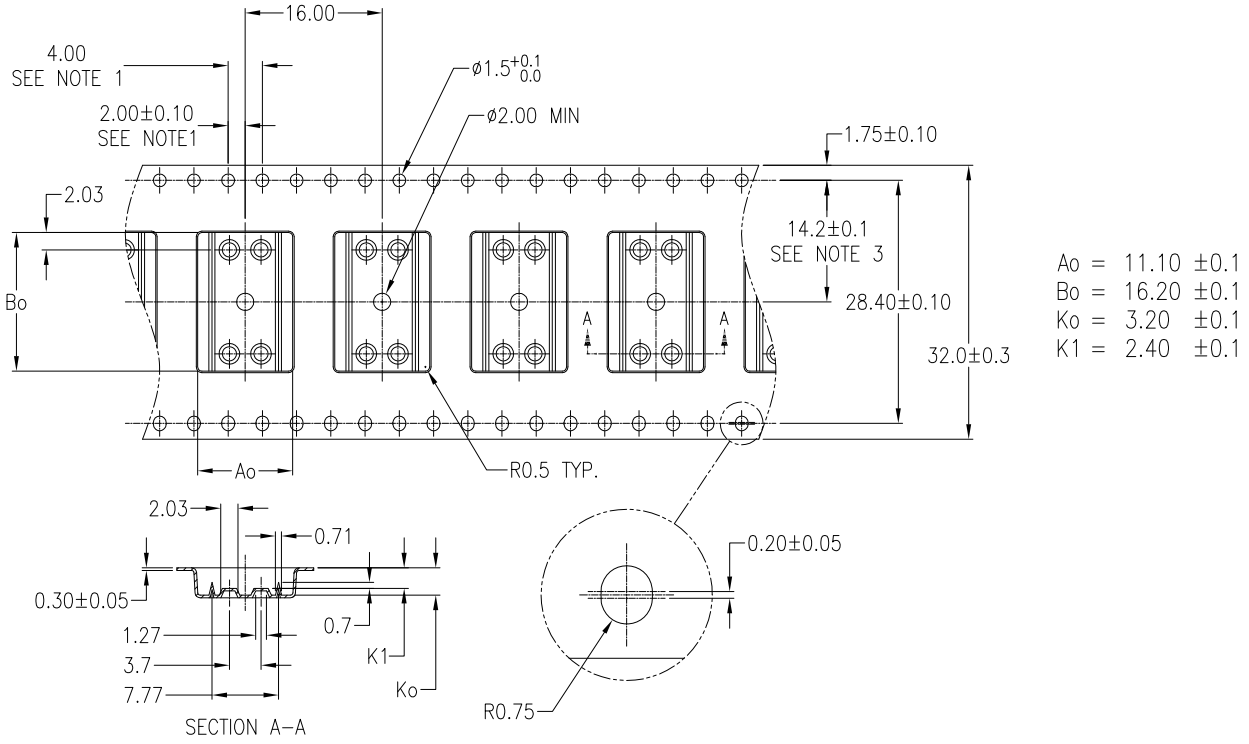
**Table 29. Solder Reflow Specifications**

| Package | Maximum Peak Temperature ($T_C$) | Maximum Time above $T_C$ – 5 °C |
|---|---|---|
| 28-pin SSOP | 260 °C | 30 seconds |
| 48-pin SSOP | 260 °C | 30 seconds |

**Note**
22. $T_J = T_A + POWER \times \theta_{JA}$

**Figure 13. 48-pin SSOP (300 Mils) Carrier Tape, 51-51104**

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE




51-51104 *E

**Table 30. Tape and Reel Specifications**

| Package | Cover Tape Width (mm) | Hub Size (inches) | Minimum Leading Empty Pockets | Minimum Trailing Empty Pockets | Standard Full Reel Quantity |
|---|---|---|---|---|---|
| 28-pin SSOP | 13.3 | 7 | 42 | 25 | 1000 |
| 48-pin SSOP | 25.5 | 4 | 32 | 19 | 1000 |

## Document Conventions

### Units of Measure

Table 32 lists the units of measure that are used in this document.

**Table 32. Units of Measure**

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| kB | 1024 bytes | ms | millisecond |
| °C | degree Celsius | mV | millivolt |
| kHz | kilohertz | nA | nanoampere |
| kΩ | kilohm | ns | nanosecond |
| LSbit | least-significant bit | W | ohm |
| MHz | megahertz | % | percent |
| µA | microampere | pF | picofarad |
| µs | microsecond | ps | picosecond |
| µV | microvolt | pA | picoampere |
| mA | milliampere | V | volt |
| mm | millimeter | W | watt |

### Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

## Glossary

| | |
|---|---|
| active high | 1. A logic signal having its asserted state as the logic 1 state.<br>2. A logic signal having the logic 1 state as the higher voltage of the two states. |
| analog blocks | The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more. |
| analog-to-digital (ADC) | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation. |
| API (Application Programming Interface) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications. |
| asynchronous | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal. |
| bandgap reference | A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference. |
| bandwidth | 1. The frequency range of a message or information processing system measured in hertz.<br>2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum. |
| bias | 1. A systematic deviation of a value from a reference value.<br>2. The amount by which the average of a set of values departs from a reference value.<br>3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device. |

## Glossary (continued)

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|---|---|
| external reset (XRES) | An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state. |
| flash | An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off. |
| Flash block | The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes. |
| frequency | The number of cycles or events per unit of time, for a periodic function. |
| gain | The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB. |
| $I^2C$ | A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode. |
| ICE | The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer). |
| input/output (I/O) | A device that introduces data into or extracts data from a system. |
| interrupt | A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed. |
| interrupt service routine (ISR) | A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution. |
| jitter | 1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams.<br>2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles. |
| low-voltage detect (LVD) | A circuit that senses $V_{DD}$ and provides an interrupt to the system when $V_{DD}$ falls below a selected threshold. |
| M8C | An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space. |
| master device | A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device***. |
| microcontroller | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal | The reference to a circuit containing both analog and digital techniques and components. |

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