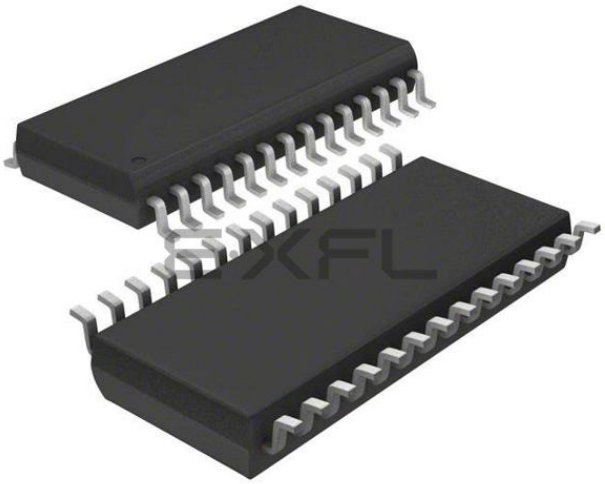

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21345-24pvxat

Pinouts

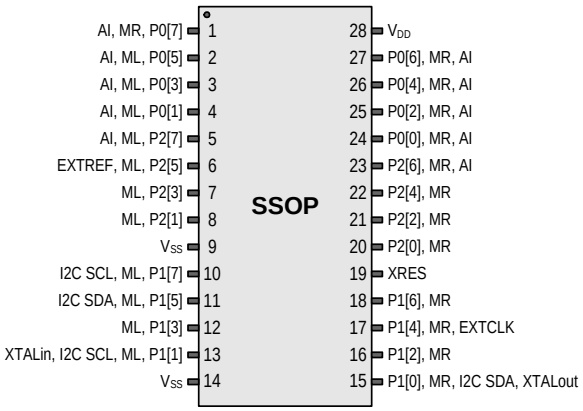
The automotive CY8C21x45 and CY8C22x45 PSoC devices are available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog mux bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

28-pin Part Pinout

Table 2. 28-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, MR	P0[7]	Analog column mux input, C_{MOD} capacitor pin
2	I/O	I, ML	P0[5]	Analog column mux input, C_{MOD} capacitor pin
3	I/O	I, ML	P0[3]	Analog column mux input
4	I/O	I, ML	P0[1]	Analog column mux input
5	I/O	I, ML	P2[7]	Direct input to analog block
6	I/O	ML	P2[5]	Optional SAR ADC external reference (EXTREF)
7	I/O	ML	P2[3]	
8	I/O	ML	P2[1]	
9	Power		V_{SS}	Ground connection
10	I/O	ML	P1[7]	I^2C serial clock (SCL)
11	I/O	ML	P1[5]	I^2C serial data (SDA)
12	I/O	ML	P1[3]	
13	I/O	ML	P1[1]	Crystal input (XTALin), I^2C SCL, ISSP-SCLK[5]
14	Power		V_{SS}	Ground connection
15	I/O	MR	P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA[5]
16	I/O	MR	P1[2]	
17	I/O	MR	P1[4]	Optional external clock input (EXTCLK)
18	I/O	MR	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	MR	P2[0]	
21	I/O	MR	P2[2]	
22	I/O	MR	P2[4]	
23	I/O	I, MR	P2[6]	Direct input to analog block
24	I/O	I, MR	P0[0]	Analog column mux input
25	I/O	I, MR	P0[2]	Analog column mux input
26	I/O	I, MR	P0[4]	Analog column mux input
27	I/O	I, MR	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

Figure 3. CY8C21345 and CY8C22345 28-pin PSoC Device



LEGEND: A = Analog, I = Input, O = Output, MR= Right analog mux bus input, ML= Left analog mux bus input.

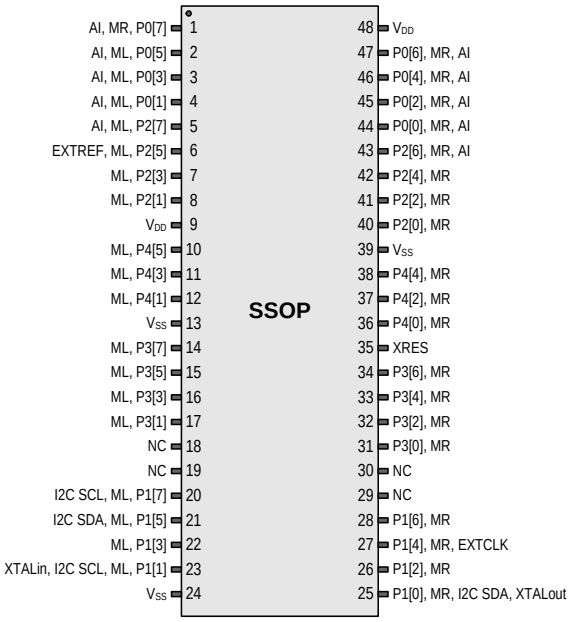
Note
5. These are the ISSP pins, which are not High Z after exiting a reset state. See the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for details.

48-pin Part Pinout

Table 3. 48-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, MR	P0[7]	Analog column mux input, C_{MOD} capacitor pin
2	I/O	I, ML	P0[5]	Analog column mux input, C_{MOD} capacitor pin
3	I/O	I, ML	P0[3]	Analog column mux input
4	I/O	I, ML	P0[1]	Analog column mux input
5	I/O	I, ML	P2[7]	Direct input to analog block
6	I/O	ML	P2[5]	Optional SAR ADC external reference
7	I/O	ML	P2[3]	
8	I/O	ML	P2[1]	
9	Power		V_{DD}	Supply voltage
10	I/O	ML	P4[5]	
11	I/O	ML	P4[3]	
12	I/O	ML	P4[1]	
13	Power		V_{SS}	Ground connection
14	I/O	ML	P3[7]	
15	I/O	ML	P3[5]	
16	I/O	ML	P3[3]	
17	I/O	ML	P3[1]	
18			NC	Not connected
19			NC	Not connected
20	I/O	ML	P1[7]	I^2C serial clock
21	I/O	ML	P1[5]	I^2C serial data
22	I/O	ML	P1[3]	
23	I/O	ML	P1[1]	Crystal input (XTALin), I^2C SCL, ISSP-SCLK[6]
24	Power		V_{SS}	
25	I/O	MR	P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA[6]
26	I/O	MR	P1[2]	
27	I/O	MR	P1[4]	Optional external clock input
28	I/O	MR	P1[6]	
29			NC	Not connected
30			NC	Not connected
31	I/O	MR	P3[0]	
32	I/O	MR	P3[2]	
33	I/O	MR	P3[4]	
34	I/O	MR	P3[6]	
35	Input		XRES	Active high external reset with internal pull-down
36	I/O	MR	P4[0]	
37	I/O	MR	P4[2]	
38	I/O	MR	P4[4]	
39	Power		V_{SS}	Ground connection
40	I/O	MR	P2[0]	
41	I/O	MR	P2[2]	
42	I/O	MR	P2[4]	

Figure 4. CY8C21645 and CY8C22645 48-pin PSoC Device



Note
6. These are the ISSP pins, which are not High Z after exiting a reset state. See the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for details.

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
PRT2DR	08	RW		48			88		PWMVREF0	C8	#
PRT2IE	09	RW		49			89		PWMVREF1	C9	#
PRT2GS	0A	RW		4A			8A		IDAC_MODE	CA	RW
PRT2DM2	0B	RW		4B			8B		PWM_SRC	CB	#
PRT3DR	0C	RW		4C			8C		TS_CR0	CC	RW
PRT3IE	0D	RW		4D			8D		TS_CMPH	CD	RW
PRT3GS	0E	RW		4E			8E		TS_CMPL	CE	RW
PRT3DM2	0F	RW		4F			8F		TS_CR1	CF	RW
PRT4DR	10	RW	CSD0_DR0_L	50	R		90		CUR PP	D0	RW
PRT4IE	11	RW	CSD0_DR1_L	51	W		91		STK_PP	D1	RW
PRT4GS	12	RW	CSD0_CNT_L	52	R		92			D2	
PRT4DM2	13	RW	CSD0_CR0	53	#		93		IDX_PP	D3	RW
	14		CSD0_DR0_H	54	R		94		MVR_PP	D4	RW
	15		CSD0_DR1_H	55	W		95		MVW_PP	D5	RW
	16		CSD0_CNT_H	56	R		96		I2C0_CFG	D6	RW
	17		CSD0_CR1	57	RW		97		I2C0_SCR	D7	#
	18		CSD1_DR0_L	58	R		98		I2C0_DR	D8	RW
	19		CSD1_DR1_L	59	W		99		I2C0_MSCR	D9	#
	1A		CSD1_CNT_L	5A	R		9A		INT_CLR0	DA	RW
	1B		CSD1_CR0	5B	#		9B		INT_CLR1	DB	RW
	1C		CSD1_DR0_H	5C	R		9C		INT_CLR2	DC	RW
	1D		CSD1_DR1_H	5D	W		9D		INT_CLR3	DD	RW
	1E		CSD1_CNT_H	5E	R		9E		INT_MSK3	DE	RW
	1F		CSD1_CR1	5F	RW		9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW		A1		INT_MSK1	E1	RW
DBC00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#		A4				
DBC01DR1	25	W	ASY_CR	65	#		A5				
DBC01DR2	26	RW	CMP_CR1	66	RW		A6		DEC _CR0	E6	RW
DBC01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCC02DR0	28	#	ADC0_CR	68	#		A8		MUL0_X	E8	W
DCC02DR1	29	W	ADC1_CR	69	#		A9		MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW		AA		MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW		AB		MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW		AC		ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW		AD		ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW		AE		ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW		AF		ACC0_DR2	EF	RW
DBC10DR0	30	#		70		RDI0RI	B0	RW		F0	
DBC10DR1	31	W		71		RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#		74		RDI0LT1	B4	RW		F4	
DBC11DR1	35	W		75		RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACE01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW	IDACR_D	FC	RW
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW	IDACL_D	FD	RW
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. **# Access is bit specific.**

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
PRT4DM0	10	RW	CMP0CR1	50	RW		90		GDI_O_IN	D0	RW
PRT4DM1	11	RW	CMP0CR2	51	RW		91		GDI_E_IN	D1	RW
PRT4IC0	12	RW		52			92		GDI_O_OU	D2	RW
PRT4IC1	13	RW	VDAC50CR0	53	RW		93		GDI_E_OU	D3	RW
	14		CMP1CR1	54	RW		94			D4	
	15		CMP1CR2	55	RW		95			D5	
	16			56			96			D6	
	17		VDAC51CR0	57	RW		97			D7	
	18		CSCMPCR0	58	#		98		MUX_CR0	D8	RW
	19		CSCMPGOEN	59	RW		99		MUX_CR1	D9	RW
	1A		CSLUTCR0	5A	RW		9A		MUX_CR2	DA	RW
	1B		CMPCOLMUX	5B	RW		9B		MUX_CR3	DB	RW
	1C		CMPPWMCR	5C	RW		9C		DAC_CR1#	DC	RW
	1D		CMPFLTCR	5D	RW		9D		OSC_GO_EN	DD	RW
	1E		CMPCLK1	5E	RW		9E		OSC_CR4	DE	RW
	1F		CMPCLK0	5F	RW		9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	R
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	V2BG_TR	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	W
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	W
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DBC02CR1	2B	RW	CLK_CR3	6B	RW	SADC_CR3TRIM	AB	RW	ECO_TR	EB	W
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_AD	AD	RW		ED	
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DBC03CR1	2F	RW	TMP_DR3	6F	RW		AF			EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW		71		RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DBC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW	DAC_CR0#	FD	RW
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DBC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. **# Access is bit specific.**

Electrical Specifications

This section presents the DC and AC electrical specifications for automotive CY8C21x45 and CY8C22x45 PSoC devices. For the latest electrical specifications, check the most recent data sheet by visiting the web at http://www.cypress.com.

Specifications are valid for A-grade devices at –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 100 °C, and for E-grade devices at –40 °C ≤ T_A ≤ 125 °C, T_J ≤ 135 °C, unless noted otherwise.

Figure 5. Voltage vs. CPU Frequency for A-grade Devices

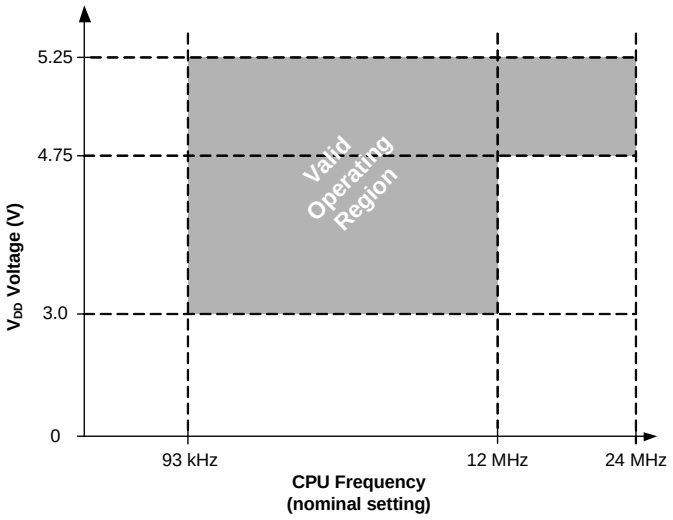


Figure 6. Voltage vs. CPU Frequency for E-grade Devices

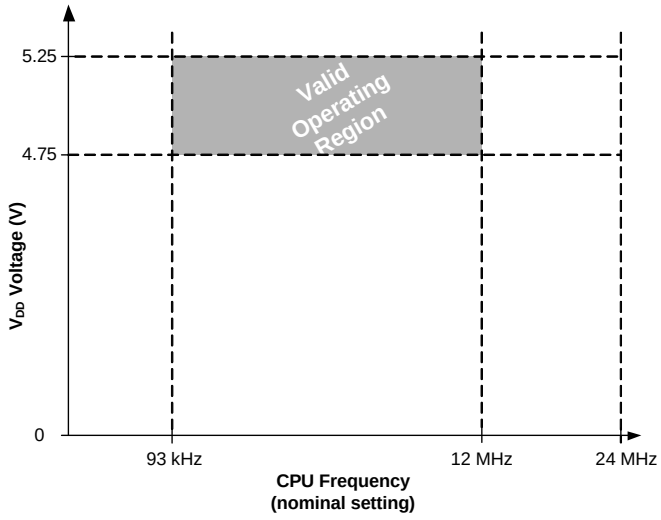
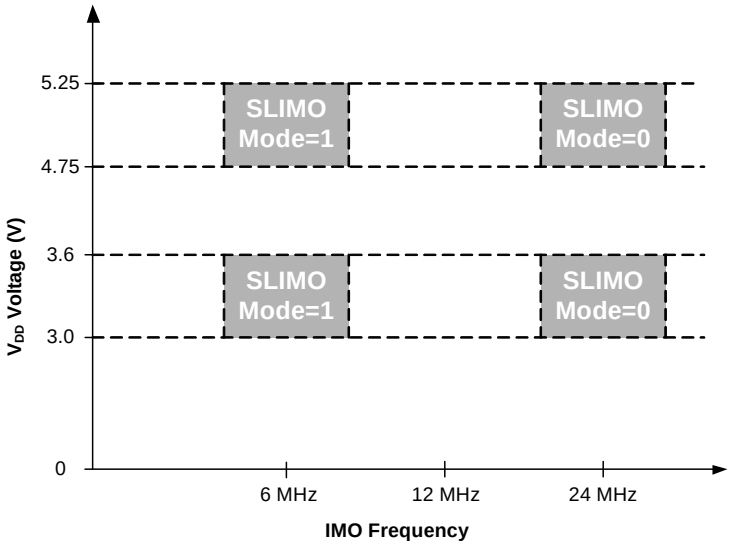


Figure 7. IMO Frequency Trim Options (A-grade Devices Only)



DC Electrical Characteristics

DC Chip Level Specifications

Table 9 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 9. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage A-grade devices E-grade devices	 3.0 4.75	 – –	 5.25 5.25	 V V	See Table 15 on page 19
I_{DD}	Supply current A-grade devices, 3.0 V ≤ V_{DD} ≤ 3.6 V A-grade devices, 4.75 V ≤ V_{DD} ≤ 5.25 V E-grade devices	 – – –	 4 7 8	 7 12 15	 mA mA mA	CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, Analog blocks disabled
I_{SB}	Sleep (mode) current A-grade devices, 3.0 V ≤ V_{DD} ≤ 3.6 V A-grade devices, 4.75 V ≤ V_{DD} ≤ 5.25 V E-grade devices	 – – –	 3 4 4	 12 25 25	 µA µA µA	Everything disabled except ILO, POR, LVD, Sleep Timer, and WDT circuits
I_{SBXTL}	Sleep (mode) current with ECO A-grade devices, 3.0 V ≤ V_{DD} ≤ 3.6 V A-grade devices, 4.75 V ≤ V_{DD} ≤ 5.25 V E-grade devices	 – – –	 4 5 5	 13 26 26	 µA µA µA	Everything disabled except ECO, POR, LVD, Sleep Timer, and WDT circuits
V_{REF}	Reference voltage (Bandgap)	1.275	1.30	1.325	V	Trimmed for appropriate V_{DD} setting.

DC Operational Amplifier Specifications

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25°C, unless specified otherwise, and are for design guidance only.

Table 11. DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
I_{SOA}	Supply current (absolute value) A-grade devices E-grade devices	 – –	 – –	 30 35	 µA µA	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}[7]	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. T_A = 25 °C
V_{CMOA}	Common mode voltage range	0.5	–	V_{DD} – 1	V	

DC IDAC Specifications

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 12. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$IDAC_{GAIN}$	IDAC gain	–	75.4	218	nA/bit	IDAC gain at 1x current gain
		–	335	693	nA/bit	IDAC gain at 4x current gain
		–	1160	2410	nA/bit	IDAC gain at 16x current gain
		–	2340	5700	nA/bit	IDAC gain at 32x current gain
	Monotonicity	No	–	–	–	IDAC gain is non-monotonous at step intervals of (0x10)
$IDAC_{GAIN\_VAR}$	IDAC gain variation over temperature –40 °C to 85 °C	–	3.22	–	nA	at 1x current gain
		–	18.1	–	nA	at 4x current gain
		–	59.9	–	nA	at 16x current gain
		–	120	–	nA	at 32x current gain
I_{IDAC}	IDAC current at maximum code (0xFF)	–	19.2	–	µA	at 1x current gain
		–	85.4	–	µA	at 4x current gain
		–	295	–	µA	at 16x current gain
		–	596	–	µA	at 32x current gain

Note
7. Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25 °C; 50 nA over temperature. Use Port 0 Pins 1 – 7 for the lowest leakage of 200 nA.

DC SAR10 ADC Specifications

Table 13 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 13. DC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ADCREF}	Reference voltage at pin P2[5] when configured as ADC reference voltage	3.0	–	5.25	V	When V_{REF} is buffered inside ADC, the voltage level at P2[5] (when configured as ADC reference voltage) must be always maintained to be at least 300 mV less than the chip supply voltage level on V_{DD} pin. ($V_{ADCREF} < V_{DD}$)
I_{ADCREF}	Current into P2[5] when configured as ADC V_{REF}	–	–	100	µA	Disables the internal voltage reference buffer
INL_{ADC}	Integral nonlinearity A-grade devices E-grade devices	 –3.0 –5.0	 – –	 3.0 5.0	 LSbit LSbit	10-bit resolution
DNL_{ADC}	Differential nonlinearity A-grade devices E-grade devices	 –1.5 –4.0	 – –	 1.5 4.0	 LSbit LSbit	10-bit resolution

DC Analog Mux Bus Specifications

Table 14 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 14. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400	Ω	
R_{GND}	Resistance of initialization switch to GND	–	–	800	Ω	

DC POR and LVD Specifications

Table 15 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 15. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 3.0 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.73	V	
	V_{DD} value for LVD trip					
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	

DC Programming Specifications

Table 16 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 16. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify A-grade devices E-grade devices	 3.0 4.7	 3.1 4.8	 3.2 4.9	 V V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation A-grade devices E-grade devices	 3.0 4.75	 – –	 5.25 5.25	 V V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor
V_{OLV}	Output low voltage during programming or verify	–	–	0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block) [8, 9] A-grade devices E-grade devices	 1,000 100	 – –	 – –	 – –	Erase/write cycles per block
$Flash_{ENT}$	Flash endurance (total) [9, 10] CY8C21x45 A-grade devices CY8C22x45 A-grade devices CY8C21x45 E-grade devices CY8C22x45 E-grade devices	 128,000 256,000 12,800 25,600	 – – – –	 – – – –	 – – – –	Erase/write cycles
$Flash_{DR}$	Flash data retention [9] A-grade devices E-grade devices	 10 10	 – –	 – –	 Years Years	

Notes

8. The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
10. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.

Table 17. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
t_{JIT_IMO} [13]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	400	ps	
t_{JIT_PLL} [13]	PLL cycle-to-cycle jitter (RMS)	–	200	800	ps	
	PLL long term N cycle-to-cycle jitter (RMS)	–	300	1200	ps	N = 32
	PLL period jitter (RMS)	–	100	700	ps	

Note
13. Refer to Cypress Jitter Specifications document, Understanding Datasheet Jitter Specifications for Cypress Timing Products for more information.

AC Programming Specifications

Table 23 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 23. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
F_{SCLK3}	Frequency of SCLK	0	–	6	MHz	$V_{DD} \leq 3.6$ V
t_{ERASEB}	Flash erase time (block)	–	10	40 [16]	ms	
t_{WRITE}	Flash block write time	–	40	160 [16]	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	55	ns	$V_{DD} > 3.6$ V, 30 pF load
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	65	ns	3.0 V $\leq V_{DD} \leq$ 3.6 V, 30 pF load
t_{PRGH}	Total flash block program time ($t_{ERASEB} + t_{WRITE}$), hot	–	–	100 [16]	ms	$T_J \geq 0$ °C
t_{PRGC}	Total flash block program time ($t_{ERASEB} + t_{WRITE}$), cold	–	–	200 [16]	ms	$T_J < 0$ °C

Note
16. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.

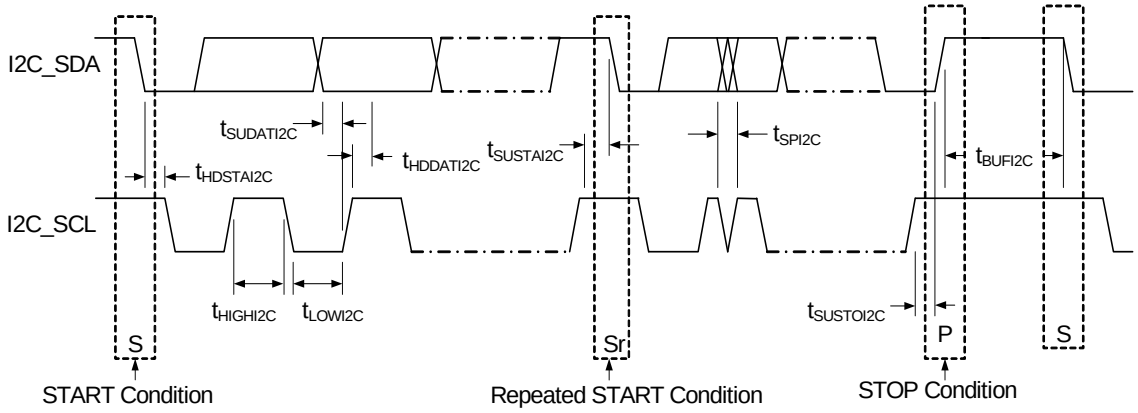
AC I²C Specifications

Table 24 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 24. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100 [17]	0	400 [17]	kHz
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$t_{SUDATI2C}$	Data setup time	250	–	100 [18]	–	ns
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUFI2C}	Bus-free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

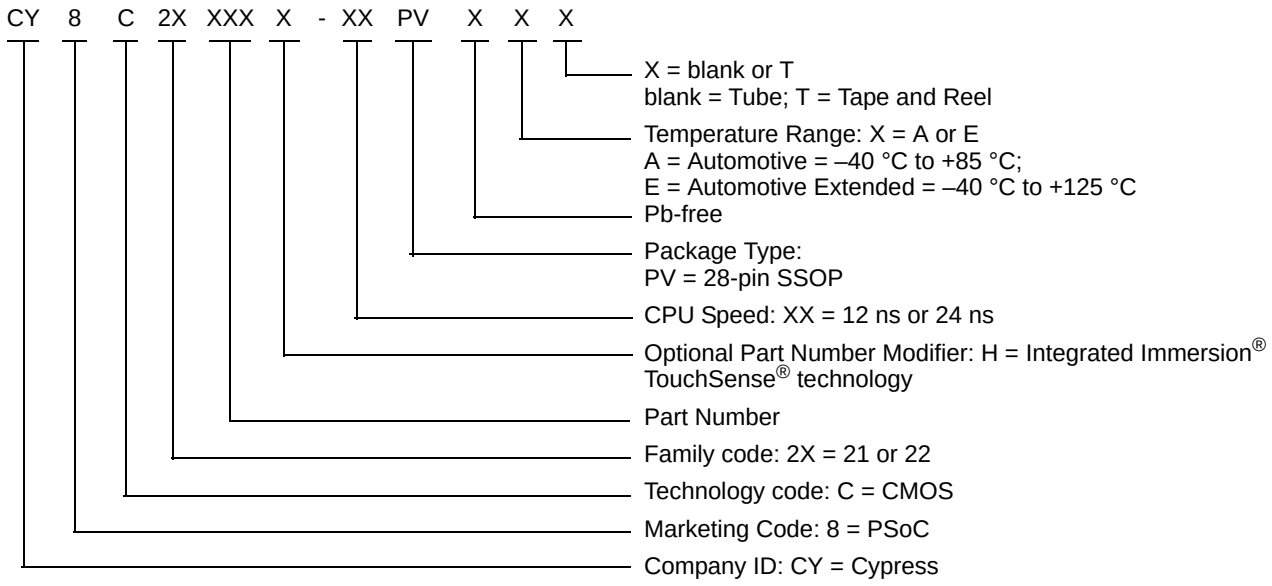
Figure 9. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

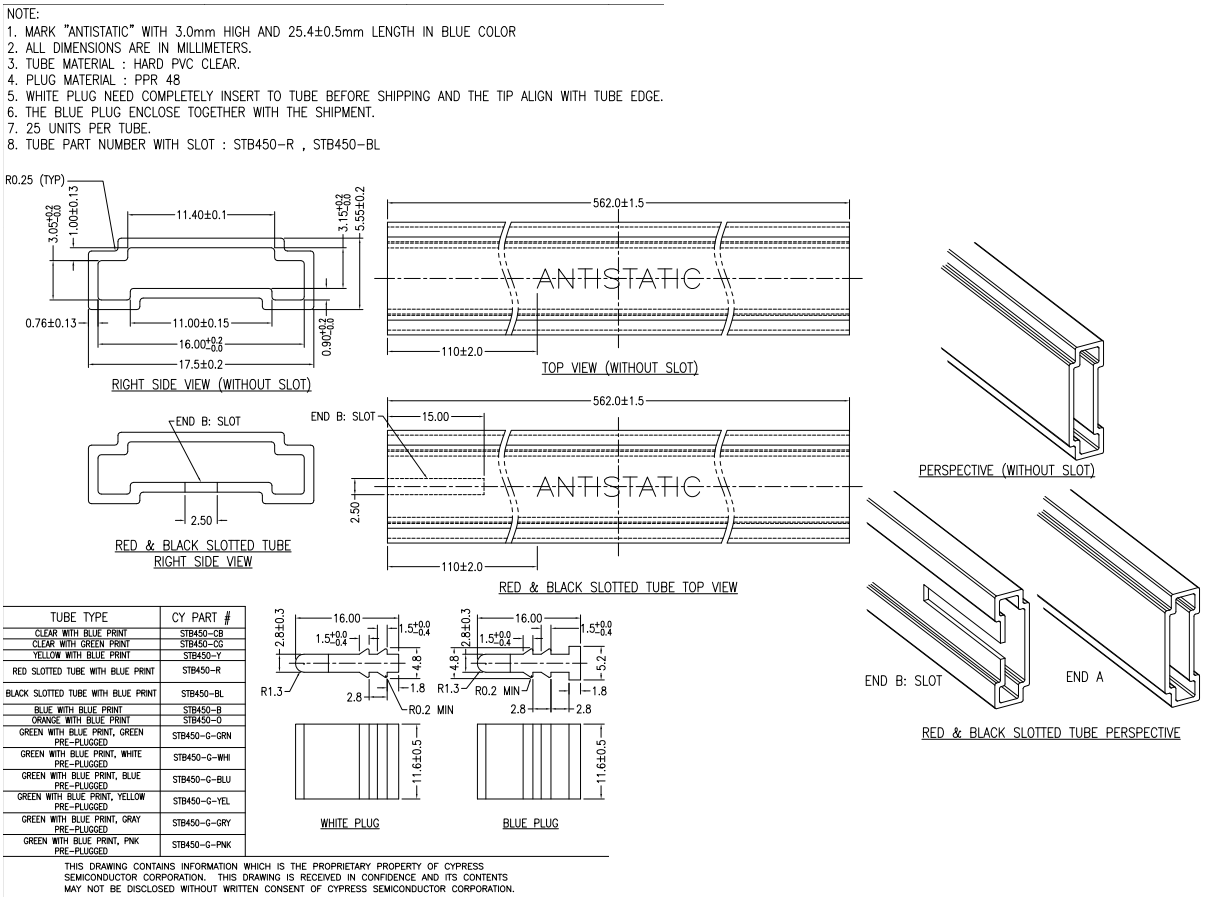
17. F_{SCLI2C} is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the F_{SCLI2C} specification adjusts accordingly.
18. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $t_{SUDATI2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C-bus specification) before the SCL line is released.

Ordering Code Definitions



Tube Information

Figure 14. 28-pin SSOP, 32-pin SOIC (450 Mils Body) Shipping Tube, 51-51029



TUBE TYPE	CY PART #
CLEAR WITH BLUE PRINT	STB450-CB
CLEAR WITH GREEN PRINT	STB450-CG
YELLOW WITH BLUE PRINT	STB450-Y
RED SLOTTED TUBE WITH BLUE PRINT	STB450-R
BLACK SLOTTED TUBE WITH BLUE PRINT	STB450-BL
BLUE WITH BLUE PRINT	STB450-B
ORANGE WITH BLUE PRINT	STB450-O
GREEN WITH BLUE PRINT, GREEN PRE-PLUGGED	STB450-G-GRN
GREEN WITH BLUE PRINT, WHITE PRE-PLUGGED	STB450-G-WHI
GREEN WITH BLUE PRINT, BLUE PRE-PLUGGED	STB450-G-BLU
GREEN WITH BLUE PRINT, YELLOW PRE-PLUGGED	STB450-G-YEL
GREEN WITH BLUE PRINT, GRAY PRE-PLUGGED	STB450-G-GRY
GREEN WITH BLUE PRINT, PNK PRE-PLUGGED	STB450-G-PNK

51-51029 *E

Acronyms

Table 31 lists the acronyms that are used in this document.

Table 31. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	LVD	low voltage detect
ADC	analog-to-digital converter	MAC	multiply-accumulate
AEC	Automotive Electronics Council	MCU	microcontroller unit
API	application programming interface	MIPS	million instructions per second
CMOS	complementary metal oxide semiconductor	PCB	printed circuit board
CPU	central processing unit	PDIP	plastic dual inline package
CRC	cyclic redundancy check	PGA	programmable gain amplifier
CSD	capsense sigma delta	POR	power-on reset
CT	continuous time	PPOR	precision POR
DAC	digital-to-analog converter	PRS	pseudo-random sequence
DC	direct current	PSoC®	Programmable System-on-Chip
DNL	differential nonlinearity	PWM	pulse-width modulator
ECO	external crystal oscillator	RMS	root mean square
EEPROM	electrically erasable programmable read-only memory	RTC	real time clock
GPIO	general-purpose I/O	SAR	successive approximation register
I^2C	inter-integrated circuit	SC	switched capacitor
I/O	input/output	SLIMO	slow IMO
ICE	in-circuit emulator	SPI	serial peripheral interface
IDE	integrated development environment	SRAM	static random-access memory
ILO	internal low speed oscillator	SROM	supervisory read-only memory
IMO	internal main oscillator	SSOP	shrunk small outline package
INL	integral nonlinearity	UART	universal asynchronous receiver transmitter
IrDA	infrared data association	USB	universal serial bus
ISSP	in-system serial programming	WDT	watchdog timer
LCD	liquid crystal display	XRES	external reset
LED	light-emitting diode		

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Data Sheet Jitter Specifications for Cypress Timing Products (001-71968)

Glossary (continued)

modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.

2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

■ **Problem Definition**

Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

■ **Parameters Affected**

The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.

■ **Trigger Condiiton(S)**

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.

■ **Scope of Impact**

This problem may affect UART, IrDA, and FSK implementations.

■ **Workaround**

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

■ **Fix Status**

The cause of this problem and its solution has been identified. No silicon fix is planned to correct the deficiency in silicon.

Document History Page

Document Title: CY8C21345/CY8C21645/CY8C22345/CY8C22345H/CY8C22645, Automotive PSoC® Programmable System-on-Chip™ Document Number: 001-55397				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2759868	VIVG	09/04/09	New data sheet.
*A	2788690	VIVG	10/20/09	Added 48 SSOP to the marketing part numbers. Corrected the I_{SOA} spec in table 13/14. Changed the ThetaJA values based on PE inputs.
*B	2792800	VIVG	10/26/09	Corrected typo in ordering information table (Digital I/O for 48-SSOP devices)
*C	2822630	BTK	12/07/09	Added CY8C22345H devices and updated Features section and PSoC Functional Overview section to include haptics device information. Updated Features section. Added Contents section. Updated PSoC Functional Overview section. Updated Block Diagram of device. Updated PSoC Device Characteristics table. Updated Pinouts section. Fixed issues with the Register Map tables. Added a figure for SLIMO configuration. Updated footnotes for the DC Programming Specifications table. Corrected $V_{DDIWRITE}$ and $Flash_{ENT}$ electrical specifications. Updated Ordering Information section. Added Development Tool Selection section. Combined 5 V DC Operational Amplifier Specifications table with 3.3 V DC Operational Amplifier Specifications table. Updated all AC specifications to conform to 5% IMO accuracy and 8.33% SLIMO accuracy. Split up electrical specifications for A-grade and E-grade devices in the Absolute Maximum Ratings, Operating Temperature, DC Chip Level Specifications, DC Programming Specifications, and AC Chip-Level Specifications tables. Added Solder Reflow Peak Temperature table. Added T_{PRGH}, T_{PRGC}, I_{OL}, I_{OH}, F_{32KU}, DC_{ILO}, and $T_{POWERUP}$ electrical specifications. Added maximum values and updated typical values for T_{ERASEB} and T_{WRITE} electrical specifications. Replaced T_{RAMP} electrical specification with $SR_{POWERUP}$ electrical specification.
*D	2905459	NJF	04/06/10	Updated Cypress website links Added $T_{BAKETEMP}$, $T_{BAKETIME}$, and Fout48M electrical specifications Removed sections ‘Third Party Tools’ ‘Build a PSoC Emulator into your Board’ Updated package diagrams Updated Ordering Information table Updated Solder Reflow Peak Temperature specifications. Updated the Getting Started and Designing with PSoC Designer sections. Converted data sheet from Preliminary to Final Deleted 5% oscillator accuracy reference in the Features section. Deleted reference to a specific SAR10 ADC sample rate in the Analog System section. Updated the following Electrical Specifications: I_{DD}, I_{SB}, I_{SBXTL}, V_{REF}, V_{CMOA}, I_{ADCREF}, INL_{ADC}, DNL_{ADC}, V_{PPOR2}, $Flash_{DR}$, F_{IMO24}, T_{RiseF}, T_{FallF}, T_{RiseS}, T_{FallS}. Deleted the SPS_{ADC} electrical specification, the DC Low Power Comparator Specifications, the AC Low Power Comparator Specifications, and the AC Analog Mux Bus Specifications.
*E	2915673	VIVG	04/16/10	Post to external web
*F	2991841	BTK	07/23/10	Added a clarifying note to the V_{PPOR1} electrical specification. Added CY8C22345-12PVXE(T) devices. Moved Document Conventions to the end of the document.
*G	3037161	BTK	09/23/10	Added CY8C21345-12PVXE(T) devices to the Ordering Information section.
*H	3085024	BTK	11/12/10	Added CY8C21645-12PVXE(T), CY8C21645-24PVXA(T), CY8C22645-12PVXE(T), and CY8C22645-24PVXA(T) devices to the Ordering Information section.
*I	3200275	BTK	03/18/11	Added tape and reel packaging information.

Document History Page (continued)

Document Title: CY8C21345/CY8C21645/CY8C22345/CY8C22345H/CY8C22645, Automotive PSoC® Programmable System-on-Chip™ Document Number: 001-55397				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	3341627	BTK/NJF	08/11/2011	Updated I^2C timing diagram to improve clarity. Updated wording, formatting, and notes of the AC Digital Block Specifications table to improve clarity. Added V_{DDP}, V_{DDLV}, and V_{DDHV} electrical specifications to give more information for programming the device. Updated solder reflow temperature specifications to give more clarity. Updated the jitter specifications. Updated PSoC Device Characteristics table. Updated the F_{32KU} electrical specification. Updated note for R_{PD} electrical specification. Updated note for the T_{STG} electrical specification to add more clarity. Removed CY8C22345H-24PVXA(T) devices from datasheet.
*K	3732256	MASJ	10/04/2012	Updated Features (Included CY8C22345H device related information). Updated PSoC Functional Overview (Updated Digital System (Changed PWM description string from “8- to 32-bit” to “8- and 16-bit”), added Haptics TS2000 Controller). Updated Development Tool Selection (Updated Accessories (Emulation and Programming) (Updated Table 25)). Updated Electrical Specifications (Updated DC Electrical Characteristics (Updated DC GPIO Specifications (Updated Table 10 (To include the V_{OL} specification for V_{DD} = 3.0 to 3.6 V condition)))). Updated Ordering Information (Updated part numbers). Updated Packaging Information (Updated Package Dimensions (spec 51-85061 (Changed revision from *D to *F), spec 51-51100 (Changed revision from *B to *C)), updated Tape and Reel Information (spec 51-51100 (Changed revision from *B to *C)), added Tube Information (spec 51-51029, spec 51-51000)).
*L	4479445	ASRI	08/20/2014	Updated Electrical Specifications: Updated DC Electrical Characteristics: Added DC IDAC Specifications. Updated Packaging Information: Updated Tape and Reel Information: spec 51-51100 – Changed revision from *C to *D. spec 51-51104 – Changed revision from *D to *E. Updated in new template. Completing Sunset Review.
*M	4513128	ASRI	09/25/2014	Updated Packaging Information: Updated Tube Information: spec 51-51000 – Changed revision from *K to *L. Added Errata.