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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/cy8c21645-12pvxe

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PSoC Functional Overview

The PSoC programmable system-on-chip series of products consists of many devices. These devices are designed to replace multiple traditional MCU-based system components with one low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, shown in the Block Diagram on page 1, consists of four main areas: PSoC core, digital system, analog system, and system resources. Configurable global busing allows the combining of all the device resources into a complete custom system. The PSoC family can have up to five I/O ports connecting to the global digital and analog interconnects, providing access to eight digital blocks [1] and six analog blocks.

PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO.

The M8C CPU core is a powerful processor with speeds up to 24 MHz (up to 12 MHz for E-grade devices), providing four MIPS (two MIPS for E-grade devices) 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller to simplify the programming of real time embedded events.

Program execution is timed and protected using the included Sleep Timer and watchdog timer (WDT).

Memory encompasses 16 KB of flash (8 KB for CY8C21x45 devices) for program storage, 1 KB of SRAM (512 bytes for CY8C21x45 devices) for data storage, and EEPROM emulation using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

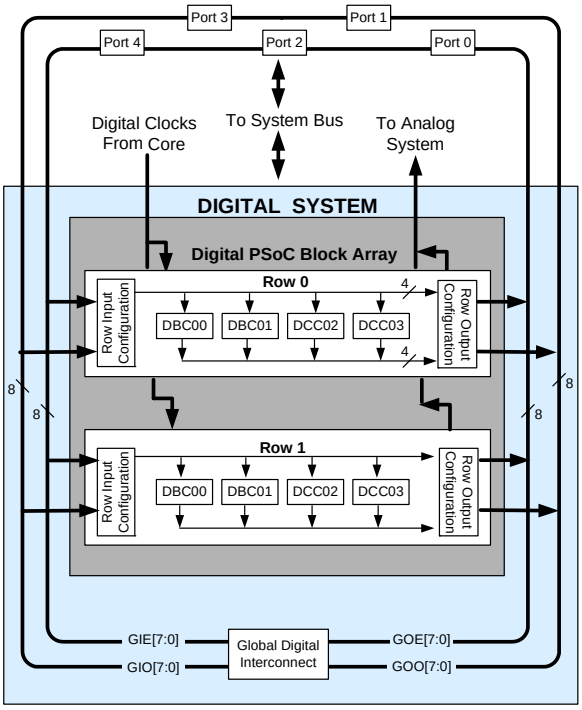
The PSoC device incorporates flexible internal clock generators, including a 24-MHz internal main oscillator (IMO). For A-grade devices the 24-MHz IMO can also be doubled to 48 MHz for use by the digital system. A low-power 32-kHz internal low-speed oscillator (ILO) is provided for the Sleep Timer and WDT. If crystal accuracy is required, the 32.768 kHz external crystal oscillator (ECO) is available for use as a RTC, and can optionally generate a crystal-accurate 24-MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Each pin can also generate a system interrupt.

Digital System

The digital system is composed of eight digital PSoC blocks. Each block is an 8-bit resource that may be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules.

Figure 1. Digital System Block Diagram [1]



Digital peripheral configurations are:

- PWMs (8- to 16-bit)
- PWMs with deadband (8- to 32-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- One-shot and multi-shot modules
- Full or half-duplex 8-bit UART with selectable parity (up to two full-duplex or four half-duplex)
- SPI master and slave (up to four total) with programmable data length from 8 to 16 bits.
- Shift register (1- to 32-bit)
- I^2C master, slave, or multi-master (one available)
- CRC/generator (16-bit)
- IrDA (up to two)
- PRS generators (8- to 32-bit)

Note
1. CY8C22x45 devices have 2 digital rows with 8 digital blocks. CY8C21x45 devices only have 1 digital row with 4 digital blocks.

The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides a choice of system resources for your application. Family resources are shown in Table 1 on page 5.

Analog System

The Analog System of CY8C21x45 and CY8C22x45 PSoC devices consists of a 10-bit SAR ADC and six configurable analog blocks.

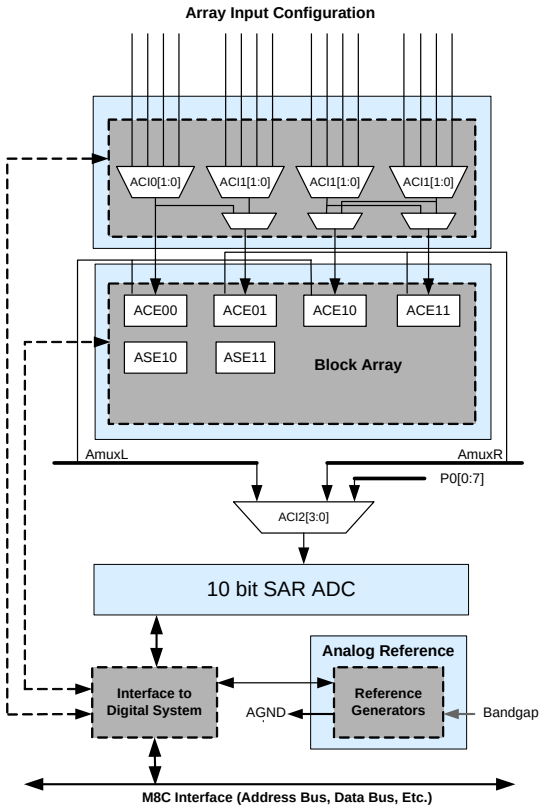
The programmable 10-bit SAR ADC is an optimized ADC with a fast maximum sample rate. External filters are required on ADC input channels for antialiasing. This ensures that any out-of-band content is not folded into the input signal band.

Reconfigurable analog resources allow creating complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (single or dual, with up to 10-bit resolution)
- Pin-to-pin comparator
- Single-ended comparators (up to four) with absolute (1.3 V) reference or DAC reference
- Precision voltage reference (1.3 V nominal)

CY8C21x45 and CY8C22x45 devices have six limited-functionality Type 'E' analog blocks. These analog blocks are arranged in four columns. Each column contains one continuous time (CT) Type E block. The first two columns also have a switched capacitor (SC) type E block. Refer to the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for detailed information on the Type E analog blocks.

Figure 2. Analog System Block Diagram



Haptics TS2000 Controller

The CY8C22x45H family of devices features an easy-to-use Haptics controller resource with up to 14 different effects. These effects are available for use with three different, selectable ERM modules.

Getting Started

For in depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

Table 3. 48-pin Part Pinout (SSOP) (continued)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
43	I/O	I, MR	P2[6]	Direct input to analog block
44	I/O	I, MR	P0[0]	Analog column mux input
45	I/O	I, MR	P0[2]	Analog column mux input
46	I/O	I, MR	P0[4]	Analog column mux input
47	I/O	I, MR	P0[6]	Analog column mux input
48	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, O = Output, MR= Right analog mux bus input, ML= Left analog mux bus input

Registers

This section lists the registers of this PSoC device family by mapping tables. For detailed register information, refer to the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 4. Abbreviations

Convention	Description
RW	Read and write register or bit(s)
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Electrical Specifications

This section presents the DC and AC electrical specifications for automotive CY8C21x45 and CY8C22x45 PSoC devices. For the latest electrical specifications, check the most recent data sheet by visiting the web at http://www.cypress.com.

Specifications are valid for A-grade devices at –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 100 °C, and for E-grade devices at –40 °C ≤ T_A ≤ 125 °C, T_J ≤ 135 °C, unless noted otherwise.

Figure 5. Voltage vs. CPU Frequency for A-grade Devices

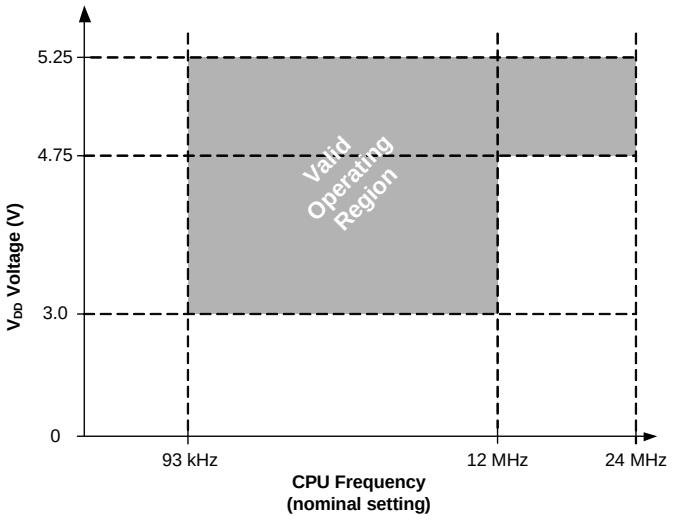


Figure 6. Voltage vs. CPU Frequency for E-grade Devices

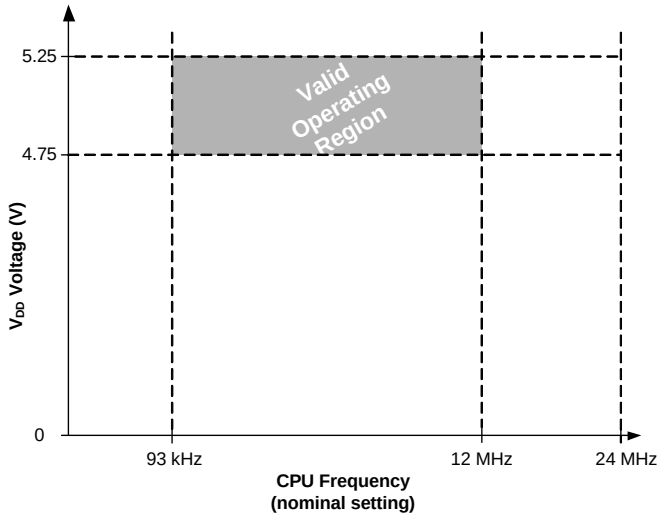
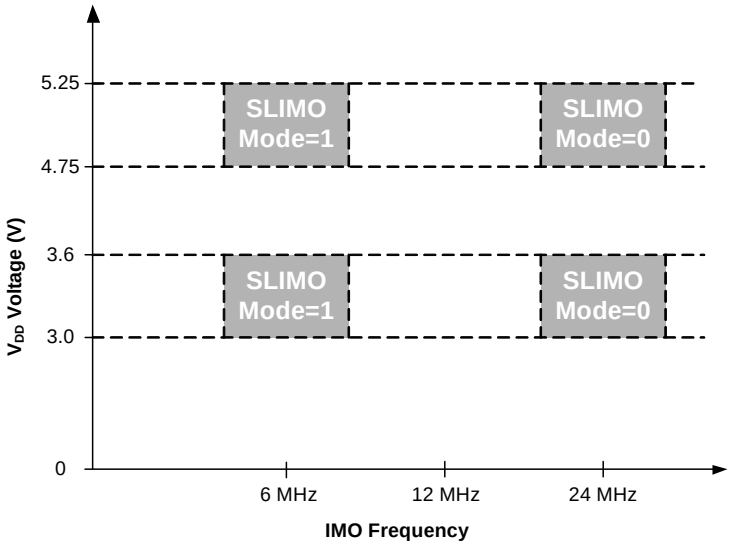


Figure 7. IMO Frequency Trim Options (A-grade Devices Only)



DC POR and LVD Specifications

Table 15 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 15. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 3.0 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.73	V	
	V_{DD} value for LVD trip					
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	

AC Electrical Characteristics

AC Chip Level Specifications

The following tables list the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 17. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal main oscillator frequency for 24 MHz A-grade devices, 4.75 V ≤ V_{DD} ≤ 5.25 V A-grade devices, 3.0 V ≤ V_{DD} ≤ 3.6 V E-grade devices	 22.8 22.5 22.3	 24 24 24	 25.2 [11] 25.5 [11] 25.7 [11]	 MHz MHz MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 7 on page 14.
F_{IMO6}	Internal main oscillator frequency for 6 MHz A-grade devices E-grade devices	 5.5 5.5	 6 6	 6.5 [11] 6.5 [11]	 MHz MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 7 on page 14.
F_{CPU1}	CPU frequency (5 V V_{DD} operation) A-grade devices E-grade devices	 0.089 0.089	 – –	 25.2 [11] 12.6 [11]	 MHz MHz	SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V V_{DD} operation)	0.089	–	12.6 [11]	MHz	A-grade devices only. SLIMO mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V V_{DD} operation) A-grade devices E-grade devices	 0 0	 48 24	 50.4 [11, 12] 25.2 [11, 12]	 MHz MHz	Refer to Table 20 on page 24.
F_{BLK33}	Digital PSoC block frequency (3.3 V V_{DD} operation)	0	24	24.6 [11]	MHz	A-grade devices only
F_{32K1}	ILO frequency	15	32	75	kHz	This specification applies when the ILO has been trimmed.
F_{32KU}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C processor starts to execute, the ILO is not trimmed.
t_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
Fout48M	48 MHz output frequency	45.6	48.0	50.4 [11]	MHz	
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	12.6	MHz	
$SR_{POWERUP}$	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time between end of POR state and CPU code execution	–	16	100	ms	Power-up from 0 V.

Notes
11. Accuracy derived from IMO with appropriate trim for V_{DD} range
12. Refer to the individual user module data sheets for information on maximum frequencies for user modules.

Table 17. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
t_{JIT_IMO} [13]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	400	ps	
t_{JIT_PLL} [13]	PLL cycle-to-cycle jitter (RMS)	–	200	800	ps	
	PLL long term N cycle-to-cycle jitter (RMS)	–	300	1200	ps	N = 32
	PLL period jitter (RMS)	–	100	700	ps	

Note
13. Refer to Cypress Jitter Specifications document, Understanding Datasheet Jitter Specifications for Cypress Timing Products for more information.

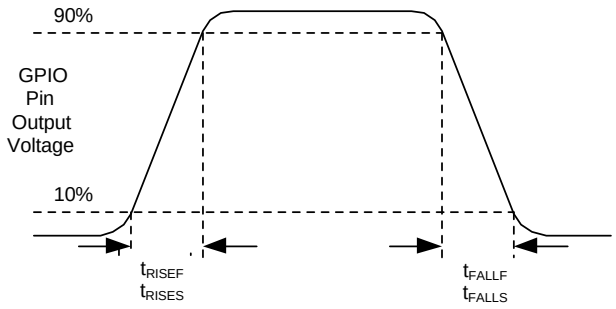
AC GPIO Specifications

Table 18 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 18. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.6	MHz	Normal strong mode
t_{RISEF}	Rise time, normal strong mode, Cload = 50 pF A-grade devices E-grade devices	 3 3	 – –	 18 24	 ns ns	Refer to Figure 8
t_{FALLF}	Fall time, normal strong mode, Cload = 50 pF A-grade devices E-grade devices	 2 2	 – –	 18 28	 ns ns	Refer to Figure 8
t_{RISES}	Rise time, slow strong mode, Cload = 50 pF A-grade devices E-grade devices	 7 7	 27 32	 – –	 ns ns	Refer to Figure 8
t_{FALLS}	Fall time, slow strong mode, Cload = 50 pF A-grade devices E-grade devices	 7 7	 22 28	 – –	 ns ns	Refer to Figure 8

Figure 8. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 19 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 19. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator mode response time, 50 mV	–	–	100	ns	

Table 20. AC Digital Block Specifications (continued)

Function	Description	Min	Typ	Max	Units	Notes
Transmitter	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 Stop Bits	–	–	50.4 [15]	MHz	
	$V_{DD} \geq 4.75$ V, 1 Stop Bit	–	–	25.2 [15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	
Receiver	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 Stop Bits	–	–	50.4 [15]	MHz	
	$V_{DD} \geq 4.75$ V, 1 Stop Bit	–	–	25.2 [15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	

Note
15. Accuracy derived from IMO with appropriate trim for V_{DD} range.

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows the user to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240-V power supply, Euro-Plug adapter
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 25. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit [19]	Foot Kit [20]	Prototyping Module	Adapter [21]
CY8C21345-24PVXA CY8C21345-12PVXE CY8C22345-24PVXA CY8C22345H-24PVXA CY8C22345-12PVXE	28-pin SSOP	CY3250-22345	CY3250-28SSOP-FK	–	AS-28-28-02SS-6ENP-GANG
CY8C21645-24PVXA CY8C21645-12PVXE CY8C22645-24PVXA CY8C22645-12PVXE	48-pin SSOP	–	–	–	AS-48-48-01SS-6-GANG

Notes
19. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
20. Foot kit includes surface mount feet that can be soldered to the target PCB.
21. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

The following table lists the key package features and ordering codes of the automotive CY8C21x45 and CY8C22x45 device families.

Table 26. PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-pin (210-Mil) SSOP	CY8C21345-24PVXA	8 K	512	–40 °C to +85 °C	4	6	24	24	0	Yes
28-pin (210-Mil) SSOP (Tape and Reel)	CY8C21345-24PVXAT	8 K	512	–40 °C to +85 °C	4	6	24	24	0	Yes
28-pin (210-Mil) SSOP	CY8C21345-12PVXE	8 K	512	–40 °C to +125 °C	4	6	24	24	0	Yes
28-pin (210-Mil) SSOP (Tape and Reel)	CY8C21345-12PVXET	8 K	512	–40 °C to +125 °C	4	6	24	24	0	Yes
28-pin (210-Mil) SSOP	CY8C22345-24PVXA	16 K	1 K	–40 °C to +85 °C	8	6	24	24	0	Yes
28-pin (210-Mil) SSOP (Tape and Reel)	CY8C22345-24PVXAT	16 K	1 K	–40 °C to +85 °C	8	6	24	24	0	Yes
28-pin (210-Mil) SSOP	CY8C22345H-24PVXA	16 K	1 K	–40 °C to +85 °C	8	6	24	24	0	Yes
28-pin (210-Mil) SSOP (Tape and Reel)	CY8C22345H-24PVXAT	16 K	1 K	–40 °C to +85 °C	8	6	24	24	0	Yes
28-pin (210-Mil) SSOP	CY8C22345-12PVXE	16 K	1 K	–40 °C to +125 °C	8	6	24	24	0	Yes
28-pin (210-Mil) SSOP (Tape and Reel)	CY8C22345-12PVXET	16 K	1 K	–40 °C to +125 °C	8	6	24	24	0	Yes
48-pin (300-Mil) SSOP	CY8C21645-24PVXA	8 K	512	–40 °C to +85 °C	4	6	38	38	0	Yes
48-pin (300-Mil) SSOP (Tape and Reel)	CY8C21645-24PVXAT	8 K	512	–40 °C to +85 °C	4	6	38	38	0	Yes
48-pin (300-Mil) SSOP	CY8C21645-12PVXE	8 K	512	–40 °C to +125 °C	4	6	38	38	0	Yes
48-pin (300-Mil) SSOP (Tape and Reel)	CY8C21645-12PVXET	8 K	512	–40 °C to +125 °C	4	6	38	38	0	Yes
48-pin (300-Mil) SSOP	CY8C22645-24PVXA	16 K	1 K	–40 °C to +85 °C	8	6	38	38	0	Yes
48-pin (300-Mil) SSOP (Tape and Reel)	CY8C22645-24PVXAT	16 K	1 K	–40 °C to +85 °C	8	6	38	38	0	Yes
48-pin (300-Mil) SSOP	CY8C22645-12PVXE	16 K	1 K	–40 °C to +125 °C	8	6	38	38	0	Yes
48-pin (300-Mil) SSOP (Tape and Reel)	CY8C22645-12PVXET	16 K	1 K	–40 °C to +125 °C	8	6	38	38	0	Yes

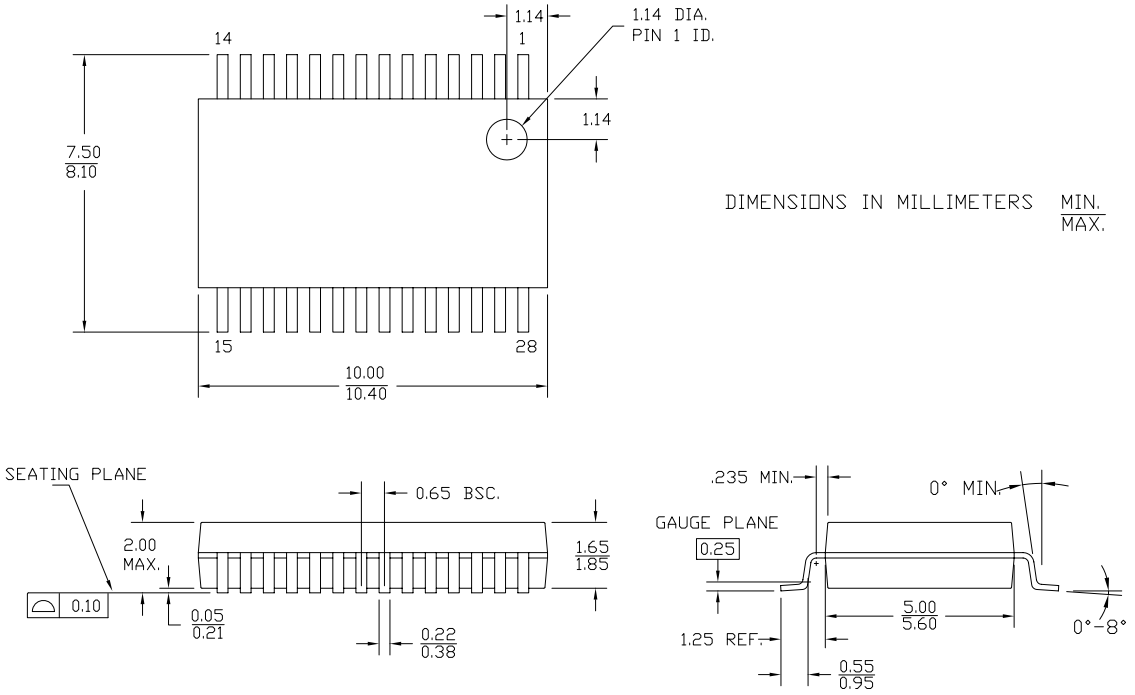
Packaging Information

This section provides the packaging specifications for the automotive CY8C21x45 and CY8C22x45 PSoC devices. The thermal impedances for each package and the typical package capacitance on crystal pins are given.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Package Dimensions

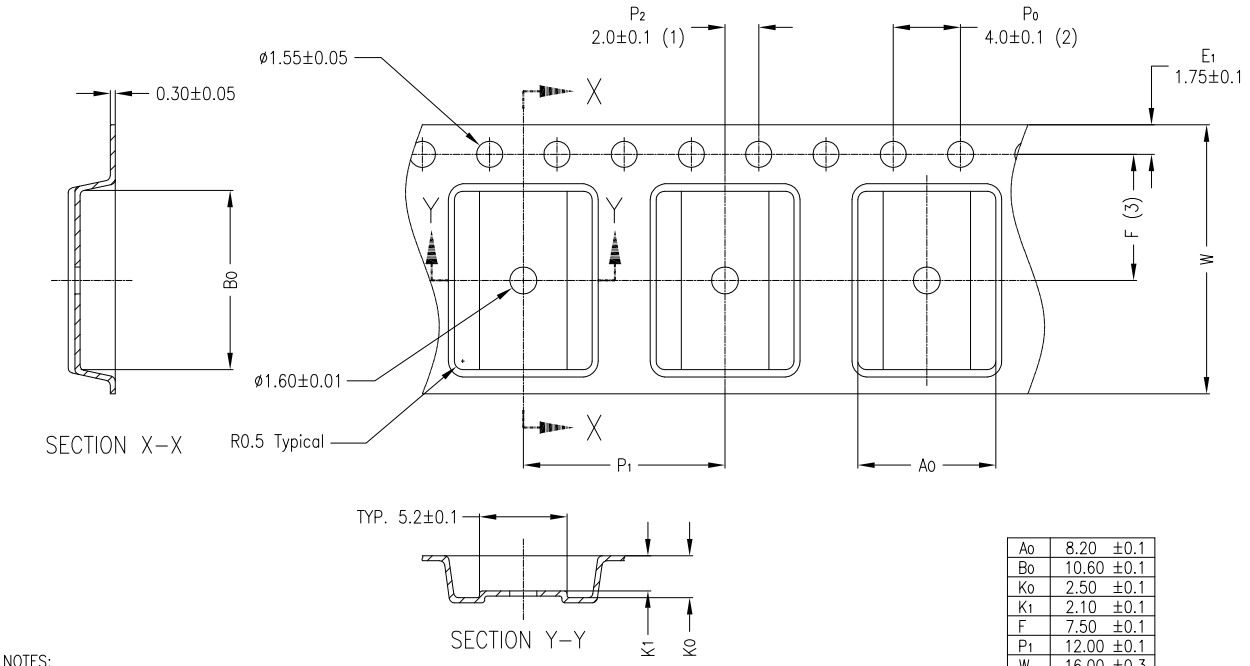
Figure 10. 28-pin SSOP (210 Mils) Package Outline, 51-85079



51-85079 *E

Tape and Reel Information

Figure 12. 28-pin SSOP (209 Mils) Carrier Tape, 51-51100



A0	8.20 ±0.1
B0	10.60 ±0.1
K0	2.50 ±0.1
K1	2.10 ±0.1
F	7.50 ±0.1
P1	12.00 ±0.1
W	16.00 ±0.3

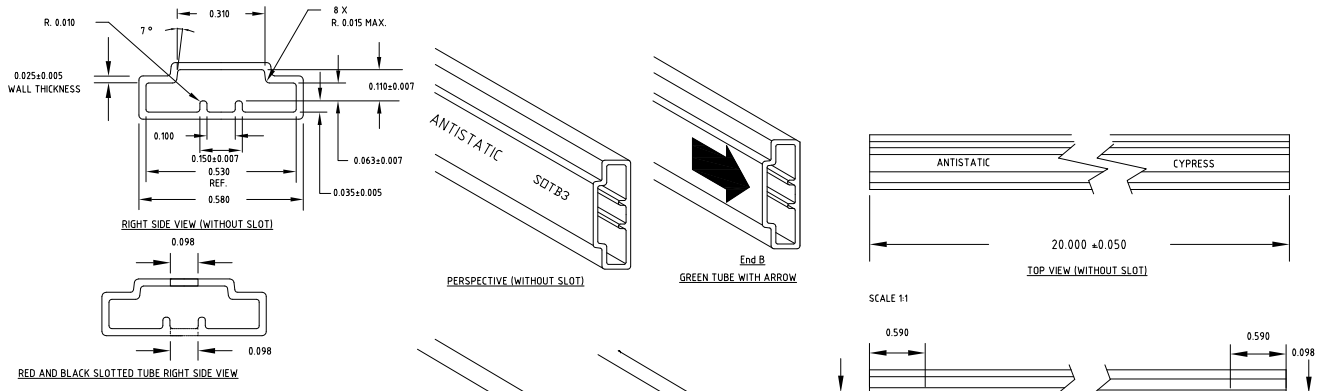
NOTES:
(1) Measured from centerline of sprocket hole to centerline of pocket.
(2) Cumulative tolerance of 10 sprocket holes is ± 0.10.
(3) Measured from centerline of sprocket hole to centerline of pocket
4 Material: Conductive Polystyrene
5 Camber not to exceed 1mm in 100mm
6 Supplier P/N: SSOP28–3 CL3 22B3 Lxx W16

51-51100 *D

Figure 15. 48-pin SSOP (300 Mils) Tube, 51-51000

NOTES:

1. ALL PARTS TO MEET THE REQUIREMENTS OF CYPRESS SPECIFICATION #03-00029
2. MATERIAL: REFER TO SPEC. #03-00029
3. FINISH: REFER TO SPEC. #03-00029
4. MAX. BURR ON INNER SIDE OF TUBE SHALL BE 0.010 IN.
5. CYPRESS LOGO AND "CYPRESS SEMICONDUCTOR" PRINT ON TUBE IS OPTIONAL
6. TUBE PART NUMBER WITH SLOT: SOTB3-R, SOTB3-BL
7. TUBE PART NUMBER WITH ARROW MARK: SOTB3-G



SOTB3-B	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS, BLUE WITH BLUE PRINT
SOTB3-BL	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS,SLOTTED BLACK TUBE WITH BLUE PRINT
SOTB3-CB	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS, CLEAR WITH BLUE PRINT
SOTB3-CG	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS, CLEAR WITH GREEN PRINT
SOTB3-G-GRN	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS, GREEN WITH BLUE PRINT, GREEN PREPLUGGED
SOTB3-G-WHI	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS, GREEN WITH BLUE PRINT, WHITE PREPLUGGED
SOTB3-G-BLU	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS, GREEN WITH BLUE PRINT, BLUE PREPLUGGED
SOTB3-G-YEL	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS, GREEN WITH BLUE PRINT, YELLOW PREPLUGGED
SOTB3-G-GRY	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS, GREEN WITH BLUE PRINT, GRAY PREPLUGGED
SOTB3-G-PNK	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS, GREEN WITH BLUE PRINT, PINK PREPLUGGED
SOTB3-O	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS, ORANGE WITH BLUE PRINT
SOTB3-R	SOJ20/24/28/32,SSOP48/56,SOIC16/20/24/28, 300 MILS, SLOTTED RED TUBE WITH BLUE PRINT

51-51000 *L

Document Conventions

Units of Measure

Table 32 lists the units of measure that are used in this document.

Table 32. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	ms	millisecond
°C	degree Celsius	mV	millivolt
kHz	kilohertz	nA	nanoampere
kΩ	kilohm	ns	nanosecond
LSbit	least-significant bit	W	ohm
MHz	megahertz	%	percent
µA	microampere	pF	picofarad
µs	microsecond	ps	picosecond
µV	microvolt	pA	picoampere
mA	milliampere	V	volt
mm	millimeter	W	watt

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

Glossary (continued)

external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device***.
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.

Glossary (continued)

modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.

Errata

This section describes the errata for the CY8C21x45, CY8C22x45 family of PSoC devices. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CY8C21345	All Variants
CY8C21645	All Variants
CY8C22345	All Variants
CY8C22645	All Variants

CY8C21x45, CY8C22x45 Qualification Status

Product Status: In Production

Errata Summary

The following table defines the errata applicable for this PSoC family device.

Items	Part Number	Silicon Revision	Fix Status
1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC	All CY8C21x45, CY8C22x45 devices affected	All	Silicon fix not planned. Use workaround.
2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	All CY8C21x45, CY8C22x45 devices affected	All	Silicon fix not planned. Use workaround.

1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC

■ Problem Definition

In free running mode, there can be a variation of up to 7 LSB in the digital output of SAR10 ADC.

■ Parameters Affected

Code Variation. This is not a specified parameter.

It is defined as the number of unique output codes generated by the ADC for a given constant input voltage, in addition to the correct code. For example, for an input voltage of 2.000 V, the expected code is 190hex and the ADC generates three codes: 191hex, 190hex, and 192hex. The code variation is 2 LSB.

■ Trigger Condition(S)

SAR10 ADC is configured in the free running mode. When ADC is operated in free running mode, for a constant input voltage output of ADC can have a variation of up to 7LSB. This can be resolved by using the averaging technique or by disabling the free running mode before reading the data and enabling again after reading the data.

■ Scope of Impact

Inaccurate output is possible.

■ Workaround

This issue can be averted by using one or both of the following workarounds. Consult a Cypress representative for additional assistance.

- Use the averaging technique. That is, take multiple samples of the input, and use a digital averaging filter.
- Disable the free running mode before reading data out, and enable the free running mode after completing the read operation.

■ Fix Status

No silicon fix is planned.