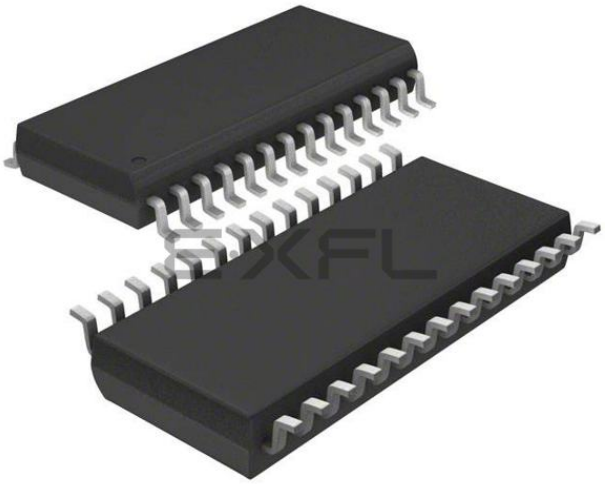


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c22345-24pvxa

The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides a choice of system resources for your application. Family resources are shown in Table 1 on page 5.

Analog System

The Analog System of CY8C21x45 and CY8C22x45 PSoC devices consists of a 10-bit SAR ADC and six configurable analog blocks.

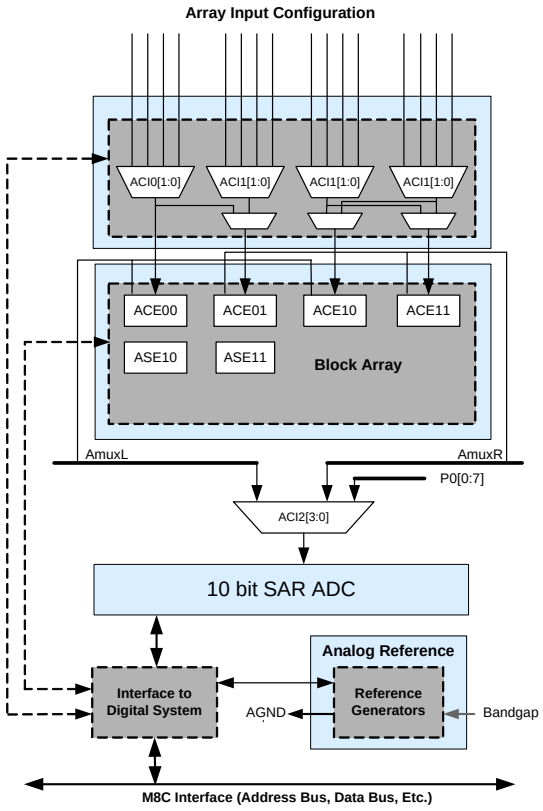
The programmable 10-bit SAR ADC is an optimized ADC with a fast maximum sample rate. External filters are required on ADC input channels for antialiasing. This ensures that any out-of-band content is not folded into the input signal band.

Reconfigurable analog resources allow creating complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (single or dual, with up to 10-bit resolution)
- Pin-to-pin comparator
- Single-ended comparators (up to four) with absolute (1.3 V) reference or DAC reference
- Precision voltage reference (1.3 V nominal)

CY8C21x45 and CY8C22x45 devices have six limited-functionality Type 'E' analog blocks. These analog blocks are arranged in four columns. Each column contains one continuous time (CT) Type E block. The first two columns also have a switched capacitor (SC) type E block. Refer to the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for detailed information on the Type E analog blocks.

Figure 2. Analog System Block Diagram



Haptics TS2000 Controller

The CY8C22x45H family of devices features an easy-to-use Haptics controller resource with up to 14 different effects. These effects are available for use with three different, selectable ERM modules.

Getting Started

For in depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC® device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pinouts

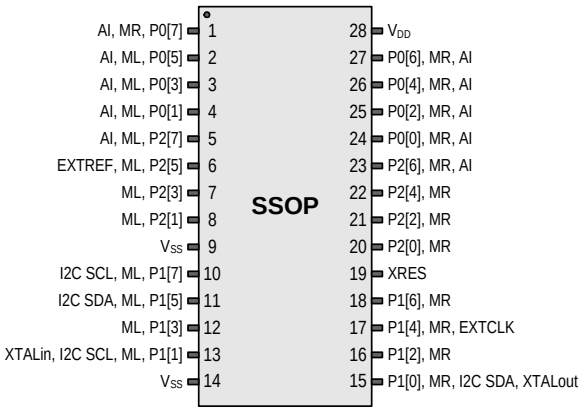
The automotive CY8C21x45 and CY8C22x45 PSoC devices are available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog mux bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

28-pin Part Pinout

Table 2. 28-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, MR	P0[7]	Analog column mux input, C_{MOD} capacitor pin
2	I/O	I, ML	P0[5]	Analog column mux input, C_{MOD} capacitor pin
3	I/O	I, ML	P0[3]	Analog column mux input
4	I/O	I, ML	P0[1]	Analog column mux input
5	I/O	I, ML	P2[7]	Direct input to analog block
6	I/O	ML	P2[5]	Optional SAR ADC external reference (EXTREF)
7	I/O	ML	P2[3]	
8	I/O	ML	P2[1]	
9	Power		V_{SS}	Ground connection
10	I/O	ML	P1[7]	I^2C serial clock (SCL)
11	I/O	ML	P1[5]	I^2C serial data (SDA)
12	I/O	ML	P1[3]	
13	I/O	ML	P1[1]	Crystal input (XTALin), I^2C SCL, ISSP-SCLK[5]
14	Power		V_{SS}	Ground connection
15	I/O	MR	P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA[5]
16	I/O	MR	P1[2]	
17	I/O	MR	P1[4]	Optional external clock input (EXTCLK)
18	I/O	MR	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	MR	P2[0]	
21	I/O	MR	P2[2]	
22	I/O	MR	P2[4]	
23	I/O	I, MR	P2[6]	Direct input to analog block
24	I/O	I, MR	P0[0]	Analog column mux input
25	I/O	I, MR	P0[2]	Analog column mux input
26	I/O	I, MR	P0[4]	Analog column mux input
27	I/O	I, MR	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

Figure 3. CY8C21345 and CY8C22345 28-pin PSoC Device



LEGEND: A = Analog, I = Input, O = Output, MR= Right analog mux bus input, ML= Left analog mux bus input.

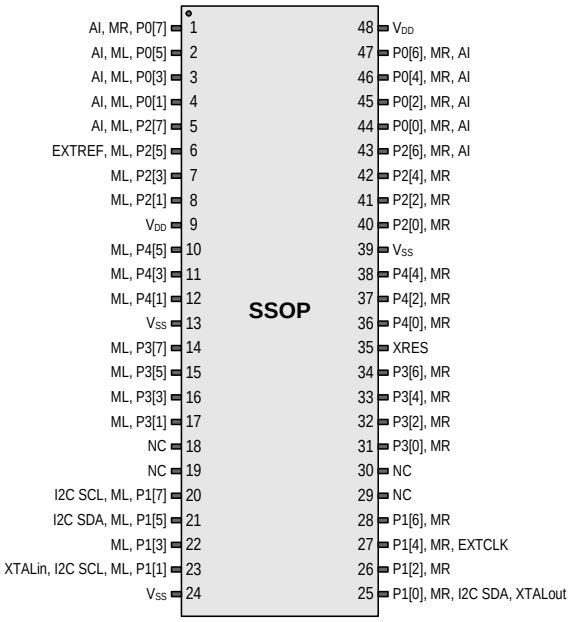
Note
5. These are the ISSP pins, which are not High Z after exiting a reset state. See the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for details.

48-pin Part Pinout

Table 3. 48-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, MR	P0[7]	Analog column mux input, C_{MOD} capacitor pin
2	I/O	I, ML	P0[5]	Analog column mux input, C_{MOD} capacitor pin
3	I/O	I, ML	P0[3]	Analog column mux input
4	I/O	I, ML	P0[1]	Analog column mux input
5	I/O	I, ML	P2[7]	Direct input to analog block
6	I/O	ML	P2[5]	Optional SAR ADC external reference
7	I/O	ML	P2[3]	
8	I/O	ML	P2[1]	
9	Power		V_{DD}	Supply voltage
10	I/O	ML	P4[5]	
11	I/O	ML	P4[3]	
12	I/O	ML	P4[1]	
13	Power		V_{SS}	Ground connection
14	I/O	ML	P3[7]	
15	I/O	ML	P3[5]	
16	I/O	ML	P3[3]	
17	I/O	ML	P3[1]	
18			NC	Not connected
19			NC	Not connected
20	I/O	ML	P1[7]	I^2C serial clock
21	I/O	ML	P1[5]	I^2C serial data
22	I/O	ML	P1[3]	
23	I/O	ML	P1[1]	Crystal input (XTALin), I^2C SCL, ISSP-SCLK[6]
24	Power		V_{SS}	
25	I/O	MR	P1[0]	Crystal output (XTALout), I^2C SDA, ISSP-SDATA[6]
26	I/O	MR	P1[2]	
27	I/O	MR	P1[4]	Optional external clock input
28	I/O	MR	P1[6]	
29			NC	Not connected
30			NC	Not connected
31	I/O	MR	P3[0]	
32	I/O	MR	P3[2]	
33	I/O	MR	P3[4]	
34	I/O	MR	P3[6]	
35	Input		XRES	Active high external reset with internal pull-down
36	I/O	MR	P4[0]	
37	I/O	MR	P4[2]	
38	I/O	MR	P4[4]	
39	Power		V_{SS}	Ground connection
40	I/O	MR	P2[0]	
41	I/O	MR	P2[2]	
42	I/O	MR	P2[4]	

Figure 4. CY8C21645 and CY8C22645 48-pin PSoC Device



Note
6. These are the ISSP pins, which are not High Z after exiting a reset state. See the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for details.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
PRT4DM0	10	RW	CMP0CR1	50	RW		90		GDI_O_IN	D0	RW
PRT4DM1	11	RW	CMP0CR2	51	RW		91		GDI_E_IN	D1	RW
PRT4IC0	12	RW		52			92		GDI_O_OU	D2	RW
PRT4IC1	13	RW	VDAC50CR0	53	RW		93		GDI_E_OU	D3	RW
	14		CMP1CR1	54	RW		94			D4	
	15		CMP1CR2	55	RW		95			D5	
	16			56			96			D6	
	17		VDAC51CR0	57	RW		97			D7	
	18		CSCMPCR0	58	#		98		MUX_CR0	D8	RW
	19		CSCMPGOEN	59	RW		99		MUX_CR1	D9	RW
	1A		CSLUTCR0	5A	RW		9A		MUX_CR2	DA	RW
	1B		CMPCOLMUX	5B	RW		9B		MUX_CR3	DB	RW
	1C		CMPPWMCR	5C	RW		9C		DAC_CR1#	DC	RW
	1D		CMPFLTCR	5D	RW		9D		OSC_GO_EN	DD	RW
	1E		CMPCLK1	5E	RW		9E		OSC_CR4	DE	RW
	1F		CMPCLK0	5F	RW		9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	R
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	V2BG_TR	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	W
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	W
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DBC02CR1	2B	RW	CLK_CR3	6B	RW	SADC_CR3TRIM	AB	RW	ECO_TR	EB	W
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_AD	AD	RW		ED	
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DBC03CR1	2F	RW	TMP_DR3	6F	RW		AF			EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW		71		RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DBC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW	DAC_CR0#	FD	RW
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DBC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. **# Access is bit specific.**

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+150	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ±25 °C. Time spent in storage at a temperature greater than 65 °C counts toward the $Flash_{DR}$ electrical specification in Table 16 on page 20.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied A-grade devices E-grade devices	 –40 –40	 – –	 +85 +125	 °C °C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOz}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature A-grade devices E-grade devices	 –40 –40	 – –	 +85 +125	 °C °C	
T_J	Junction temperature A-grade devices E-grade devices	 –40 –40	 – –	 +100 +135	 °C °C	The temperature rise from ambient to junction is package specific. See Table 27 on page 34. The user must limit the power consumption to comply with this requirement.

Electrical Specifications

This section presents the DC and AC electrical specifications for automotive CY8C21x45 and CY8C22x45 PSoC devices. For the latest electrical specifications, check the most recent data sheet by visiting the web at http://www.cypress.com.

Specifications are valid for A-grade devices at –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 100 °C, and for E-grade devices at –40 °C ≤ T_A ≤ 125 °C, T_J ≤ 135 °C, unless noted otherwise.

Figure 5. Voltage vs. CPU Frequency for A-grade Devices

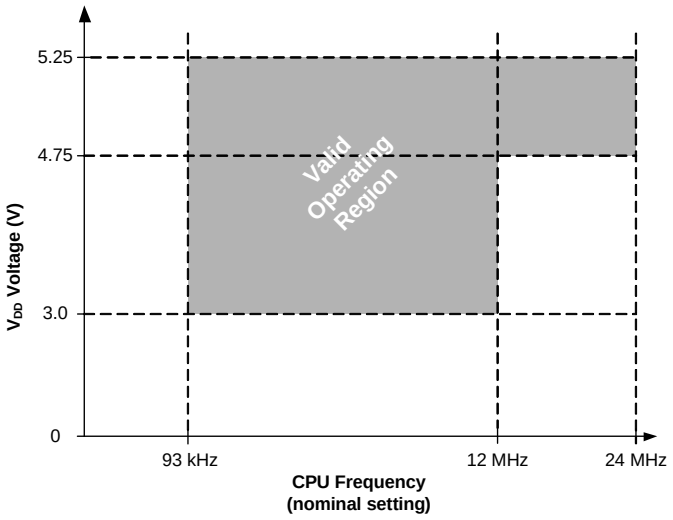


Figure 6. Voltage vs. CPU Frequency for E-grade Devices

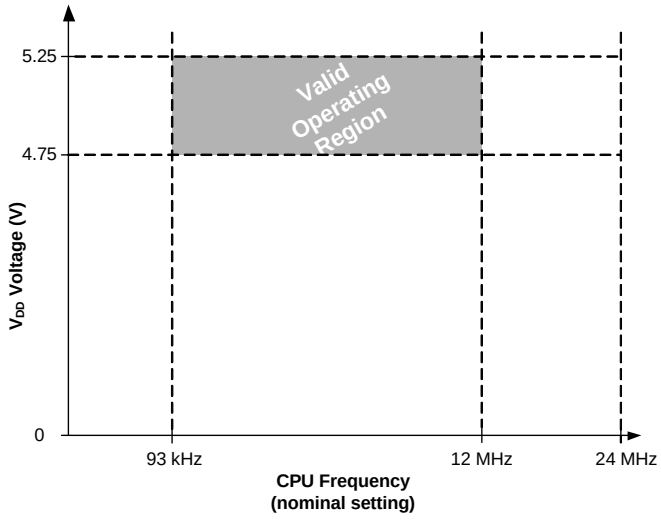
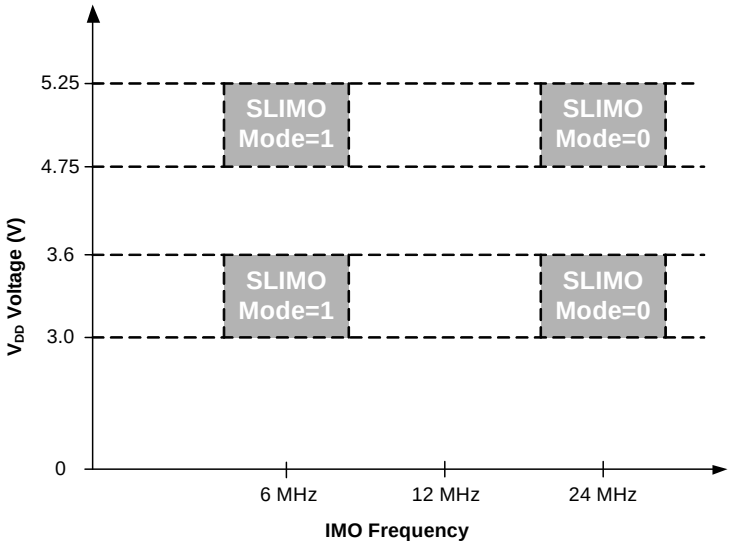


Figure 7. IMO Frequency Trim Options (A-grade Devices Only)



DC GPIO Specifications

Table 10 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 10. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	Also applies to the internal pull-down resistor on the XRES pin
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (80 mA maximum combined I_{OH} budget)
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (100 mA maximum combined I_{OL} budget)
		–	–	0.65	V	I_{OL} = 5 mA, V_{DD} = 3.0 to 3.6 V
I_{OH}	High-level source current	10	–	–	mA	$V_{OH} \geq V_{DD}$ – 1.0 V, see the limitations of the total current in the note for V_{OH}.
I_{OL}	Low-level sink current	25	–	–	mA	$V_{OL} \leq 0.75$ V, see the limitations of the total current in the note for V_{OL}.
V_{IL}	Input low level	–	–	0.8	V	
V_{IH}	Input high level	2.1	–		V	
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C

Table 20. AC Digital Block Specifications (continued)

Function	Description	Min	Typ	Max	Units	Notes
Transmitter	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 Stop Bits	–	–	50.4 [15]	MHz	
	$V_{DD} \geq 4.75$ V, 1 Stop Bit	–	–	25.2 [15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	
Receiver	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 Stop Bits	–	–	50.4 [15]	MHz	
	$V_{DD} \geq 4.75$ V, 1 Stop Bit	–	–	25.2 [15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	

Note
15. Accuracy derived from IMO with appropriate trim for V_{DD} range.

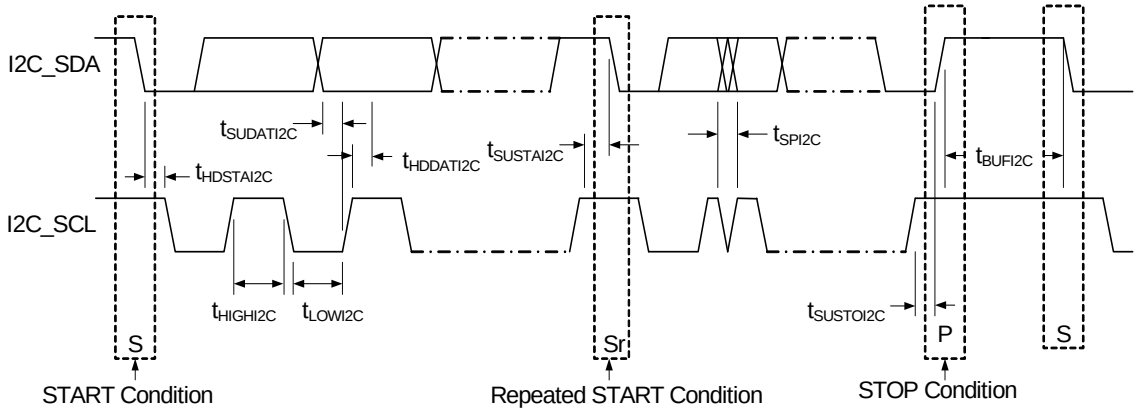
AC I²C Specifications

Table 24 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 24. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100 [17]	0	400 [17]	kHz
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$t_{SUDATI2C}$	Data setup time	250	–	100 [18]	–	ns
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUFI2C}	Bus-free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 9. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

17. F_{SCLI2C} is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the F_{SCLI2C} specification adjusts accordingly.
18. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $t_{SUDATI2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C-bus specification) before the SCL line is released.

Development Tool Selection

This section presents the development tools available for the automotive CY8C21x45 and CY8C22x45 families.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the contents of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- ICE-Cube unit
- 28-pin PDIP emulation pod for CY8C29466-24PXI
- 28-pin CY8C29466-24PXI PDIP PSoC device samples (two)
- PSoC Designer software CD
- ISSP cable
- MiniEval socket programming and evaluation board
- Backward compatibility cable (for connecting to legacy pods)
- Universal 110/220 power supply (12 V)
- European plug adapter
- USB 2.0 cable
- Getting Started guide
- Development kit registration form

CY3280-22X45 Universal CapSense Controller Board

The CY3280-22X45 controller board is an additional controller board for the CY3280-BK1 Universal CapSense Controller Kit. The Universal CapSense Controller kit is designed for easy prototyping and debug of CapSense designs with pre-defined control circuitry and plug-in hardware. The CY3280-22X45 kit contains no plug-in hardware. Therefore, it is only usable if plug-in hardware is purchased as part of the CY3280-BK1 kit or other separate kits. The kit includes:

- CY3280-22X45 universal CapSense controller board
- CY3280-22X45 universal CapSense controller board CD
- DC power supply
- Printed documentation

CY3280-CPM1 CapSensePlus Module

The CY3280-CPM1 CapSensePlus Module is a plug-in module board for the CY3280-22X45 CapSense controller board kit. This plug-in module has no capacitive sensors on it. Instead, it has other general circuitry (such as a seven-segment display, potentiometer, LEDs, buttons, thermistor) that can be used to develop applications that require capacitive sensing along with other additional functionality. To use this kit, a CY3280-22X45 kit is required.

Evaluation Tools

All evaluation tools can be purchased from the Cypress online store. The online store also has the most up-to-date information on kit contents, descriptions, and availability.

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-pin CY8C29466-24PXI PDIP PSoC device sample (two)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows the user to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240-V power supply, Euro-Plug adapter
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 25. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit [19]	Foot Kit [20]	Prototyping Module	Adapter [21]
CY8C21345-24PVXA CY8C21345-12PVXE CY8C22345-24PVXA CY8C22345H-24PVXA CY8C22345-12PVXE	28-pin SSOP	CY3250-22345	CY3250-28SSOP-FK	–	AS-28-28-02SS-6ENP-GANG
CY8C21645-24PVXA CY8C21645-12PVXE CY8C22645-24PVXA CY8C22645-12PVXE	48-pin SSOP	–	–	–	AS-48-48-01SS-6-GANG

Notes
19. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
20. Foot kit includes surface mount feet that can be soldered to the target PCB.
21. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

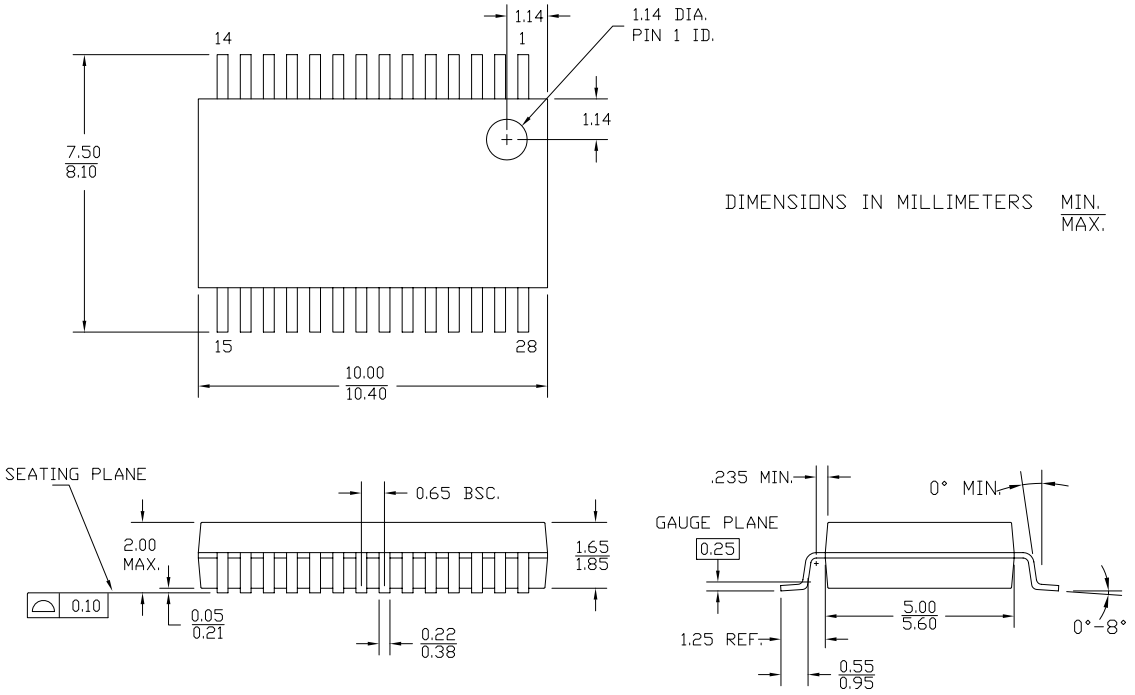
Packaging Information

This section provides the packaging specifications for the automotive CY8C21x45 and CY8C22x45 PSoC devices. The thermal impedances for each package and the typical package capacitance on crystal pins are given.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Package Dimensions

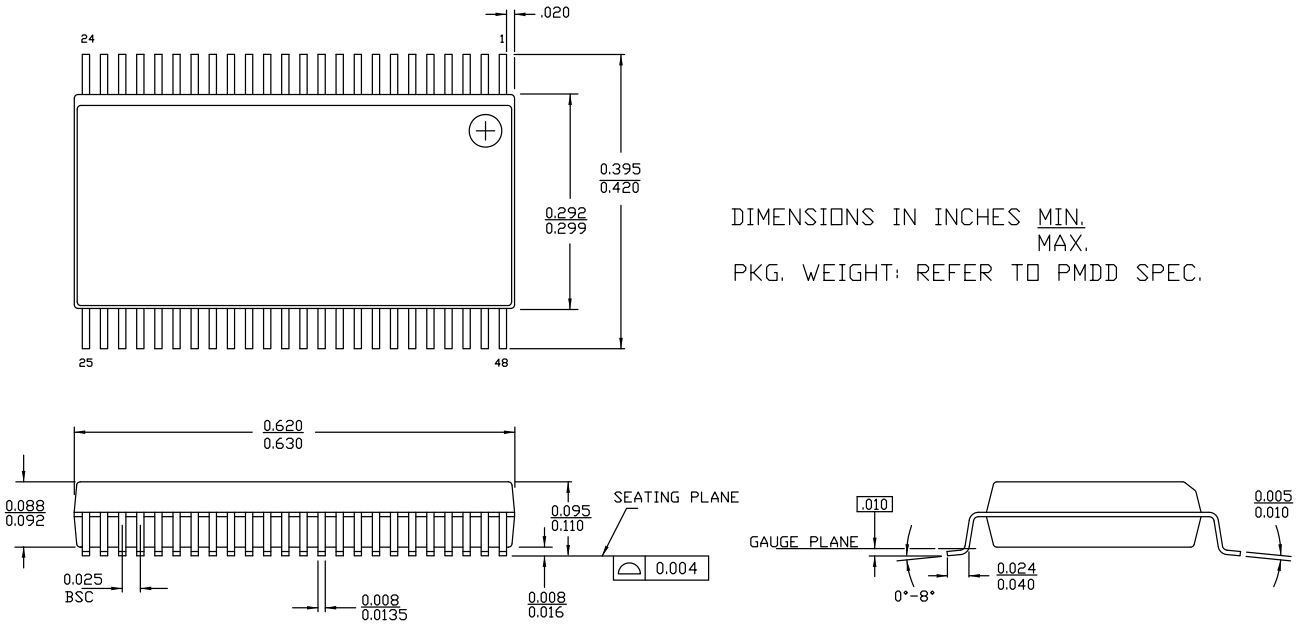
Figure 10. 28-pin SSOP (210 Mils) Package Outline, 51-85079



51-85079 *E

Packaging Information (continued)

Figure 11. 48-pin SSOP (300 Mils) Package Outline, 51-85061



Thermal Impedances

Table 27. Thermal Impedances per Package

Package	Typical θ_{JA} [22]
28-pin SSOP	97.6 °C/W
48-pin SSOP	69 °C/W

Capacitance on Crystal Pins

Table 28. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28-pin SSOP	2.8 pF
48-pin SSOP	3.3 pF

Solder Reflow Specifications

Table 29 shows the solder reflow temperature limits that must not be exceeded.

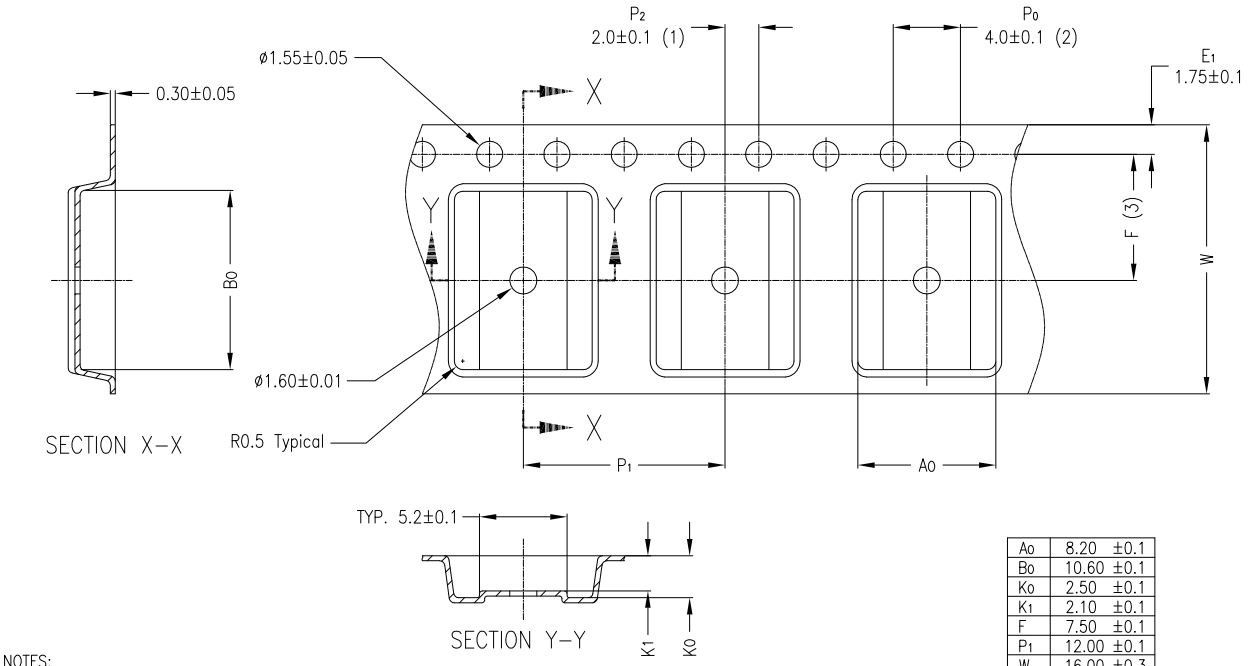
Table 29. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
28-pin SSOP	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds

Note
22. $T_J = T_A + POWER \times \theta_{JA}$

Tape and Reel Information

Figure 12. 28-pin SSOP (209 Mils) Carrier Tape, 51-51100



A0	8.20 ±0.1
B0	10.60 ±0.1
K0	2.50 ±0.1
K1	2.10 ±0.1
F	7.50 ±0.1
P1	12.00 ±0.1
W	16.00 ±0.3

NOTES:
(1) Measured from centerline of sprocket hole to centerline of pocket.
(2) Cumulative tolerance of 10 sprocket holes is ± 0.10.
(3) Measured from centerline of sprocket hole to centerline of pocket
4 Material: Conductive Polystyrene
5 Camber not to exceed 1mm in 100mm
6 Supplier P/N: SSOP28–3 CL3 22B3 Lxx W16

51-51100 *D

Document Conventions

Units of Measure

Table 32 lists the units of measure that are used in this document.

Table 32. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	ms	millisecond
°C	degree Celsius	mV	millivolt
kHz	kilohertz	nA	nanoampere
kΩ	kilohm	ns	nanosecond
LSbit	least-significant bit	W	ohm
MHz	megahertz	%	percent
µA	microampere	pF	picofarad
µs	microsecond	ps	picosecond
µV	microvolt	pA	picoampere
mA	milliampere	V	volt
mm	millimeter	W	watt

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

Glossary (continued)

external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device***.
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.

Glossary (continued)

SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***Application Programming Interface (API)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

■ **Problem Definition**

Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

■ **Parameters Affected**

The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.

■ **Trigger Condiiton(S)**

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.

■ **Scope of Impact**

This problem may affect UART, IrDA, and FSK implementations.

■ **Workaround**

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

■ **Fix Status**

The cause of this problem and its solution has been identified. No silicon fix is planned to correct the deficiency in silicon.