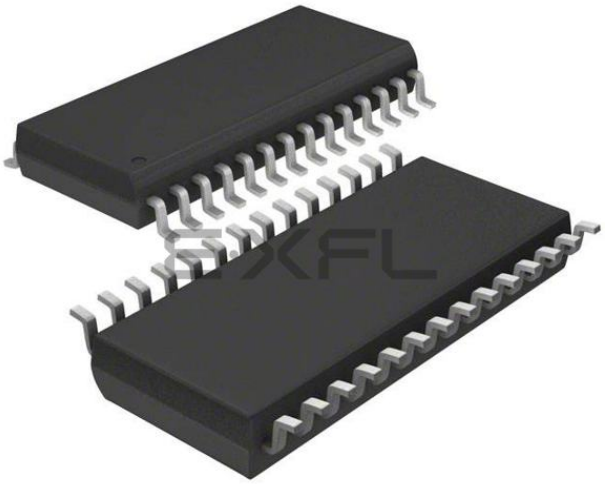


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | M8C |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 24 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.25V |
| Data Converters | A/D 3x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c22345h-24pvxa |

## Contents

The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides a choice of system resources for your application. Family resources are shown in Table 1 on page 5.

## Analog System

The Analog System of CY8C21x45 and CY8C22x45 PSoC devices consists of a 10-bit SAR ADC and six configurable analog blocks.

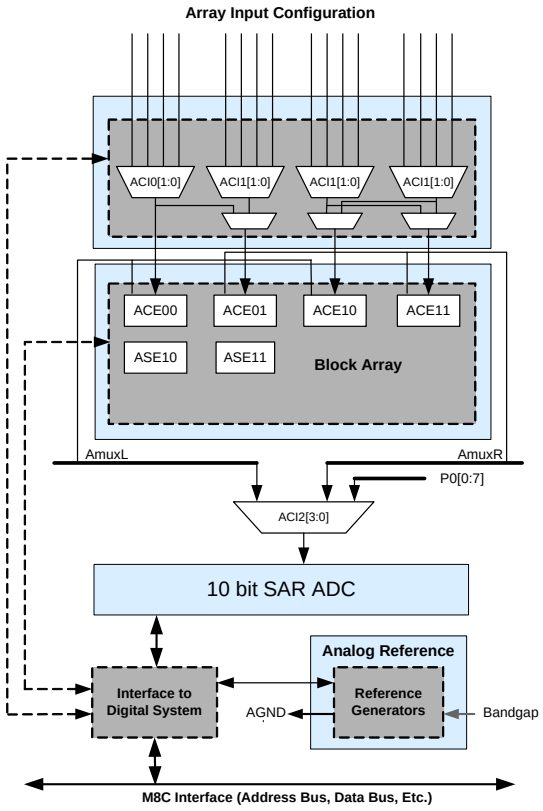
The programmable 10-bit SAR ADC is an optimized ADC with a fast maximum sample rate. External filters are required on ADC input channels for antialiasing. This ensures that any out-of-band content is not folded into the input signal band.

Reconfigurable analog resources allow creating complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (single or dual, with up to 10-bit resolution)
- Pin-to-pin comparator
- Single-ended comparators (up to four) with absolute (1.3 V) reference or DAC reference
- Precision voltage reference (1.3 V nominal)

CY8C21x45 and CY8C22x45 devices have six limited-functionality Type 'E' analog blocks. These analog blocks are arranged in four columns. Each column contains one continuous time (CT) Type E block. The first two columns also have a switched capacitor (SC) type E block. Refer to the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for detailed information on the Type E analog blocks.

**Figure 2. Analog System Block Diagram**




## Haptics TS2000 Controller

The CY8C22x45H family of devices features an easy-to-use Haptics controller resource with up to 14 different effects. These effects are available for use with three different, selectable ERM modules.

## Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful for complete systems. Additional resources include a MAC, low voltage detection, and power on reset. The merits of each system resource are:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Additional digital resources and clocks dedicated to and optimized for CapSense.
- RTC hardware block.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The $I^2C$ module provides 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power on reset (POR) circuit eliminates the need for a system supervisor.
- An internal voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

## PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have varying numbers of digital and analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC families covered by this datasheet are highlighted in the table.

**Table 1. PSoC Device Characteristics**

| PSoC Part Number | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|---|---|---|---|---|---|---|---|---|---|
| CY8C29x66 [2] | up to 64 | 4 | 16 | up to 12 | 4 | 4 | 12 | 2 K | 32 K |
| CY8C28xxx | up to 44 | up to 3 | up to 12 | up to 44 | up to 4 | up to 6 | up to 12 + 4 [3] | 1 K | 16 K |
| CY8C27x43 | up to 44 | 2 | 8 | up to 12 | 4 | 4 | 12 | 256 | 16 K |
| CY8C24x94 [2] | up to 56 | 1 | 4 | up to 48 | 2 | 2 | 6 | 1 K | 16 K |
| CY8C24x23A [2] | up to 24 | 1 | 4 | up to 12 | 2 | 2 | 6 | 256 | 4 K |
| CY8C23x33 | up to 26 | 1 | 4 | up to 12 | 2 | 2 | 4 | 256 | 8 K |
| CY8C22x45 [2] | up to 38 | 2 | 8 | up to 38 | 0 | 4 | 6 [3] | 1 K | 16 K |
| CY8C21x45 [2] | up to 24 | 1 | 4 | up to 24 | 0 | 4 | 6 [3] | 512 | 8 K |
| CY8C21x34 [2] | up to 28 | 1 | 4 | up to 28 | 0 | 2 | 4 [3] | 512 | 8 K |
| CY8C21x23 | up to 16 | 1 | 4 | up to 8 | 0 | 2 | 4 [3] | 256 | 4 K |
| CY8C20x34 [2] | up to 28 | 0 | 0 | up to 28 | 0 | 0 | 3 [3, 4] | 512 | 8 K |
| CY8C20xx6 | up to 36 | 0 | 0 | up to 36 | 0 | 0 | 3 [3, 4] | up to 2 K | up to 32 K |

**Notes**
2. Automotive qualified devices available in this group.
3. Limited analog functionality.
4. Two analog blocks and one CapSense® block.

**C Language Compilers**. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

*Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

*Online Help System*

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

*In-Circuit Emulator*

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

## Designing with PSoC Designer

The development process for the PSoC® device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

### Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

### Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

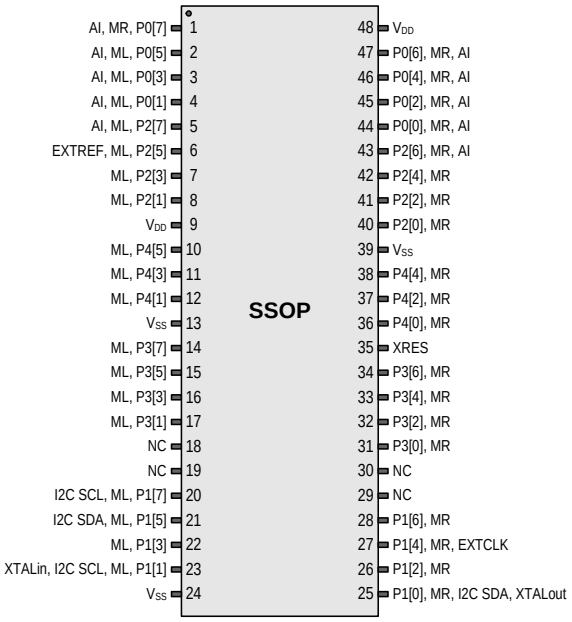
The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

## 48-pin Part Pinout

**Table 3. 48-pin Part Pinout (SSOP)**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I, MR | P0[7] | Analog column mux input, $C_{MOD}$ capacitor pin |
| 2 | I/O | I, ML | P0[5] | Analog column mux input, $C_{MOD}$ capacitor pin |
| 3 | I/O | I, ML | P0[3] | Analog column mux input |
| 4 | I/O | I, ML | P0[1] | Analog column mux input |
| 5 | I/O | I, ML | P2[7] | Direct input to analog block |
| 6 | I/O | ML | P2[5] | Optional SAR ADC external reference |
| 7 | I/O | ML | P2[3] | |
| 8 | I/O | ML | P2[1] | |
| 9 | Power | | $V_{DD}$ | Supply voltage |
| 10 | I/O | ML | P4[5] | |
| 11 | I/O | ML | P4[3] | |
| 12 | I/O | ML | P4[1] | |
| 13 | Power | | $V_{SS}$ | Ground connection |
| 14 | I/O | ML | P3[7] | |
| 15 | I/O | ML | P3[5] | |
| 16 | I/O | ML | P3[3] | |
| 17 | I/O | ML | P3[1] | |
| 18 | | | NC | Not connected |
| 19 | | | NC | Not connected |
| 20 | I/O | ML | P1[7] | $I^2C$ serial clock |
| 21 | I/O | ML | P1[5] | $I^2C$ serial data |
| 22 | I/O | ML | P1[3] | |
| 23 | I/O | ML | P1[1] | Crystal input (XTALin), $I^2C$ SCL, ISSP-SCLK[6] |
| 24 | Power | | $V_{SS}$ | |
| 25 | I/O | MR | P1[0] | Crystal output (XTALout), $I^2C$ SDA, ISSP-SDATA[6] |
| 26 | I/O | MR | P1[2] | |
| 27 | I/O | MR | P1[4] | Optional external clock input |
| 28 | I/O | MR | P1[6] | |
| 29 | | | NC | Not connected |
| 30 | | | NC | Not connected |
| 31 | I/O | MR | P3[0] | |
| 32 | I/O | MR | P3[2] | |
| 33 | I/O | MR | P3[4] | |
| 34 | I/O | MR | P3[6] | |
| 35 | Input | | XRES | Active high external reset with internal pull-down |
| 36 | I/O | MR | P4[0] | |
| 37 | I/O | MR | P4[2] | |
| 38 | I/O | MR | P4[4] | |
| 39 | Power | | $V_{SS}$ | Ground connection |
| 40 | I/O | MR | P2[0] | |
| 41 | I/O | MR | P2[2] | |
| 42 | I/O | MR | P2[4] | |

**Figure 4. CY8C21645 and CY8C22645 48-pin PSoC Device**




**Note**
6. These are the ISSP pins, which are not High Z after exiting a reset state. See the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices for details.

**Table 3. 48-pin Part Pinout (SSOP)** (continued)

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 43 | I/O | I, MR | P2[6] | Direct input to analog block |
| 44 | I/O | I, MR | P0[0] | Analog column mux input |
| 45 | I/O | I, MR | P0[2] | Analog column mux input |
| 46 | I/O | I, MR | P0[4] | Analog column mux input |
| 47 | I/O | I, MR | P0[6] | Analog column mux input |
| 48 | Power | | $V_{DD}$ | Supply voltage |

**LEGEND**: A = Analog, I = Input, O = Output, MR= Right analog mux bus input, ML= Left analog mux bus input

## Registers

This section lists the registers of this PSoC device family by mapping tables. For detailed register information, refer to the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices.

### Register Conventions

The register conventions specific to this section are listed in the following table.

**Table 4. Abbreviations**

| Convention | Description |
|---|---|
| RW | Read and write register or bit(s) |
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

### Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are Reserved and must not be accessed.

**Table 5. Register Map Bank 0 Table: User Space**

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0GS | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1GS | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DR | 08 | RW | | 48 | | | 88 | | PWMVREF0 | C8 | # |
| PRT2IE | 09 | RW | | 49 | | | 89 | | PWMVREF1 | C9 | # |
| PRT2GS | 0A | RW | | 4A | | | 8A | | IDAC_MODE | CA | RW |
| PRT2DM2 | 0B | RW | | 4B | | | 8B | | PWM_SRC | CB | # |
| PRT3DR | 0C | RW | | 4C | | | 8C | | TS_CR0 | CC | RW |
| PRT3IE | 0D | RW | | 4D | | | 8D | | TS_CMPH | CD | RW |
| PRT3GS | 0E | RW | | 4E | | | 8E | | TS_CMPL | CE | RW |
| PRT3DM2 | 0F | RW | | 4F | | | 8F | | TS_CR1 | CF | RW |
| PRT4DR | 10 | RW | CSD0_DR0_L | 50 | R | | 90 | | CUR PP | D0 | RW |
| PRT4IE | 11 | RW | CSD0_DR1_L | 51 | W | | 91 | | STK_PP | D1 | RW |
| PRT4GS | 12 | RW | CSD0_CNT_L | 52 | R | | 92 | | | D2 | |
| PRT4DM2 | 13 | RW | CSD0_CR0 | 53 | # | | 93 | | IDX_PP | D3 | RW |
| | 14 | | CSD0_DR0_H | 54 | R | | 94 | | MVR_PP | D4 | RW |
| | 15 | | CSD0_DR1_H | 55 | W | | 95 | | MVW_PP | D5 | RW |
| | 16 | | CSD0_CNT_H | 56 | R | | 96 | | I2C0_CFG | D6 | RW |
| | 17 | | CSD0_CR1 | 57 | RW | | 97 | | I2C0_SCR | D7 | # |
| | 18 | | CSD1_DR0_L | 58 | R | | 98 | | I2C0_DR | D8 | RW |
| | 19 | | CSD1_DR1_L | 59 | W | | 99 | | I2C0_MSCR | D9 | # |
| | 1A | | CSD1_CNT_L | 5A | R | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | CSD1_CR0 | 5B | # | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | CSD1_DR0_H | 5C | R | | 9C | | INT_CLR2 | DC | RW |
| | 1D | | CSD1_DR1_H | 5D | W | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | CSD1_CNT_H | 5E | R | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | CSD1_CR1 | 5F | RW | | 9F | | INT_MSK2 | DF | RW |
| DBC00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBC00DR1 | 21 | W | AMUX_CFG | 61 | RW | | A1 | | INT_MSK1 | E1 | RW |
| DBC00DR2 | 22 | RW | PWM_CR | 62 | RW | | A2 | | INT_VC | E2 | RC |
| DBC00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBC01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | | | |
| DBC01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | | | |
| DBC01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC _CR0 | E6 | RW |
| DBC01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCC02DR0 | 28 | # | ADC0_CR | 68 | # | | A8 | | MUL0_X | E8 | W |
| DCC02DR1 | 29 | W | ADC1_CR | 69 | # | | A9 | | MUL0_Y | E9 | W |
| DCC02DR2 | 2A | RW | SADC_DH | 6A | RW | | AA | | MUL0_DH | EA | R |
| DCC02CR0 | 2B | # | SADC_DL | 6B | RW | | AB | | MUL0_DL | EB | R |
| DCC03DR0 | 2C | # | TMP_DR0 | 6C | RW | | AC | | ACC0_DR1 | EC | RW |
| DCC03DR1 | 2D | W | TMP_DR1 | 6D | RW | | AD | | ACC0_DR0 | ED | RW |
| DCC03DR2 | 2E | RW | TMP_DR2 | 6E | RW | | AE | | ACC0_DR3 | EE | RW |
| DCC03CR0 | 2F | # | TMP_DR3 | 6F | RW | | AF | | ACC0_DR2 | EF | RW |
| DBC10DR0 | 30 | # | | 70 | | RDI0RI | B0 | RW | | F0 | |
| DBC10DR1 | 31 | W | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| DBC10DR2 | 32 | RW | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| DBC10CR0 | 33 | # | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBC11DR0 | 34 | # | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| DBC11DR1 | 35 | W | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| DBC11DR2 | 36 | RW | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| DBC11CR0 | 37 | # | ACE01CR2 | 77 | RW | RDI0DSM | B7 | RW | CPU_F | F7 | RL |
| DCC12DR0 | 38 | # | | 78 | | RDI1RI | B8 | RW | | F8 | |
| DCC12DR1 | 39 | W | | 79 | | RDI1SYN | B9 | RW | | F9 | |
| DCC12DR2 | 3A | RW | | 7A | | RDI1IS | BA | RW | | FA | |
| DCC12CR0 | 3B | # | | 7B | | RDI1LT0 | BB | RW | | FB | |
| DCC13DR0 | 3C | # | | 7C | | RDI1LT1 | BC | RW | IDACR_D | FC | RW |
| DCC13DR1 | 3D | W | | 7D | | RDI1RO0 | BD | RW | IDACL_D | FD | RW |
| DCC13DR2 | 3E | RW | | 7E | | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| DCC13CR0 | 3F | # | | 7F | | RDI1DSM | BF | RW | CPU_SCR0 | FF | # |

**Blank fields are Reserved and must not be accessed.** **# Access is bit specific.**

## DC Electrical Characteristics

*DC Chip Level Specifications*

Table 9 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 9. DC Chip Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage<br>A-grade devices<br>E-grade devices | <br>3.0<br>4.75 | <br>–<br>– | <br>5.25<br>5.25 | <br>V<br>V | See Table 15 on page 19 |
| $I_{DD}$ | Supply current<br>A-grade devices, 3.0 V ≤ $V_{DD}$ ≤ 3.6 V<br>A-grade devices, 4.75 V ≤ $V_{DD}$ ≤ 5.25 V<br>E-grade devices | <br>–<br>–<br>– | <br>4<br>7<br>8 | <br>7<br>12<br>15 | <br>mA<br>mA<br>mA | CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, Analog blocks disabled |
| $I_{SB}$ | Sleep (mode) current<br>A-grade devices, 3.0 V ≤ $V_{DD}$ ≤ 3.6 V<br>A-grade devices, 4.75 V ≤ $V_{DD}$ ≤ 5.25 V<br>E-grade devices | <br>–<br>–<br>– | <br>3<br>4<br>4 | <br>12<br>25<br>25 | <br>µA<br>µA<br>µA | Everything disabled except ILO, POR, LVD, Sleep Timer, and WDT circuits |
| $I_{SBXTL}$ | Sleep (mode) current with ECO<br>A-grade devices, 3.0 V ≤ $V_{DD}$ ≤ 3.6 V<br>A-grade devices, 4.75 V ≤ $V_{DD}$ ≤ 5.25 V<br>E-grade devices | <br>–<br>–<br>– | <br>4<br>5<br>5 | <br>13<br>26<br>26 | <br>µA<br>µA<br>µA | Everything disabled except ECO, POR, LVD, Sleep Timer, and WDT circuits |
| $V_{REF}$ | Reference voltage (Bandgap) | 1.275 | 1.30 | 1.325 | V | Trimmed for appropriate $V_{DD}$ setting. |

*DC Operational Amplifier Specifications*

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25°C, unless specified otherwise, and are for design guidance only.

**Table 11. DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input offset voltage (absolute value) | – | 2.5 | 15 | mV | |
| $I_{SOA}$ | Supply current (absolute value)<br>A-grade devices<br>E-grade devices | <br>–<br>– | <br>–<br>– | <br>30<br>35 | <br>µA<br>µA | |
| $TCV_{OSOA}$ | Average input offset voltage drift | – | 10 | – | µV/°C | |
| $I_{EBOA}$[7] | Input leakage current (Port 0 analog pins) | – | 200 | – | pA | Gross tested to 1 µA |
| $C_{INOA}$ | Input capacitance (Port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. $T_A$ = 25 °C |
| $V_{CMOA}$ | Common mode voltage range | 0.5 | – | $V_{DD}$ – 1 | V | |

*DC IDAC Specifications*

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 12. DC IDAC Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $IDAC_{GAIN}$ | IDAC gain | – | 75.4 | 218 | nA/bit | IDAC gain at 1x current gain |
| | | – | 335 | 693 | nA/bit | IDAC gain at 4x current gain |
| | | – | 1160 | 2410 | nA/bit | IDAC gain at 16x current gain |
| | | – | 2340 | 5700 | nA/bit | IDAC gain at 32x current gain |
| | Monotonicity | No | – | – | – | IDAC gain is non-monotonous at step intervals of (0x10) |
| $IDAC_{GAIN\_VAR}$ | IDAC gain variation over temperature –40 °C to 85 °C | – | 3.22 | – | nA | at 1x current gain |
| | | – | 18.1 | – | nA | at 4x current gain |
| | | – | 59.9 | – | nA | at 16x current gain |
| | | – | 120 | – | nA | at 32x current gain |
| $I_{IDAC}$ | IDAC current at maximum code (0xFF) | – | 19.2 | – | µA | at 1x current gain |
| | | – | 85.4 | – | µA | at 4x current gain |
| | | – | 295 | – | µA | at 16x current gain |
| | | – | 596 | – | µA | at 32x current gain |

**Note**
7. Atypical behavior: $I_{EBOA}$ of Port 0 Pin 0 is below 1 nA at 25 °C; 50 nA over temperature. Use Port 0 Pins 1 – 7 for the lowest leakage of 200 nA.

*DC POR and LVD Specifications*

Table 15 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 15. DC POR and LVD Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| | $V_{DD}$ value for PPOR trip | | | | | $V_{DD}$ must be greater than or equal to 3.0 V during startup, reset from the XRES pin, or reset from Watchdog. |
| $V_{PPOR1}$ | PORLEV[1:0] = 01b | – | 2.82 | 2.95 | V | |
| $V_{PPOR2}$ | PORLEV[1:0] = 10b | – | 4.55 | 4.73 | V | |
| | $V_{DD}$ value for LVD trip | | | | | |
| $V_{LVD2}$ | VM[2:0] = 010b | 2.95 | 3.02 | 3.09 | V | |
| $V_{LVD3}$ | VM[2:0] = 011b | 3.06 | 3.13 | 3.20 | V | |
| $V_{LVD4}$ | VM[2:0] = 100b | 4.37 | 4.48 | 4.55 | V | |
| $V_{LVD5}$ | VM[2:0] = 101b | 4.50 | 4.64 | 4.75 | V | |
| $V_{LVD6}$ | VM[2:0] = 110b | 4.62 | 4.73 | 4.83 | V | |
| $V_{LVD7}$ | VM[2:0] = 111b | 4.71 | 4.81 | 4.95 | V | |

*DC Programming Specifications*

Table 16 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 16. DC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{DDP}$ | $V_{DD}$ for programming and erase | 4.5 | 5 | 5.5 | V | This specification applies to the functional requirements of external programmer tools |
| $V_{DDLV}$ | Low $V_{DD}$ for verify<br>A-grade devices<br>E-grade devices | <br>3.0<br>4.7 | <br>3.1<br>4.8 | <br>3.2<br>4.9 | <br>V<br>V | This specification applies to the functional requirements of external programmer tools |
| $V_{DDHV}$ | High $V_{DD}$ for verify | 5.1 | 5.2 | 5.3 | V | This specification applies to the functional requirements of external programmer tools |
| $V_{DDIWRITE}$ | Supply voltage for flash write operation<br>A-grade devices<br>E-grade devices | <br>3.0<br>4.75 | <br>–<br>– | <br>5.25<br>5.25 | <br>V<br>V | This specification applies to this device when it is executing internal flash writes |
| $I_{DDP}$ | Supply current during programming or verify | – | 5 | 25 | mA | |
| $V_{ILP}$ | Input low voltage during programming or verify | – | – | 0.8 | V | |
| $V_{IHP}$ | Input high voltage during programming or verify | 2.2 | – | – | V | |
| $I_{ILP}$ | Input current when applying $V_{ILP}$ to P1[0] or P1[1] during programming or verify | – | – | 0.2 | mA | Driving internal pull-down resistor |
| $I_{IHP}$ | Input current when applying $V_{IHP}$ to P1[0] or P1[1] during programming or verify | – | – | 1.5 | mA | Driving internal pull-down resistor |
| $V_{OLV}$ | Output low voltage during programming or verify | – | – | 0.75 | V | |
| $V_{OHV}$ | Output high voltage during programming or verify | $V_{DD}$ – 1.0 | – | $V_{DD}$ | V | |
| $Flash_{ENPB}$ | Flash endurance (per block) [8, 9]<br>A-grade devices<br>E-grade devices | <br>1,000<br>100 | <br>–<br>– | <br>–<br>– | <br>–<br>– | Erase/write cycles per block |
| $Flash_{ENT}$ | Flash endurance (total) [9, 10]<br>CY8C21x45 A-grade devices<br>CY8C22x45 A-grade devices<br>CY8C21x45 E-grade devices<br>CY8C22x45 E-grade devices | <br>128,000<br>256,000<br>12,800<br>25,600 | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | Erase/write cycles |
| $Flash_{DR}$ | Flash data retention [9]<br>A-grade devices<br>E-grade devices | <br>10<br>10 | <br>–<br>– | <br>–<br>– | <br>Years<br>Years | |

**Notes**

8. The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
10. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.

*AC Digital Block Specifications*

The following tables list the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 20. AC Digital Block Specifications**

| Function | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| All functions | Block Input Clock Frequency | | | | | |
| | $V_{DD} \geq 4.75$ V | – | – | 50.4 [15] | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 25.2 [15] | MHz | |
| Timer | Input Clock Frequency | | | | | |
| | No Capture, $V_{DD} \geq 4.75$ V | – | – | 50.4 [15] | MHz | |
| | No Capture, $V_{DD} < 4.75$ V | – | – | 25.2 [15] | MHz | |
| | With Capture | – | – | 25.2 [15] | MHz | |
| | Capture Pulse Width | 50 [14] | – | – | ns | |
| Counter | Input Clock Frequency | | | | | |
| | No Enable Input, $V_{DD} \geq 4.75$ V | – | – | 50.4 [15] | MHz | |
| | No Enable Input, $V_{DD} < 4.75$ V | – | – | 25.2 [15] | MHz | |
| | With Enable Input | – | – | 25.2 [15] | MHz | |
| | Enable Input Pulse Width | 50 [14] | – | – | ns | |
| Dead Band | Kill Pulse Width | | | | | |
| | Asynchronous Restart Mode | 20 | – | – | ns | |
| | Synchronous Restart Mode | 50 [14] | – | – | ns | |
| | Disable Mode | 50 [14] | – | – | ns | |
| | Input Clock Frequency | | | | | |
| | $V_{DD} \geq 4.75$ V | – | – | 50.4 [15] | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 25.2 [15] | MHz | |
| CRCPRS (PRS Mode) | Input Clock Frequency | | | | | |
| | $V_{DD} \geq 4.75$ V | – | – | 50.4 [15] | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 25.2 [15] | MHz | |
| CRCPRS (CRC Mode) | Input Clock Frequency | – | – | 25.2 [15] | MHz | |
| SPIM | Input Clock Frequency | – | – | 8.4 [15] | MHz | The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2. |
| SPIS | Input Clock (SCLK) Frequency | – | – | 4.2 [15] | MHz | The input clock is the SPI SCLK in SPIS mode. |
| | Width of SS_Negated Between Transmissions | 50 [14] | – | – | ns | |

**Note**
14. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

*AC Programming Specifications*

Table 23 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

**Table 23. AC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{RSCLK}$ | Rise time of SCLK | 1 | – | 20 | ns | |
| $t_{FSCLK}$ | Fall time of SCLK | 1 | – | 20 | ns | |
| $t_{SSCLK}$ | Data setup time to falling edge of SCLK | 40 | – | – | ns | |
| $t_{HSCLK}$ | Data hold time from falling edge of SCLK | 40 | – | – | ns | |
| $F_{SCLK}$ | Frequency of SCLK | 0 | – | 8 | MHz | |
| $F_{SCLK3}$ | Frequency of SCLK | 0 | – | 6 | MHz | $V_{DD} \leq 3.6$ V |
| $t_{ERASEB}$ | Flash erase time (block) | – | 10 | 40 [16] | ms | |
| $t_{WRITE}$ | Flash block write time | – | 40 | 160 [16] | ms | |
| $t_{DSCLK}$ | Data out delay from falling edge of SCLK | – | – | 55 | ns | $V_{DD} > 3.6$ V, 30 pF load |
| $t_{DSCLK3}$ | Data out delay from falling edge of SCLK | – | – | 65 | ns | 3.0 V $\leq V_{DD} \leq$ 3.6 V, 30 pF load |
| $t_{PRGH}$ | Total flash block program time ($t_{ERASEB} + t_{WRITE}$), hot | – | – | 100 [16] | ms | $T_J \geq 0$ °C |
| $t_{PRGC}$ | Total flash block program time ($t_{ERASEB} + t_{WRITE}$), cold | – | – | 200 [16] | ms | $T_J < 0$ °C |

**Note**
16. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.

## Device Programmers

All device programmers can be purchased from the Cypress Online Store.

*CY3210-MiniProg1*

The CY3210-MiniProg1 kit allows the user to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

*CY3207ISSP In-System Serial Programmer*

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

**Note** CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240-V power supply, Euro-Plug adapter
- USB 2.0 cable

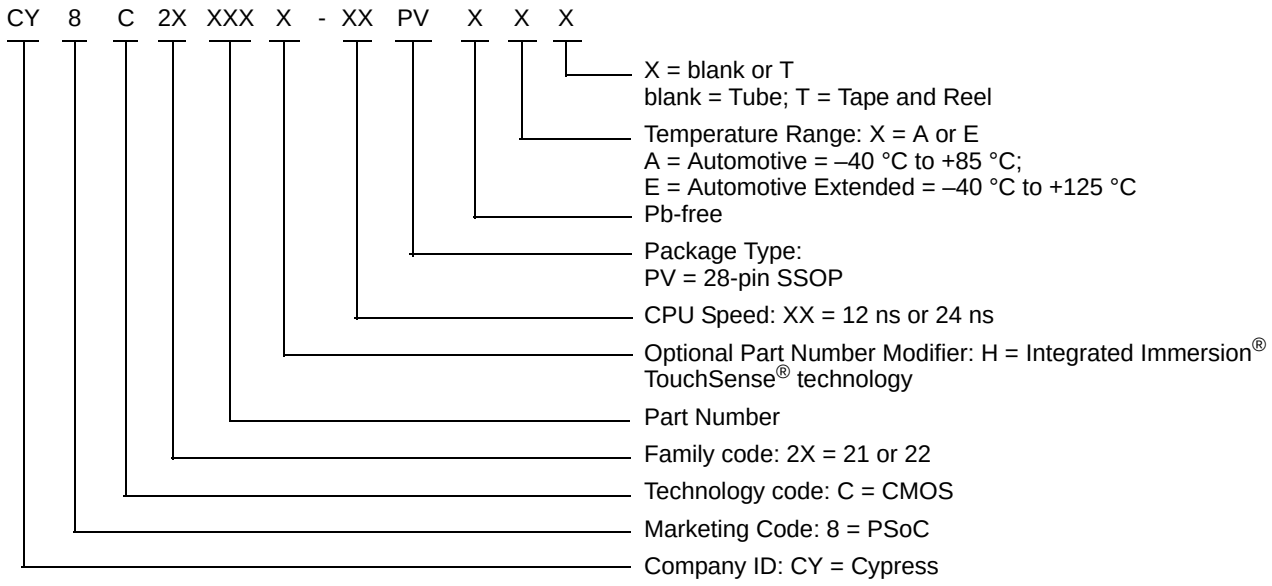
## Accessories (Emulation and Programming)

**Table 25. Emulation and Programming Accessories**

| Part Number | Pin Package | Pod Kit [19] | Foot Kit [20] | Prototyping Module | Adapter [21] |
|---|---|---|---|---|---|
| CY8C21345-24PVXA<br>CY8C21345-12PVXE<br>CY8C22345-24PVXA<br>CY8C22345H-24PVXA<br>CY8C22345-12PVXE | 28-pin SSOP | CY3250-22345 | CY3250-28SSOP-FK | – | AS-28-28-02SS-6ENP-GANG |
| CY8C21645-24PVXA<br>CY8C21645-12PVXE<br>CY8C22645-24PVXA<br>CY8C22645-12PVXE | 48-pin SSOP | – | – | – | AS-48-48-01SS-6-GANG |

**Notes**
19. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
20. Foot kit includes surface mount feet that can be soldered to the target PCB.
21. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

## Ordering Code Definitions



## Glossary (continued)

| | |
|---|---|
| block | 1. A functional unit that performs a single function, such as an oscillator.<br>2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block. |
| buffer | 1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written.<br>2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.<br>3. An amplifier used to lower the output impedance of a system. |
| bus | 1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.<br>2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].<br>3. One or more conductors that serve as a common connection for a group of related devices. |
| clock | The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks. |
| comparator | An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements. |
| compiler | A program that translates a high level language, such as C, into machine language. |
| configuration space | In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’. |
| crystal oscillator | An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components. |
| cyclic redundancy check (CRC) | A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression. |
| data bus | A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions. |
| debugger | A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory. |
| dead band | A period of time when neither of two or more signals are in their active state or in transition. |
| digital blocks | The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI. |
| digital-to-analog (DAC) | A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation. |
| duty cycle | The relationship of a clock period high time to its low time, expressed as a percent. |
| emulator | Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system. |

## Glossary (continued)

| | |
|---|---|
| external reset (XRES) | An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state. |
| flash | An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off. |
| Flash block | The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes. |
| frequency | The number of cycles or events per unit of time, for a periodic function. |
| gain | The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB. |
| $I^2C$ | A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode. |
| ICE | The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer). |
| input/output (I/O) | A device that introduces data into or extracts data from a system. |
| interrupt | A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed. |
| interrupt service routine (ISR) | A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution. |
| jitter | 1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams.<br>2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles. |
| low-voltage detect (LVD) | A circuit that senses $V_{DD}$ and provides an interrupt to the system when $V_{DD}$ falls below a selected threshold. |
| M8C | An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space. |
| master device | A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device***. |
| microcontroller | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal | The reference to a circuit containing both analog and digital techniques and components. |

## Glossary (continued)

| | |
|---|---|
| modulator | A device that imposes a signal on a carrier. |
| noise | 1. A disturbance that affects a signal and that may distort the information carried by the signal.<br>2. The random variations of one or more characteristics of any entity such as voltage, current, or data. |
| oscillator | A circuit that may be crystal controlled and is used to generate a clock frequency. |
| parity | A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity). |
| phase-locked loop (PLL) | An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal. |
| pinouts | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names. |
| port | A group of pins, usually eight. |
| power on reset (POR) | A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset. |
| PSoC® | Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress. |
| PSoC Designer™ | The software for Cypress' Programmable System-on-Chip technology. |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied measurand |
| RAM | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in. |
| register | A storage device with a specific capacity, such as a bit or byte. |
| reset | A means of bringing a system back to a know state. See hardware reset and software reset. |
| ROM | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in. |
| serial | 1. Pertaining to a process in which all events occur one after the other.<br>2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. |
| settling time | The time it takes for an output signal or value to stabilize after the input has changed from one value to another. |
| shift register | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data. |
| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |

# Errata

This section describes the errata for the CY8C21x45, CY8C22x45 family of PSoC devices. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

## Part Numbers Affected

| Part Number | Device Characteristics |
|---|---|
| CY8C21345 | All Variants |
| CY8C21645 | All Variants |
| CY8C22345 | All Variants |
| CY8C22645 | All Variants |

## CY8C21x45, CY8C22x45 Qualification Status

Product Status: In Production

## Errata Summary

The following table defines the errata applicable for this PSoC family device.

| Items | Part Number | Silicon Revision | Fix Status |
|---|---|---|---|
| 1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC | All CY8C21x45, CY8C22x45 devices affected | All | Silicon fix not planned. Use workaround. |
| 2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes | All CY8C21x45, CY8C22x45 devices affected | All | Silicon fix not planned. Use workaround. |

### 1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC

**■ Problem Definition**

In free running mode, there can be a variation of up to 7 LSB in the digital output of SAR10 ADC.

**■ Parameters Affected**

Code Variation. This is not a specified parameter.

It is defined as the number of unique output codes generated by the ADC for a given constant input voltage, in addition to the correct code. For example, for an input voltage of 2.000 V, the expected code is 190hex and the ADC generates three codes: 191hex, 190hex, and 192hex. The code variation is 2 LSB.

**■ Trigger Condition(S)**

SAR10 ADC is configured in the free running mode. When ADC is operated in free running mode, for a constant input voltage output of ADC can have a variation of up to 7LSB. This can be resolved by using the averaging technique or by disabling the free running mode before reading the data and enabling again after reading the data.

**■ Scope of Impact**

Inaccurate output is possible.

**■ Workaround**

This issue can be averted by using one or both of the following workarounds. Consult a Cypress representative for additional assistance.

- Use the averaging technique. That is, take multiple samples of the input, and use a digital averaging filter.
- Disable the free running mode before reading data out, and enable the free running mode after completing the read operation.

**■ Fix Status**

No silicon fix is planned.

### 2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

■ **Problem Definition**

Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

■ **Parameters Affected**

The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.

■ **Trigger Condiiton(S)**

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.

■ **Scope of Impact**

This problem may affect UART, IrDA, and FSK implementations.

■ **Workaround**

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

■ **Fix Status**

The cause of this problem and its solution has been identified. No silicon fix is planned to correct the deficiency in silicon.