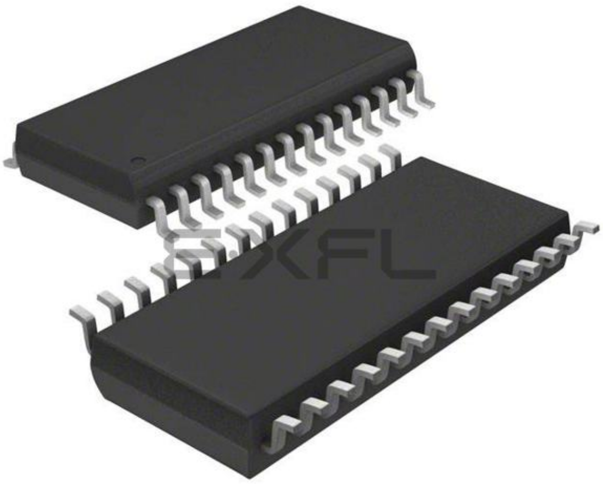


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c22345h-24pvxat

Contents

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC® device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Table 3. 48-pin Part Pinout (SSOP) (continued)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
43	I/O	I, MR	P2[6]	Direct input to analog block
44	I/O	I, MR	P0[0]	Analog column mux input
45	I/O	I, MR	P0[2]	Analog column mux input
46	I/O	I, MR	P0[4]	Analog column mux input
47	I/O	I, MR	P0[6]	Analog column mux input
48	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, O = Output, MR= Right analog mux bus input, ML= Left analog mux bus input

Registers

This section lists the registers of this PSoC device family by mapping tables. For detailed register information, refer to the PSoC Technical Reference Manual for CY8C21x45 and CY8C22x45 devices.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 4. Abbreviations

Convention	Description
RW	Read and write register or bit(s)
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
PRT4DM0	10	RW	CMP0CR1	50	RW		90		GDI_O_IN	D0	RW
PRT4DM1	11	RW	CMP0CR2	51	RW		91		GDI_E_IN	D1	RW
PRT4IC0	12	RW		52			92		GDI_O_OU	D2	RW
PRT4IC1	13	RW	VDAC50CR0	53	RW		93		GDI_E_OU	D3	RW
	14		CMP1CR1	54	RW		94			D4	
	15		CMP1CR2	55	RW		95			D5	
	16			56			96			D6	
	17		VDAC51CR0	57	RW		97			D7	
	18		CSCMPCR0	58	#		98		MUX_CR0	D8	RW
	19		CSCMPGOEN	59	RW		99		MUX_CR1	D9	RW
	1A		CSLUTCR0	5A	RW		9A		MUX_CR2	DA	RW
	1B		CMPCOLMUX	5B	RW		9B		MUX_CR3	DB	RW
	1C		CMPPWMCR	5C	RW		9C		DAC_CR1#	DC	RW
	1D		CMPFLTCR	5D	RW		9D		OSC_GO_EN	DD	RW
	1E		CMPCLK1	5E	RW		9E		OSC_CR4	DE	RW
	1F		CMPCLK0	5F	RW		9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	R
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	V2BG_TR	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	W
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	W
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DBC02CR1	2B	RW	CLK_CR3	6B	RW	SADC_CR3TRIM	AB	RW	ECO_TR	EB	W
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_AD	AD	RW		ED	
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DBC03CR1	2F	RW	TMP_DR3	6F	RW		AF			EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW		71		RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DBC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW	DAC_CR0#	FD	RW
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DBC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. **# Access is bit specific.**

DC SAR10 ADC Specifications

Table 13 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 13. DC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ADCREF}	Reference voltage at pin P2[5] when configured as ADC reference voltage	3.0	–	5.25	V	When V_{REF} is buffered inside ADC, the voltage level at P2[5] (when configured as ADC reference voltage) must be always maintained to be at least 300 mV less than the chip supply voltage level on V_{DD} pin. ($V_{ADCREF} < V_{DD}$)
I_{ADCREF}	Current into P2[5] when configured as ADC V_{REF}	–	–	100	µA	Disables the internal voltage reference buffer
INL_{ADC}	Integral nonlinearity A-grade devices E-grade devices	 –3.0 –5.0	 – –	 3.0 5.0	 LSbit LSbit	10-bit resolution
DNL_{ADC}	Differential nonlinearity A-grade devices E-grade devices	 –1.5 –4.0	 – –	 1.5 4.0	 LSbit LSbit	10-bit resolution

DC Analog Mux Bus Specifications

Table 14 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 14. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400	Ω	
R_{GND}	Resistance of initialization switch to GND	–	–	800	Ω	

DC Programming Specifications

Table 16 lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 85 °C, or 3.0 V to 3.6 V and –40 °C to 85 °C. Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and –40 °C to 125 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C, unless specified otherwise, and are for design guidance only.

Table 16. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify A-grade devices E-grade devices	 3.0 4.7	 3.1 4.8	 3.2 4.9	 V V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation A-grade devices E-grade devices	 3.0 4.75	 – –	 5.25 5.25	 V V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor
V_{OLV}	Output low voltage during programming or verify	–	–	0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block) [8, 9] A-grade devices E-grade devices	 1,000 100	 – –	 – –	 – –	Erase/write cycles per block
$Flash_{ENT}$	Flash endurance (total) [9, 10] CY8C21x45 A-grade devices CY8C22x45 A-grade devices CY8C21x45 E-grade devices CY8C22x45 E-grade devices	 128,000 256,000 12,800 25,600	 – – – –	 – – – –	 – – – –	Erase/write cycles
$Flash_{DR}$	Flash data retention [9] A-grade devices E-grade devices	 10 10	 – –	 – –	 Years Years	

Notes

8. The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
10. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.

Table 20. AC Digital Block Specifications (continued)

Function	Description	Min	Typ	Max	Units	Notes
Transmitter	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 Stop Bits	–	–	50.4 [15]	MHz	
	$V_{DD} \geq 4.75$ V, 1 Stop Bit	–	–	25.2 [15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	
Receiver	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 Stop Bits	–	–	50.4 [15]	MHz	
	$V_{DD} \geq 4.75$ V, 1 Stop Bit	–	–	25.2 [15]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2 [15]	MHz	

Note

15. Accuracy derived from IMO with appropriate trim for V_{DD} range.

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows the user to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240-V power supply, Euro-Plug adapter
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 25. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit [19]	Foot Kit [20]	Prototyping Module	Adapter [21]
CY8C21345-24PVXA CY8C21345-12PVXE CY8C22345-24PVXA CY8C22345H-24PVXA CY8C22345-12PVXE	28-pin SSOP	CY3250-22345	CY3250-28SSOP-FK	–	AS-28-28-02SS-6ENP-GANG
CY8C21645-24PVXA CY8C21645-12PVXE CY8C22645-24PVXA CY8C22645-12PVXE	48-pin SSOP	–	–	–	AS-48-48-01SS-6-GANG

Notes
19. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
20. Foot kit includes surface mount feet that can be soldered to the target PCB.
21. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

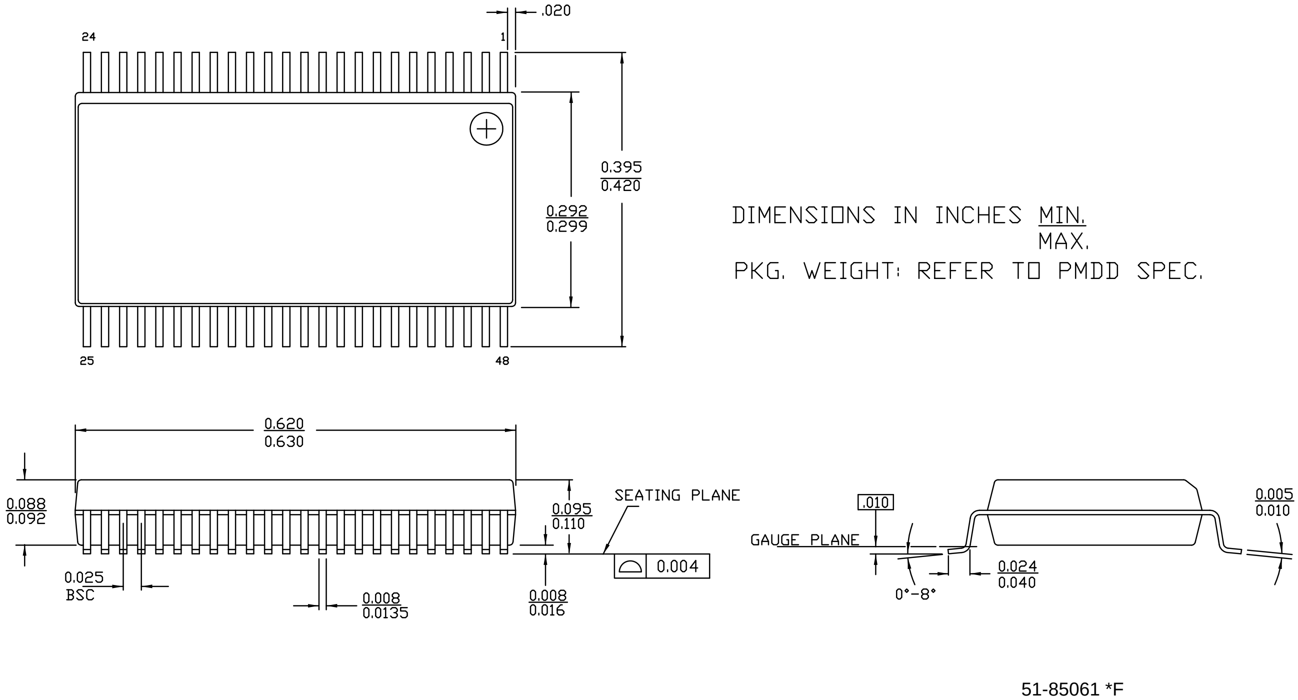
Ordering Code Definitions

CY 8 C 2X XXX X - XX PV X X X

- X = blank or T
  blank = Tube; T = Tape and Reel
- Temperature Range: X = A or E
  A = Automotive = –40 °C to +85 °C;
  E = Automotive Extended = –40 °C to +125 °C
- Pb-free
- Package Type:
  PV = 28-pin SSOP
- CPU Speed: XX = 12 ns or 24 ns
- Optional Part Number Modifier: H = Integrated Immersion® TouchSense® technology
- Part Number
- Family code: 2X = 21 or 22
- Technology code: C = CMOS
- Marketing Code: 8 = PSoC
- Company ID: CY = Cypress

Packaging Information (continued)

Figure 11. 48-pin SSOP (300 Mils) Package Outline, 51-85061



Thermal Impedances

Table 27. Thermal Impedances per Package

Package	Typical θ_{JA} [22]
28-pin SSOP	97.6 °C/W
48-pin SSOP	69 °C/W

Capacitance on Crystal Pins

Table 28. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28-pin SSOP	2.8 pF
48-pin SSOP	3.3 pF

Solder Reflow Specifications

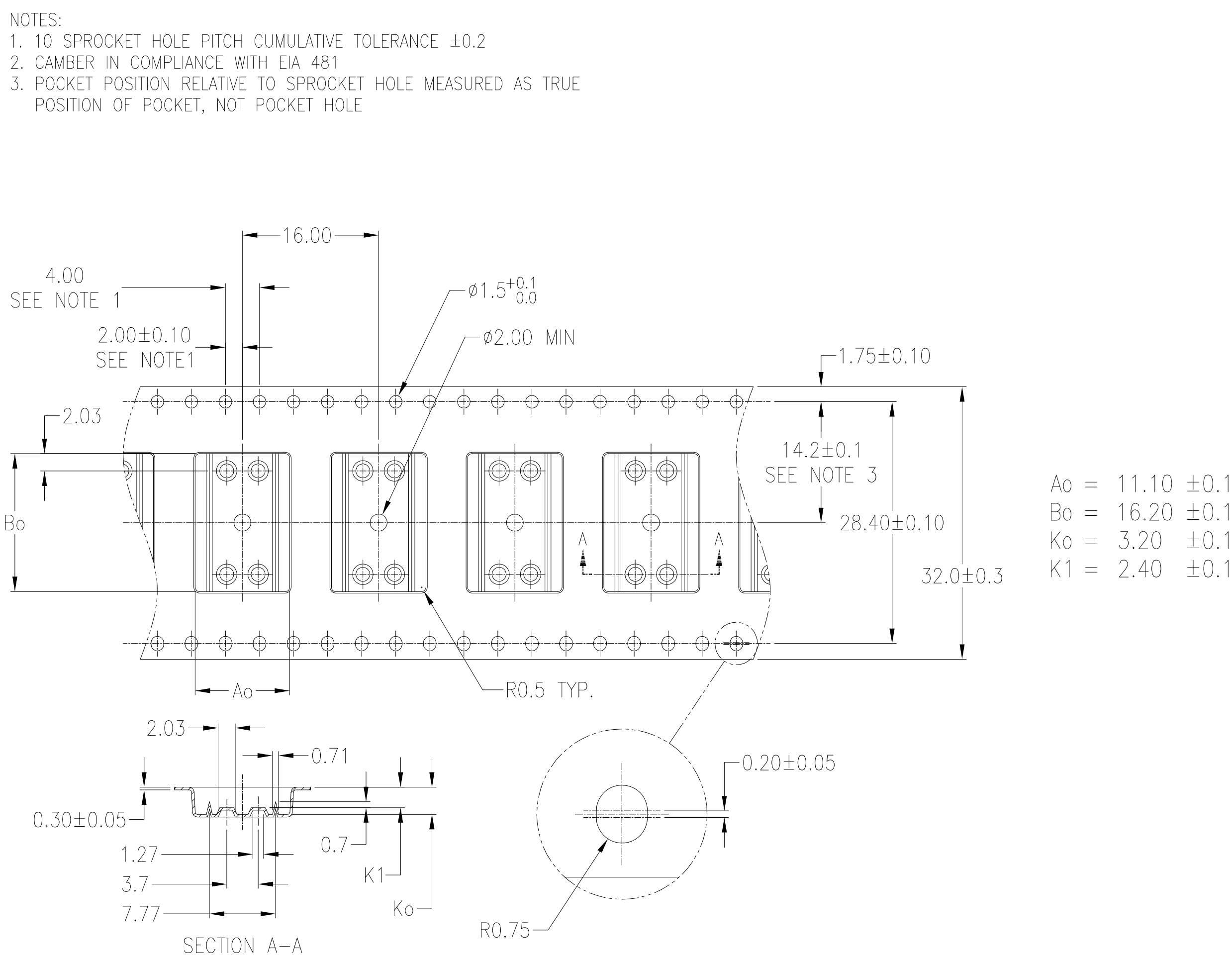
Table 29 shows the solder reflow temperature limits that must not be exceeded.

Table 29. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
28-pin SSOP	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds

Note
22. $T_J = T_A + POWER \times \theta_{JA}$

Figure 13. 48-pin SSOP (300 Mils) Carrier Tape, 51-51104



51-51104 *E

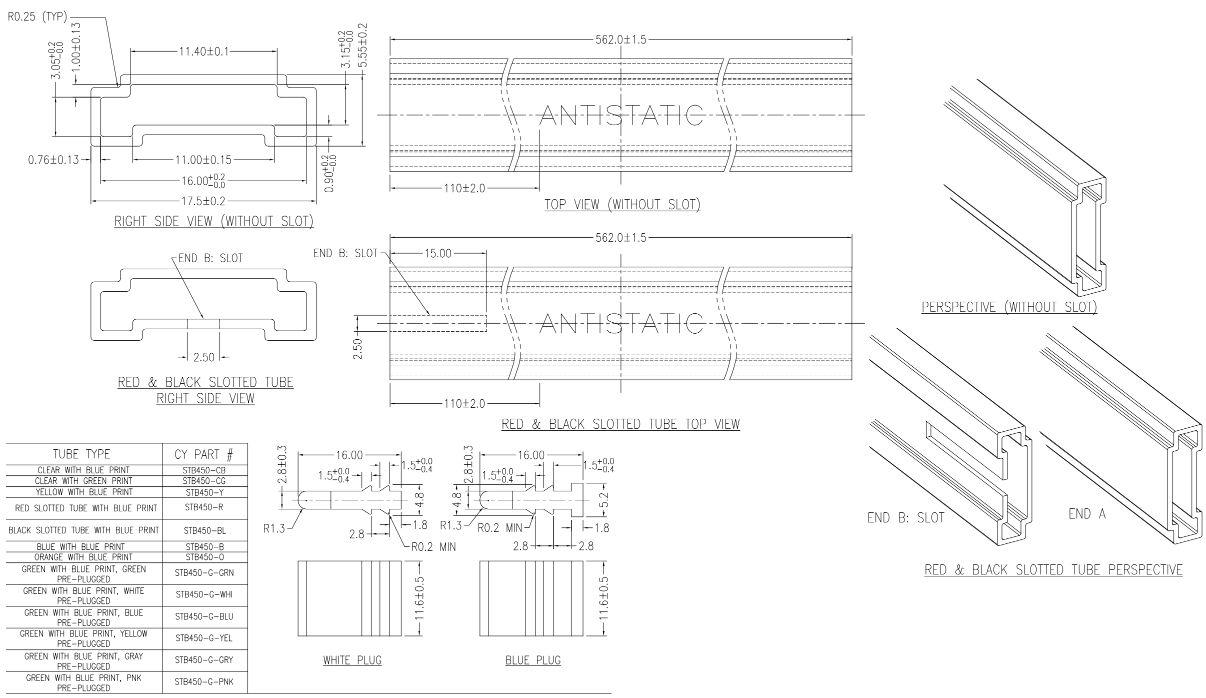
Table 30. Tape and Reel Specifications

Package	Cover Tape Width (mm)	Hub Size (inches)	Minimum Leading Empty Pockets	Minimum Trailing Empty Pockets	Standard Full Reel Quantity
28-pin SSOP	13.3	7	42	25	1000
48-pin SSOP	25.5	4	32	19	1000

Tube Information

Figure 14. 28-pin SSOP, 32-pin SOIC (450 Mils Body) Shipping Tube, 51-51029

NOTE:
1. MARK "ANTISTATIC" WITH 3.0mm HIGH AND 25.4±0.5mm LENGTH IN BLUE COLOR
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. TUBE MATERIAL : HARD PVC CLEAR.
4. PLUG MATERIAL : PPR 48
5. WHITE PLUG NEED COMPLETELY INSERT TO TUBE BEFORE SHIPPING AND THE TIP ALIGN WITH TUBE EDGE.
6. THE BLUE PLUG ENCLOSE TOGETHER WITH THE SHIPMENT.
7. 25 UNITS PER TUBE.
8. TUBE PART NUMBER WITH SLOT : STB450-R , STB450-BL



TUBE TYPE	CY PART #
CLEAR WITH BLUE PRINT	STB450-CB
CLEAR WITH GREEN PRINT	STB450-CG
YELLOW WITH BLUE PRINT	STB450-Y
RED SLOTTED TUBE WITH BLUE PRINT	STB450-R
BLACK SLOTTED TUBE WITH BLUE PRINT	STB450-BL
BLUE WITH BLUE PRINT	STB450-B
ORANGE WITH BLUE PRINT	STB450-O
GREEN WITH BLUE PRINT, GREEN PRE-PLUGGED	STB450-G-GRN
GREEN WITH BLUE PRINT, WHITE PRE-PLUGGED	STB450-G-WHI
GREEN WITH BLUE PRINT, BLUE PRE-PLUGGED	STB450-G-BLU
GREEN WITH BLUE PRINT, YELLOW PRE-PLUGGED	STB450-G-YEL
GREEN WITH BLUE PRINT, GRAY PRE-PLUGGED	STB450-G-GRY
GREEN WITH BLUE PRINT, PNK PRE-PLUGGED	STB450-G-PNK

51-51029 *E

Document Conventions

Units of Measure

Table 32 lists the units of measure that are used in this document.

Table 32. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	ms	millisecond
°C	degree Celsius	mV	millivolt
kHz	kilohertz	nA	nanoampere
kΩ	kilohm	ns	nanosecond
LSbit	least-significant bit	W	ohm
MHz	megahertz	%	percent
µA	microampere	pF	picofarad
µs	microsecond	ps	picosecond
µV	microvolt	pA	picoampere
mA	milliampere	V	volt
mm	millimeter	W	watt

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

Glossary (continued)

block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.

Glossary (continued)

modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.

Glossary (continued)

SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***Application Programming Interface (API)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Errata

This section describes the errata for the CY8C21x45, CY8C22x45 family of PSoC devices. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CY8C21345	All Variants
CY8C21645	All Variants
CY8C22345	All Variants
CY8C22645	All Variants

CY8C21x45, CY8C22x45 Qualification Status

Product Status: In Production

Errata Summary

The following table defines the errata applicable for this PSoC family device.

Items	Part Number	Silicon Revision	Fix Status
1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC	All CY8C21x45, CY8C22x45 devices affected	All	Silicon fix not planned. Use workaround.
2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	All CY8C21x45, CY8C22x45 devices affected	All	Silicon fix not planned. Use workaround.

1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC

■ **Problem Definition**

In free running mode, there can be a variation of up to 7 LSB in the digital output of SAR10 ADC.

■ **Parameters Affected**

Code Variation. This is not a specified parameter.

It is defined as the number of unique output codes generated by the ADC for a given constant input voltage, in addition to the correct code. For example, for an input voltage of 2.000 V, the expected code is 190hex and the ADC generates three codes: 191hex, 190hex, and 192hex. The code variation is 2 LSB.

■ **Trigger Condition(S)**

SAR10 ADC is configured in the free running mode. When ADC is operated in free running mode, for a constant input voltage output of ADC can have a variation of up to 7LSB. This can be resolved by using the averaging technique or by disabling the free running mode before reading the data and enabling again after reading the data.

■ **Scope of Impact**

Inaccurate output is possible.

■ **Workaround**

This issue can be averted by using one or both of the following workarounds. Consult a Cypress representative for additional assistance.

- Use the averaging technique. That is, take multiple samples of the input, and use a digital averaging filter.
- Disable the free running mode before reading data out, and enable the free running mode after completing the read operation.

■ **Fix Status**

No silicon fix is planned.

2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

- **Problem Definition**

  Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

- **Parameters Affected**

  The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.

- **Trigger Condiiton(S)**

  The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.

- **Scope of Impact**

  This problem may affect UART, IrDA, and FSK implementations.

- **Workaround**

  Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

- **Fix Status**

  The cause of this problem and its solution has been identified. No silicon fix is planned to correct the deficiency in silicon.

Document History Page

Document Title: CY8C21345/CY8C21645/CY8C22345/CY8C22345H/CY8C22645, Automotive PSoC® Programmable System-on-Chip™ Document Number: 001-55397				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2759868	VIVG	09/04/09	New data sheet.
*A	2788690	VIVG	10/20/09	Added 48 SSOP to the marketing part numbers. Corrected the I_{SOA} spec in table 13/14. Changed the ThetaJA values based on PE inputs.
*B	2792800	VIVG	10/26/09	Corrected typo in ordering information table (Digital I/O for 48-SSOP devices)
*C	2822630	BTK	12/07/09	Added CY8C22345H devices and updated Features section and PSoC Functional Overview section to include haptics device information. Updated Features section. Added Contents section. Updated PSoC Functional Overview section. Updated Block Diagram of device. Updated PSoC Device Characteristics table. Updated Pinouts section. Fixed issues with the Register Map tables. Added a figure for SLIMO configuration. Updated footnotes for the DC Programming Specifications table. Corrected $V_{DDIWRITE}$ and $Flash_{ENT}$ electrical specifications. Updated Ordering Information section. Added Development Tool Selection section. Combined 5 V DC Operational Amplifier Specifications table with 3.3 V DC Operational Amplifier Specifications table. Updated all AC specifications to conform to 5% IMO accuracy and 8.33% SLIMO accuracy. Split up electrical specifications for A-grade and E-grade devices in the Absolute Maximum Ratings, Operating Temperature, DC Chip Level Specifications, DC Programming Specifications, and AC Chip-Level Specifications tables. Added Solder Reflow Peak Temperature table. Added T_{PRGH}, T_{PRGC}, I_{OL}, I_{OH}, F_{32KU}, DC_{ILO}, and $T_{POWERUP}$ electrical specifications. Added maximum values and updated typical values for T_{ERASEB} and T_{WRITE} electrical specifications. Replaced T_{RAMP} electrical specification with $SR_{POWERUP}$ electrical specification.
*D	2905459	NJF	04/06/10	Updated Cypress website links Added $T_{BAKETEMP}$, $T_{BAKETIME}$, and Fout48M electrical specifications Removed sections 'Third Party Tools' 'Build a PSoC Emulator into your Board' Updated package diagrams Updated Ordering Information table Updated Solder Reflow Peak Temperature specifications. Updated the Getting Started and Designing with PSoC Designer sections. Converted data sheet from Preliminary to Final Deleted 5% oscillator accuracy reference in the Features section. Deleted reference to a specific SAR10 ADC sample rate in the Analog System section. Updated the following Electrical Specifications: I_{DD}, I_{SB}, I_{SBXTL}, V_{REF}, V_{CMOA}, I_{ADCREF}, INL_{ADC}, DNL_{ADC}, V_{PPOR2}, $Flash_{DR}$, F_{IMO24}, T_{RiseF}, T_{FallF}, T_{RiseS}, T_{FallS}. Deleted the SPS_{ADC} electrical specification, the DC Low Power Comparator Specifications, the AC Low Power Comparator Specifications, and the AC Analog Mux Bus Specifications.
*E	2915673	VIVG	04/16/10	Post to external web
*F	2991841	BTK	07/23/10	Added a clarifying note to the V_{PPOR1} electrical specification. Added CY8C22345-12PVXE(T) devices. Moved Document Conventions to the end of the document.
*G	3037161	BTK	09/23/10	Added CY8C21345-12PVXE(T) devices to the Ordering Information section.
*H	3085024	BTK	11/12/10	Added CY8C21645-12PVXE(T), CY8C21645-24PVXA(T), CY8C22645-12PVXE(T), and CY8C22645-24PVXA(T) devices to the Ordering Information section.
*I	3200275	BTK	03/18/11	Added tape and reel packaging information.

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