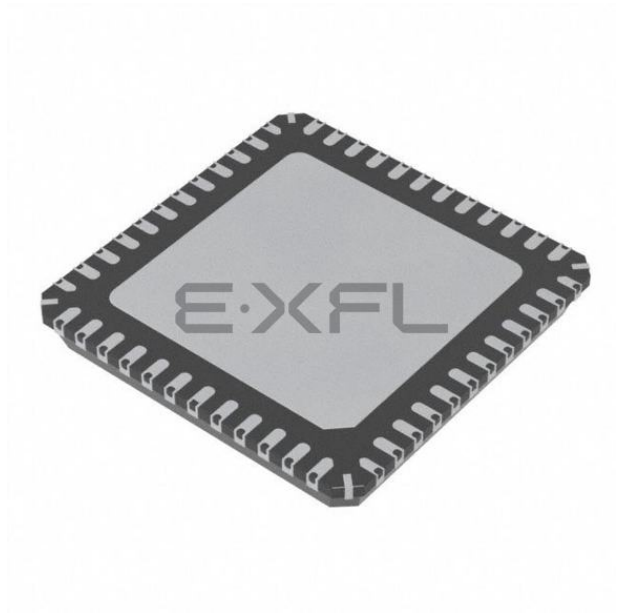

Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (64kB)
Controller Series	-
RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9877qxa40xuma1

- Overtemperature protection
- Short circuit protection
- Loss of clock detection with fail safe mode entry for low system power consumption
- Temperature Range T_j = -40 °C to +150 °C
- Package VQFN-48 with LTI feature
- Green package (RoHS compliant)
- AEC qualified

3.2 Pin Configuration

After reset, all pins are configured as input (except supply and LIN pins) with one of the following settings:

- Pull-up device enabled only (PU)
- Pull-down device enabled only (PD)
- Input with both pull-up and pull-down devices disabled (I)
- Output with output stage deactivated = high impedance state (Hi-Z)

The functions and default states of the TLE9877QXA40 external pins are provided in the following table.

Type: indicates the pin type.

- I/O: Input or output
- I: Input only
- O: Output only
- P: Power supply

Not all alternate functions listed.

Table 2 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State[1)]	Function	
P0				**Port 0** Port 0 is a 5-bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the port description. Main function is listed below.	
P0.0	21	I/O	I/PU	SWD	Serial Wire Debug Clock
P0.1	23	I/O	I/PU	GPIO	General Purpose IO Alternate function mapping see **Table 8**
P0.2	25	I/O	I/PD	GPIO	General Purpose IO Alternate function mapping see **Table 8** *Note: For a functional SWD connection this GPIO must be tied to zero!*
P0.3	24	I/O	I/PU	GPIO	General Purpose IO Alternate function mapping see **Table 8**
P0.4	18	I/O	I/PD	GPIO	General Purpose IO Alternate function mapping see **Table 8**
P1				**Port 1** Port 1 is a 5-bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the Port description. The principal functions are listed below.	
P1.0	15	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**
P1.1	16	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**
P1.2	17	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**
P1.3	26	I/O	I	GPIO	General Purpose IO, used for Inrush Transistor Alternate function mapping see **Table 9**
P1.4	27	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**

1) May not be switched off due to safety reasons
2) MC PLL clock disabled, MC supply reduced to 1.1 V

Wake-Up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for the monitor input, by LIN or by cyclic wake-up.

14 GPIO Ports and Peripheral I/O

The TLE9877QXA40 has 15 port pins organized into three parallel ports: Port 0 (P0), Port 1 (P1) and Port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. P0 and P1 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. On Port 2 (P2) analog inputs are shared with general purpose input.

14.1 Features

Bidirectional Port Features (P0, P1)

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

Analog Port Features (P2)

- Configurable pull-up/pull-down devices
- Transfer of data through digital inputs
- Alternate inputs for on-chip peripherals

14.2 Introduction

14.2.1 Port 0 and Port 1

Figure 17 shows the block diagram of an TLE9877QXA40 bidirectional port pin. Each port pin is equipped with a number of control and data bits, thus enabling very flexible usage of the pin. By defining the contents of the control register, each individual pin can be configured as an input or an output. The user can also configure each pin as an open drain pin with or without internal pull-up/pull-down device.

Each bidirectional port pin can be configured for input or output operation. Switching between input and output mode is accomplished through the register Px_DIR (x = 0 or 1), which enables or disables the output and input drivers. A port pin can only be configured as either input or output mode at any one time.

In input mode (default after reset), the output driver is switched off (high-impedance). The voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt trigger device and can be read via the register Px_DATA.

In output mode, the output driver is activated and drives the value supplied through the multiplexer to the port pin. In the output driver, each port line can be switched to open drain mode or normal mode (push-pull mode) via the register Px_OD.

The output multiplexer in front of the output driver enables the port output function to be used for different purposes. If the pin is used for general purpose output, the multiplexer is switched by software to the data register Px_DATA. Software can set or clear the bit in Px_DATA and therefore directly influence the state of the port pin. If an on-chip peripheral uses the pin for output signals, alternate output lines (AltDataOut) can be switched via the multiplexer to the output driver circuitry. Selection of the alternate output function is defined in registers Px_ALTSEL0 and Px_ALTSEL1. When a port pin is used as an alternate function, its direction must be set accordingly in the register Px_DIR.

14.3 TLE9877QXA40 Port Module

14.3.1 Port 0

14.3.1.1 Port 0 Functions

Table 8 Port 0 Input/Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.0	Input	GPI	P0_DATA.P0	
		INP1	SWCLK / TCK_0	SW
		INP2	T12HR_0	CCU6
		INP3	T4INA	GPT12T4
		INP4	T2_0	Timer 2
		INP5	–	–
		INP6	EXINT2_3	SCU
	Output	GPO	P0_DATA.P0	
		ALT1	T3OUT	GPT12T3
		ALT2	EXF21_0	Timer 21
		ALT3	RXDO_2	UART2
P0.1	Input	GPI	P0_DATA.P1	
		INP2	T13HR_0	CCU6
		INP3	TxD1	LIN_TxD
		INP4	CAPINA	GPT12CAP
		INP5	T21_0	Timer 21
		INP6	T4INC	GPT12T4
		INP7	MRST_1_2	SSC1
		INP8	EXINT0_2	SCU
	Output	GPO	P0_DATA.P1	
		ALT1	TxD1	UART1 / LIN_TxD
		ALT2	–	–
		ALT3	T6OUT	GPT12T6

14.3.2 Port 1

14.3.2.1 Port 1 Functions

Table 9 Port 1 Input / Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.0	Input	GPI	P1_DATA.P0	
		INP1	T3INC	GPT12T3
		INP2	T4EUDB	GPT12T4
		INP3	CC61_0	CCU6
		INP4	SCK_2	SSC2
		INP5	EXINT1_2	SCU
	Output	GPO	P1_DATA.P0	
		ALT1	SCK_2	SSC2
		ALT2	CC61_0	CCU6
		ALT3	EXF21_3	Timer 21
P1.1	Input	GPI	P1_DATA.P1	
		INP1	–	–
		INP2	T6EUDA	GPT12T6
		INP3	–	-
		INP4	MTSR_2	SSC2
		INP5	T21_1	Timer 21
		INP6	EXINT1_0	SCU
	Output	GPO	P1_DATA.P1	–
		ALT1	MTSR_2	SSC2
		ALT2	COUT61_0	CCU6
		ALT3	TXD2_0	UART2
P1.2	Input	GPI	P1_DATA.P2	
		INP1	T2INA	GPT12T2
		INP2	T2EX_1	Timer 2
		INP3	T21EX_3	Timer 21
		INP4	MRST_2_0	SSC2
		INP5	RXD2_0	UART2
		INP6	CCPOS2_2	CCU6
		INP7	EXINT0_1	SCU
	Output	GPO	P1_DATA.P2	
		ALT1	MRST_2_0	SSC2
		ALT2	COUT63_0	CCU6
		ALT3	T3OUT	GPT12T3

16 Timer2 and Timer21

16.1 Features

- 16-bit auto-reload mode
  - selectable up or down counting
- One channel 16-bit capture mode

16.2 Introduction

The timer modules are general-purpose 16-bit timers. Timer 2/21 can function as a timer or counter in each of its modes. As a timer, it counts with an input clock of $f_{PCLK}/12$ (if prescaler is disabled). As a counter, Timer 2 counts 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is $f_{PCLK}/24$ (if prescaler is disabled).

16.2.1 Timer2 and Timer21 Modes Overview

Table 11 Timer2 and Timer21 Modes

Mode	Description
Auto-reload	**Up/Down Count Disabled** • Count up only • Start counting from 16-bit reload value, overflow at $FFFF_H$ • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well • Programmable reload value in register RC2 • Interrupt is generated with reload events.
Auto-reload	**Up/Down Count Enabled** • Count up or down, direction determined by level at input pin T2EX • No interrupt is generated • Count up – Start counting from 16-bit reload value, overflow at $FFFF_H$ – Reload event triggered by overflow condition – Programmable reload value in register RC2 • Count down – Start counting from $FFFF_H$, underflow at value defined in register RC2 – Reload event triggered by underflow condition – Reload value fixed at $FFFF_H$
Channel capture	• Count up only • Start counting from 0000_H, overflow at $FFFF_H$ • Reload event triggered by overflow condition • Reload value fixed at 0000_H • Capture event triggered by falling/rising edge at pin T2EX • Captured timer value stored in register RC2 • Interrupt is generated by reload or capture events

Note: The capture/compare module itself is referred to as CCU6 (capture/compare unit 6). A capture/compare channel inside this module is referred to as CC6x.

The timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel works in compare mode, whereas another channel works in capture mode). The timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

18.2.1 Block Diagram

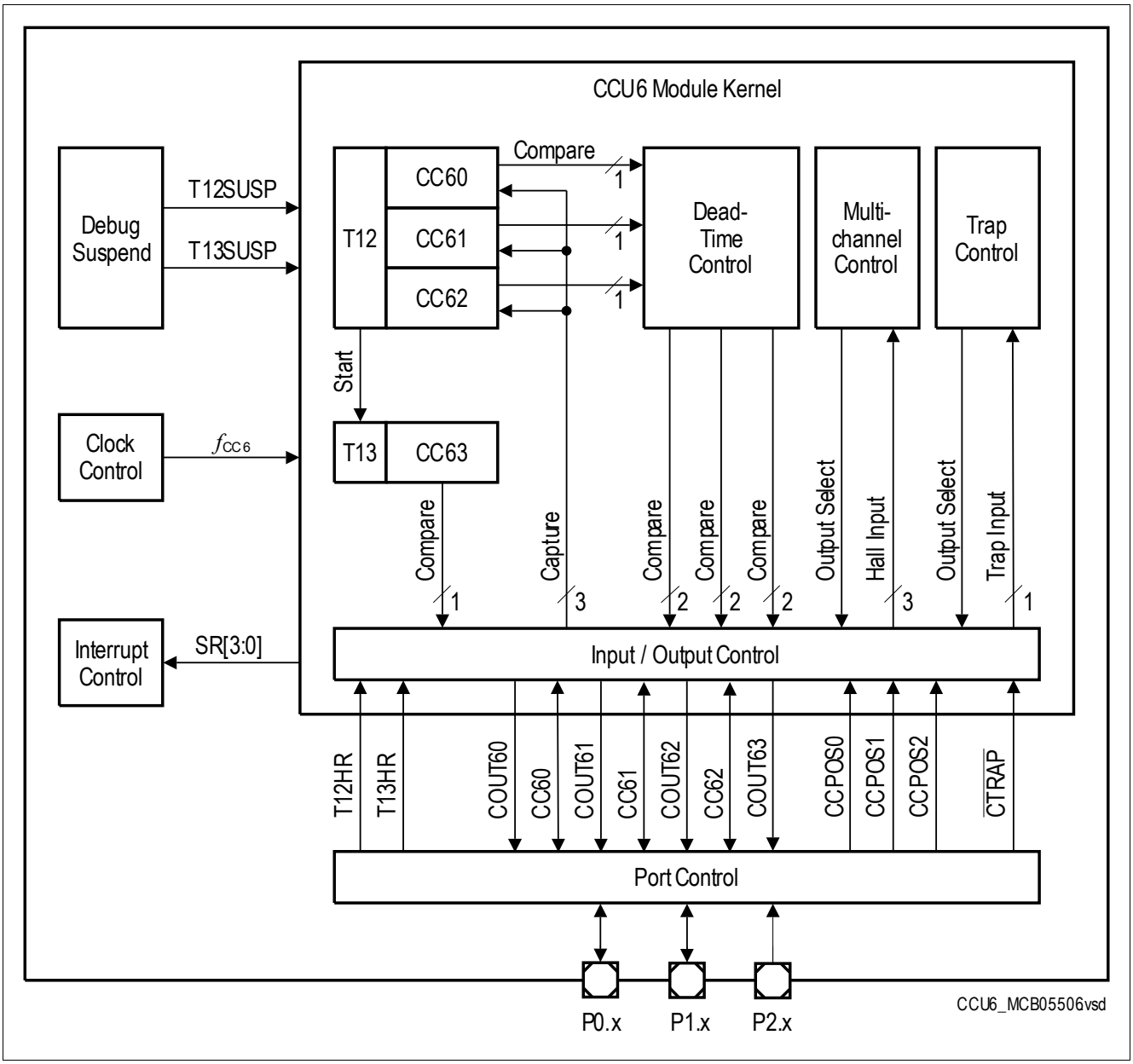

Figure 21 CCU6 Block Diagram

19 UART1/UART2

19.1 Features

- Full-duplex asynchronous modes
  - 8-bit or 9-bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates
- Hardware logic for break and synch byte detection

19.2 Introduction

The UART provides a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. It is also receive-buffered, i.e., it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

19.2.1 Block Diagram

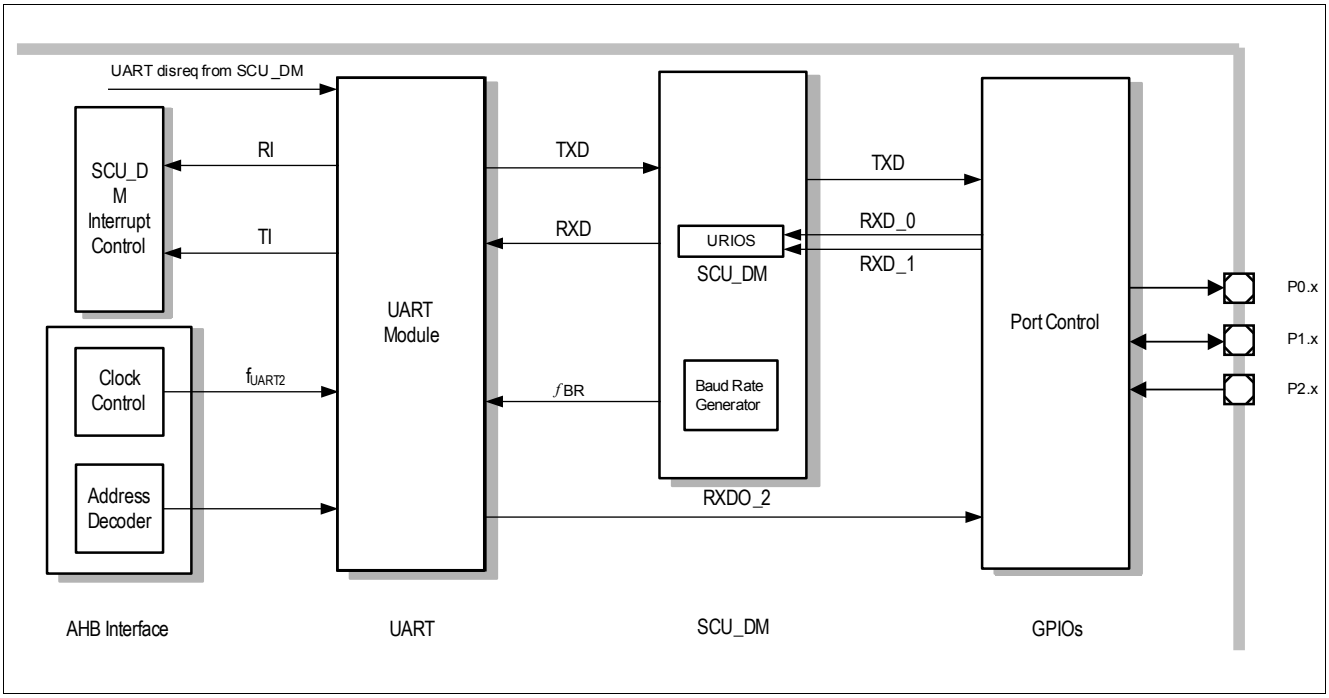

Figure 22 UART Block Diagram

24 10-Bit Analog Digital Converter (ADC1)

24.1 Features

The principal features of the ADC1 are:

- Up to 8 analog input channels (channel 7 reserved for future use)
- Flexible results handling
  - 8-bit and 10-bit resolution
- Flexible source selection due to sequencer
  - insert one exceptional sequence (ESM)
  - insert one interrupt measurement into the current sequence (EIM), single or up to 128 times
  - software mode
- Conversion sample time (separate for each channel) adjustable to adapt to sensors and reference
- Standard external reference (VAREF) to support ratiometric measurements and different signal scales
- DMA support, transfer ADC conversion results via DMA into RAM
- Support of suspend and power saving modes
- Result data protection for slow CPU access (wait-for-read mode)
- Programmable clock divider
- Integrated sample and hold circuitry

24.2 Introduction

The TLE9877QXA40 includes a high-performance 10-bit Analog-to-Digital Converter (ADC1) with eight multiplexed analog input channels. The ADC1 uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC1 are available at AN0, AN2 - AN5.

27 Current Sense Amplifier

27.1 Features

Main Features

- Programmable gain settings: G = 10, 20, 40, 60
- Differential input voltage: ± 1.5V / G
- Wide common mode input range ± 2 V
- Low setting time < 1.4 µs

27.2 Introduction

The current sense amplifier in **Figure 31** can be used to measure near ground differential voltages via the 10-bit ADC. Its gain is digitally programmable through internal control registers.

Linear calibration has to be applied to achieve high gain accuracy, e.g. end-of-line calibration including the shunt resistor.

Figure 31 shows how the current sense amplifier can be used as a low-side current sense amplifier where the motor current is converted to a voltage by means of a shunt resistor R_{SH}. A differential amplifier input is used in order to eliminate measurement errors due to voltage drop across the stray resistance R_{Stray} and differences between the external and internal ground. If the voltage at one or both inputs is out of the operating range, the input circuit is overloaded and requires a certain specified **recovery time**.

In general, the external low pass filter should provide suppression of EMI.

27.2.1 Block Diagram

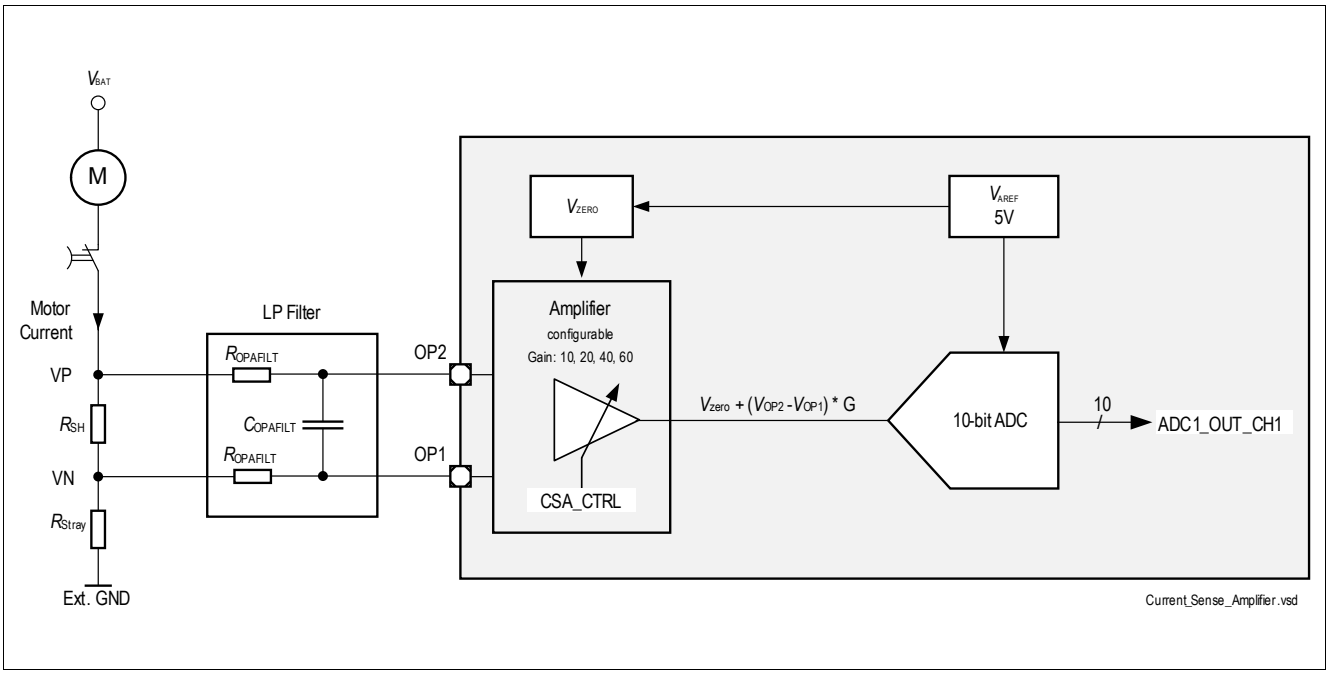

Figure 31 Simplified Application Diagram

28 Application Information

28.1 BLDC Driver

Figure 32 shows the TLE9877QXA40 in an electric drive application setup controlling a BLDC motor.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

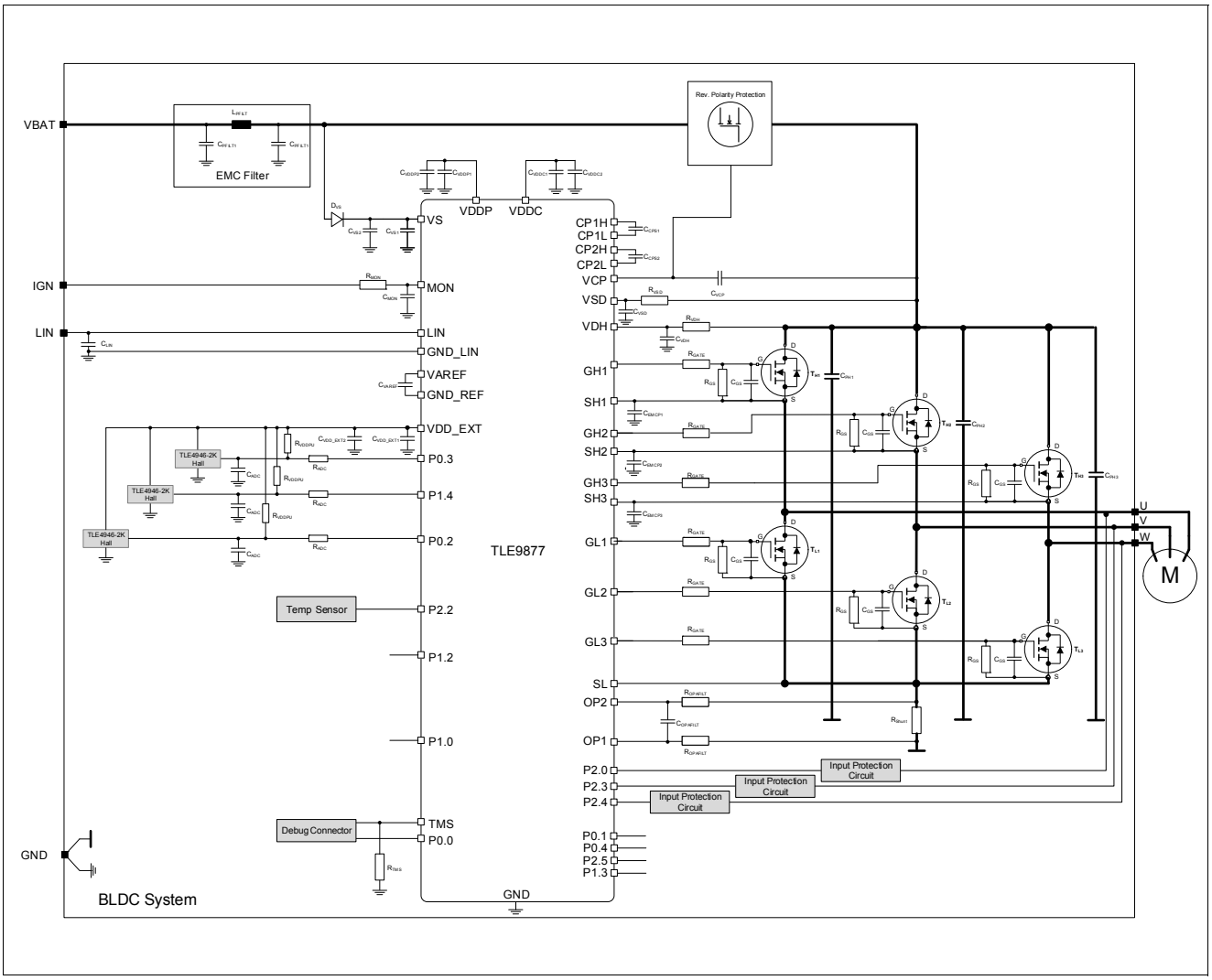

Figure 32 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of materials. The function must be verified in the actual application.

Table 22 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Overcurrent diagnostic filter time	t_{FILT_VDDPOC}	–	27	–	µs	3)7)	P_2.1.27
Overcurrent diagnostic shutdown time	$t_{FILT\_VDDPOC\_SD}$	–	290	–	µs	3)7)9)	P_2.1.28

1) Specified output current for port supply and additional other external loads already excluding VDDC current.
2) This use case applies to cases where output current on VDDEXT is max. 40 mA.
3) Not subject to production test, specified by design.
4) Ceramic capacitor.
5) Load current includes internal supply.
6) Output drop for IVDDP without internal supply current.
7) This filter time and its variation is derived from the time base $t_{LP\_CLK} = 1 / f_{LP\_CLK}$.
8) The absolute voltage value is the sum of parameters $V_{DDP} + \Delta V_{DDPSTB}$.
9) After $t_{FILT\_VDDCOC\_SD}$ is passed and the overcurrent condition is still present, the device will enter sleep mode.

5) The absolute voltage value is the sum of parameters V_{DDEXT} + $\Delta V_{DDEXTSTB}$.
6) When the condition is met, the Bit VDDEXT_CTRL.bit.SHORT will be set.

Table 32 DC Characteristics Port 2 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Pull level force current	I_{PLF}	-750	–	+750	µA	3) $V_{PIN} \le V_{IL}$ (up) $V_{PIN} \ge V_{IH}$ (dn)	P_5.2.6
Pin capacitance (digital inputs/outputs)	C_{IO}	–	–	10	pF	2)	P_5.2.7

1) Tested at V_{DDP} = 5V, specified for 4.5V < V_{DDP} < 5.5V.

2) Not subject to production test, specified by design.

3) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \ge V_{IH}$ for a pull-up; $V_{PIN} \le V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \le V_{IL}$ for a pull-up; $V_{PIN} \ge V_{IH}$ for a pull-down.

Table 33 Electrical Characteristics LIN Transceiver (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	–	P_6.1.32
Receiver delay symmetry	$t_{sym,R}$	-1.0	–	1.5	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$;	P_6.1.33
Duty cycle D7 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry	t_{duty1}	0.399	–	–		5) duty cycle D7 THRec(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 13.5 V; t_{bit} = 8.7 µs; D7 = $t_{bus\_rec(min)}$/2 t_{bit};	P_6.1.34
Duty cycle D8 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry	t_{duty2}	–	–	0.578		5) duty cycle 8 TH_{Rec}(min) = 0.422 × V_S; TH_{Dom}(min) = 0.284 × V_S;V_S = 13.5 V; t_{bit} = 8.7 µs; D8 = $t_{bus\_rec(max)}$/2 t_{bit};	P_6.1.35
LIN input capacity	C_{LIN_IN}	–	15	30	pF	6)	P_6.1.69
TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V	P_6.1.36
Thermal Shutdown (Junction Temperature)							
Thermal shutdown temp.	T_{jSD}	190	200	215	°C	6)	P_6.1.65
Thermal shutdown hyst.	ΔT	–	10	–	K	6)	P_6.1.66

1) Maximum limit specified by design.
2) $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\ rec})/2$
3) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$
4) Bus load concerning LIN Spec 2.2:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
5) Bus load
   Load 1 = 1 nF / 500 Ω = C_{BUS} / R_{BUS}
6) Not subject to production test, specified by design.

29.8 Measurement Unit

29.8.1 System Voltage Measurement Parameters

Table 35 Supply Voltage Signal Conditioning

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Measurement output voltage range @ VAREF5	V_{A5}	0	–	5	V	–	P_8.1.15
Measurement output voltage range @ VAREF1V2	V_{A1V2}	0	–	1.23	V	–	P_8.1.16
Battery / Supply Voltage Measurement							
Input to output voltage attenuation: V_S	ATT_{VS_1}	–	0.055	–		SFR setting 1	P_8.1.41
Nominal operating input voltage range V_S	$V_{S,range1}$	3	–	22	V	1)SFR setting 1; Max. value corresponds to typ. ADC full scale input; 3V < V_S < 28V	P_8.1.1
Accuracy of V_S after calibration	$V_{S,range1}$	-220	–	220	mV	SFR setting 1, V_S = 5.5 V to 18V	P_8.1.70
Input to output voltage attenuation: V_S	ATT_{VS_2}	–	0.039	–		SFR setting 2	P_8.1.42
Nominal operating input voltage range V_S	$V_{S,range2}$	3	–	31	V	1)SFR setting 2; Max. value corresponds to typ. ADC full scale input 3V < V_S < 28V	P_8.1.40
Accuracy of V_S after calibration	$V_{S,range2}$	-370	–	370	mV	SFR setting 2, V_S = 5.5V to 18V	P_8.1.44
Driver Supply Voltage Measurement V_{SD}							
Input to output voltage attenuation: V_{SD}	ATT_{VSD}	–	0.039	–		–	P_8.1.21
Nominal operating input voltage range V_{SD}	$V_{SD,range}$	2.5	–	31	V	1)	P_8.1.2
Accuracy of V_{SD} sense after calibration	ΔV_{SD}	-440	–	440	mV	V_S = 5.5V to 18V	P_8.1.47

29.9 ADC1 Reference Voltage - VAREF

29.9.1 Electrical Characteristics VAREF

Table 39 Electrical Characteristics VAREF

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Required buffer capacitance	C_{VAREF}	0.1	–	1	µF	ESR < 1Ω	P_9.1.1
Reference output voltage	V_{AREF}	4.95	5	5.05	V	V_S > 5.5V	P_9.1.2
DC supply voltage rejection	$DC_{PSRVAREF}$	30	–	–	dB	1) –	P_9.1.3
Supply voltage ripple rejection	$AC_{PSRVAREF}$	26	–	–	dB	1) V_S = 13.5V; f = 0 ... 1KHz; V_r = 2Vpp	P_9.1.4
Turn ON time	t_{so}	–	–	200	µs	1) C_{ext} = 100nF PD_N to 99.9% of final value	P_9.1.5
Input resistance at VAREF Pin	$R_{IN,VAREF}$	–	100	–	kΩ	1)input impedance in case of VAREF is applied from external	P_9.1.20

1) Not subject to production test, specified by design.