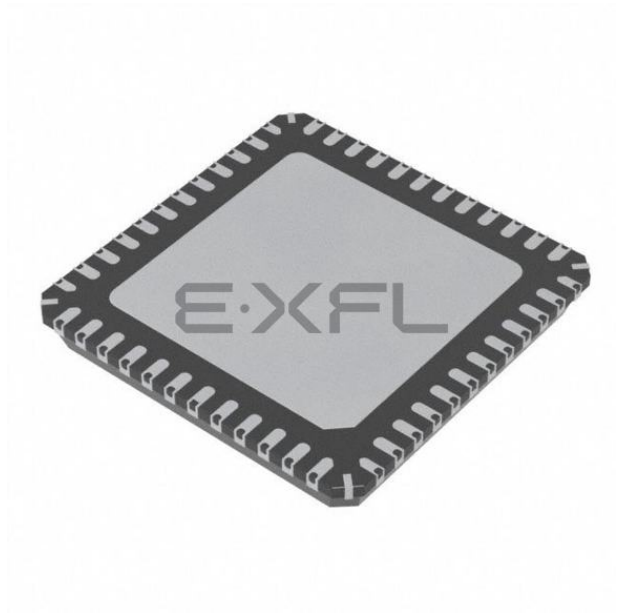

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RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
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1.1 Abbreviations

The following acronyms and terms are used within this document. List see in Table 1.

Table 1 Acronyms

Acronyms	Name
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
CCU6	Capture Compare Unit 6
CGU	Clock Generation Unit
CMU	Cyclic Management Unit
CP	Charge Pump for MOSFET driver
CSA	Current Sense Amplifier
DPP	Data Post Processing
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
EIM	Exceptional Interrupt Measurement
FSM	Finite State Machine
GPIO	General Purpose Input Output
H-Bridge	Half Bridge
ICU	Interrupt Control Unit
IEN	Interrupt Enable
IIR	Infinite Impulse Response
LDM	Load Instruction
LDO	Low DropOut voltage regulator
LIN	Local Interconnect Network
LSB	Least Significant Bit
LTI	Lead Tip Inspection
MCU	Memory Control Unit
MF	Measurement Functions
MSB	Most Significant Bit
MPU	Memory Protection Unit
MRST	Master Receive Slave Transmit
MTSR	Master Transmit Slave Receive
MU	Measurement Unit
NMI	Non Maskable Interrupt
NVIC	Nested Vector Interrupt Controller
NVM	Non-Volatile Memory
OTP	One Time Programmable
OSC	Oscillator
PBA	Peripheral Bridge

3 Device Pinout and Pin Configuration

3.1 Device Pinout

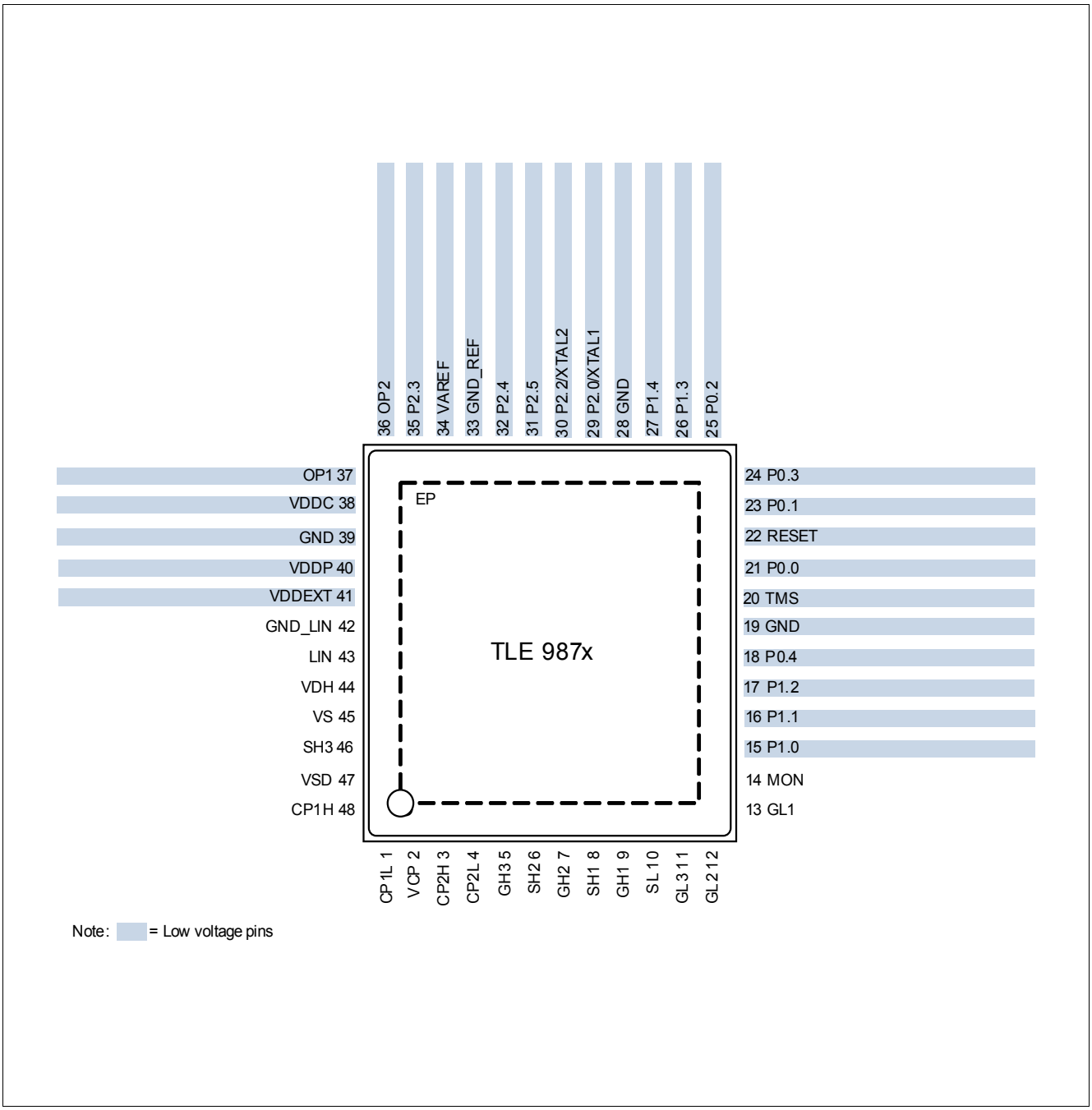

Figure 2 Device Pinout, TLE9877QXA40

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State[1)]	Function
P2				**Port 2** Port 2 is a 5-bit general purpose input-only port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below.
P2.0/XTAL1	29	I/I	I	AN0 ADC analog input 0 Alternate function mapping see **Table 10**
P2.2/XTAL2	30	I/O	I	AN2 ADC analog input 2 Alternate function mapping see **Table 10**
P2.3	35	I	I	AN3 ADC analog input 3 Alternate function mapping see **Table 10**
P2.4	32	I	I	AN4 ADC analog input 4 Alternate function mapping see **Table 10**
P2.5	31	I	I	AN5 ADC analog input 5 Alternate function mapping see **Table 10**
Power Supply				
VS	45	P	–	Battery supply input
VDDP	40	P	–	[2)]I/O port supply (5.0 V). Connect external buffer capacitor.
VDDC	38	P	–	[3)]Core supply (1.5 V during Active Mode). Do not connect external loads, connect external buffer capacitor.
VDDEXT	41	P	–	External voltage supply output (5.0 V, 20 mA)
GND	19	P	–	GND digital
GND	28	P	–	GND digital
GND	39	P	–	GND analog
Monitor Input				
MON	14	I	–	High Voltage Monitor Input
LIN Interface				
LIN	43	I/O	–	LIN bus interface input/output
GND_LIN	42	P	–	LIN ground
Charge Pump				
CP1H	48	P	–	Charge Pump Capacity 1 High, connect external C
CP1L	1	P	–	Charge Pump Capacity 1 Low, connect external C
CP2H	3	P	–	Charge Pump Capacity 2 High, connect external C
CP2L	4	P	–	Charge Pump Capacity 2 Low, connect external C
VCP	2	P	–	Charge Pump Capacity
VSD	47	P	–	Battery supply input for Charge Pump
MOSFET Driver				
VDH	44	P	–	Voltage Drain High Side MOSFET Driver
SH3	46	P	–	Source High Side FET 3
SH2	6	P	–	Source High Side FET 2

5 Power Management Unit (PMU)

5.1 Features

- System modes control (startup, sleep, stop and active)
- Power management (cyclic wake-up)
- Control of system voltage regulators with diagnosis (overload, short, overvoltage)
- Fail safe mode detection and operation in case of system errors (watchdog fail)
- Wake-up sources configuration and management (LIN, MON, GPIOs)
- System error logging

5.2 Introduction

The power management unit is responsible for generating all required voltage supplies for the embedded MCU (VDDC, VDDP) and the external supply (VDDEXT). The power management unit is designed to ensure fail-safe behavior of the system IC by controlling all system modes including the corresponding transitions. Additionally, the PMU provides well defined sequences for the system mode transitions and generates hierarchical reset priorities. The reset priorities control the reset behavior of all system functionalities especially the reset behavior of the embedded MCU. All these functions are controlled by a state machine. The system master functionality of the PMU make use of an independent logic supply and system clock. For this reason, the PMU has an "Internal logic supply and system clock" module which works independently of the MCU clock.

6 System Control Unit - Digital Modules (SCU-DM)

6.1 Features

- Flexible clock configuration features
- Reset management of all system resets
- System modes control for all power modes (active, power down, sleep)
- Interrupt enabling for many system peripherals
- General purpose input output control
- Debug mode control of system peripherals

6.2 Introduction

The System Control Unit (SCU) supports all central control tasks in the TLE9877QXA40. The SCU is made up of the following sub-modules:

- Clock System and Control
- Reset Control
- Power Management
- Interrupt Management
- General Port Control
- Flexible Peripheral Management
- Module Suspend Control
- Watchdog Timer
- Error Detection and Correction in Data Memory
- Miscellaneous Control

- f_{MI_CLK} Measurement interface clock
- f_{TFILT_CLK} Analog module filter clock
- LP_CLK Clock source for all PMU submodules and WDT1

ICU (Interrupt Control Unit)

- NMI (Non-Maskable Interrupt)
- INTISR<15,13:4,1,0> External interrupt signals

RCU (Reset Control Unit)

- PMU_1V5DidPOR Undervoltage reset of power down supply
- PMU_PIN Reset generated by reset pin
- PMU_ExtWDT WDT1 reset
- PMU_IntWDT WDT (SCU) reset
- PMU_SOFT Software reset
- PMU_Wake Sleep Mode/Stop Mode exit with reset
- RESET_TYPE_3 Peripheral reset (contains all resets)
- RESET_TYPE_4 Peripheral reset (without SOFT and WDT reset)

Port Control

- P0_POCONy.PDMx driver strength control
- P1_POCONy.PDMx driver strength control

MISC Control

- MODPISELx Mode selection registers for UART (source section) and Timer (trigger or count selection)

6.3 Clock Generation Unit

The Clock Generation Unit (CGU) enables a flexible clock generation for TLE9877QXA40. During user program execution, the frequency can be modified to optimize the performance/power consumption ratio, allowing power consumption to be adapted to the actual application state.

The CGU in the TLE9877QXA40 consists of one oscillator circuit (OSC_HP), a Phase-Locked Loop (PLL) module with an internal oscillator (OSC_PLL), and a Clock Control Unit (CCU). The CGU can convert a low-frequency input/external clock signal to a high-frequency internal clock.

The system clock f_{SYS} is generated from of the following selectable clocks:

- PLL clock output f_{PLL}
- Direct clock from oscillator OSC_HP f_{OSC}
- Low precision clock f_{LP_CLK} (HW-enabled for startup after reset and during power-down wake-up sequence)

Table 5 External CAP Capacitors

Fundamental Mode Crystal Frequency (approx., MHz)	Load Caps C_1, C_2 (pF)
4	33
8	18
12	12
16	10
20	10
25	8

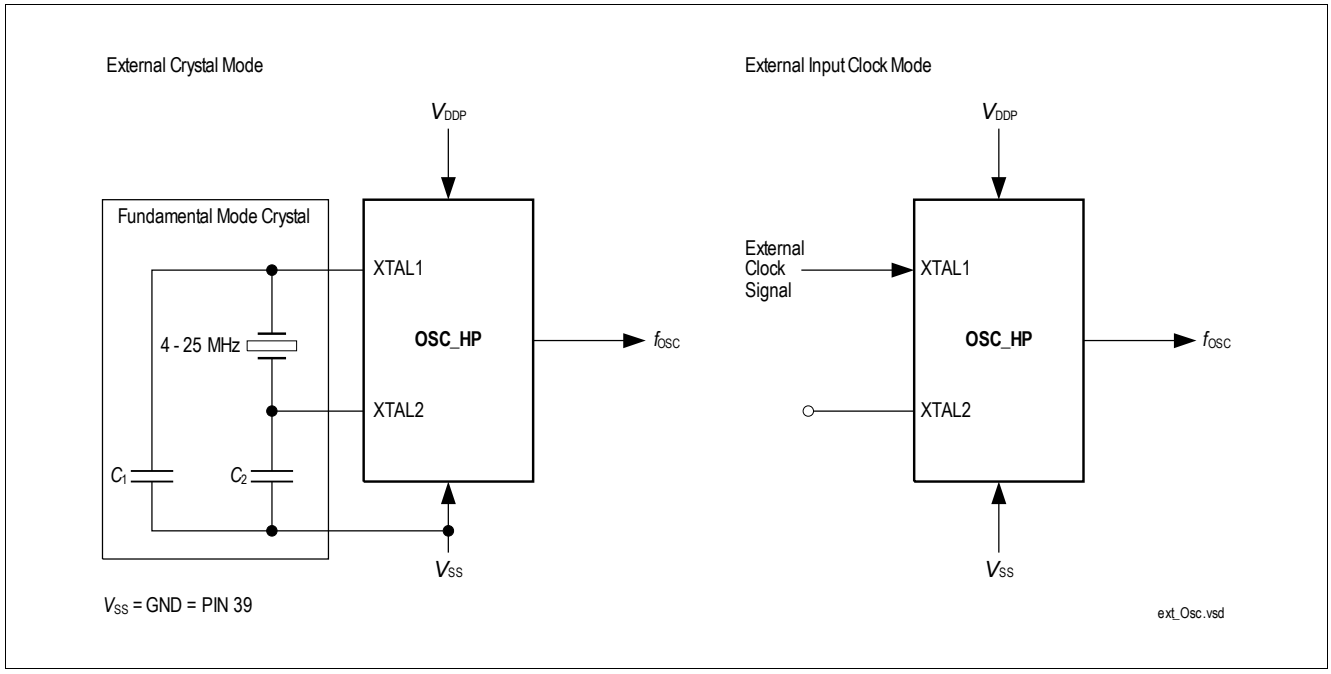

Figure 10 TLE9877QXA40 External Circuitry for the OSC_HP

13.2 Introduction

The behavior of the Watchdog Timer in Active Mode is illustrated in **Figure 16**.

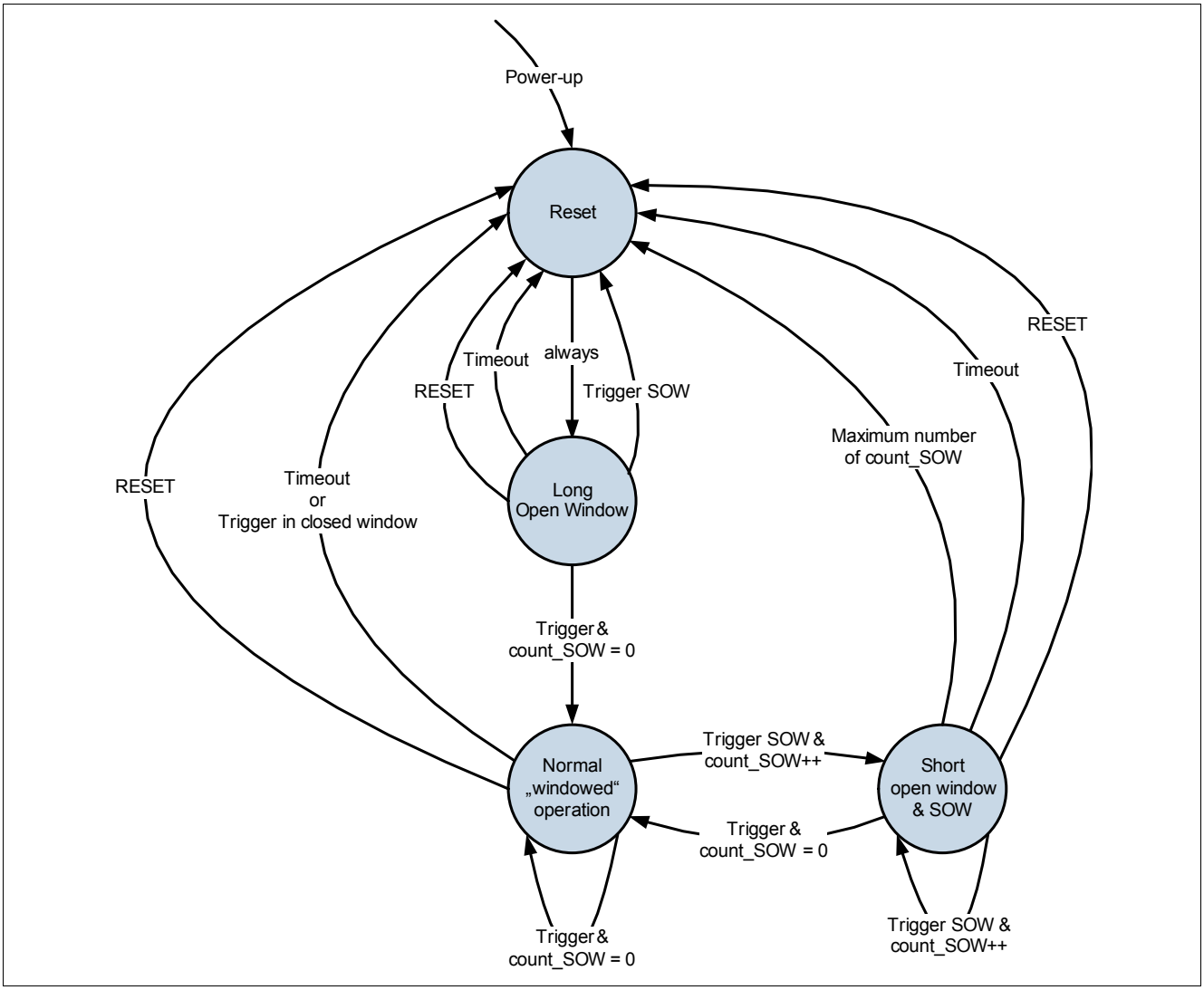

Figure 16 Watchdog Timer Behavior

Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register Px_PUDSEL selects whether a pull-up or the pull-down device is activated while register Px_PUDEN enables or disables the pull device.

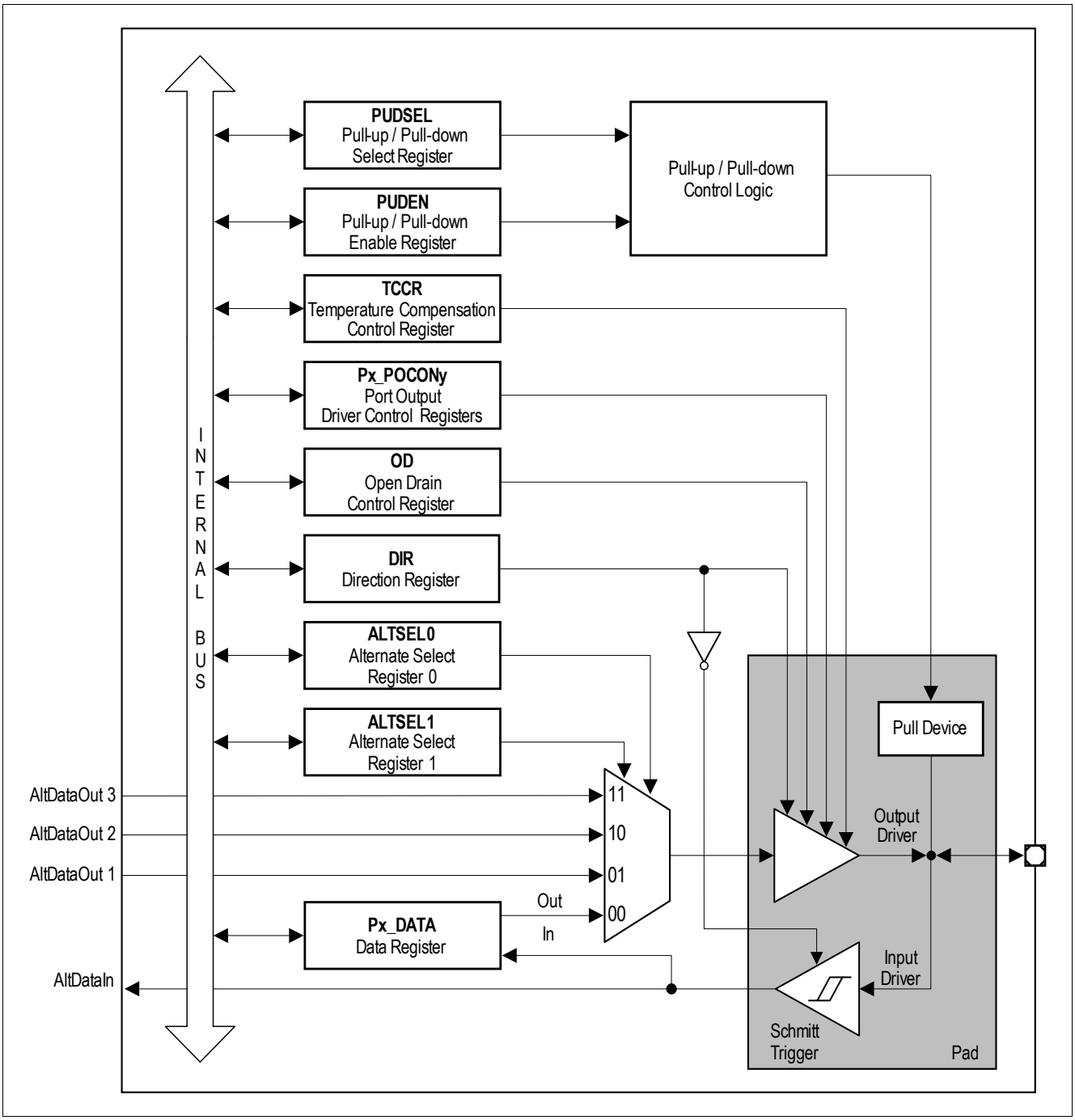

Figure 17 General Structure of Bidirectional Port (P0, P1)

14.2.2 Port 2

Figure 18 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt trigger device and can be read via register P2_DATA. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register P2_PUDSEL selects whether a pull-up or the pull-down device is activated while register P2_PUDEN enables or disables the pull device. The analog input (AnalogIn) bypasses the digital circuitry and Schmitt trigger device for direct feed-through to the ADC input channels.

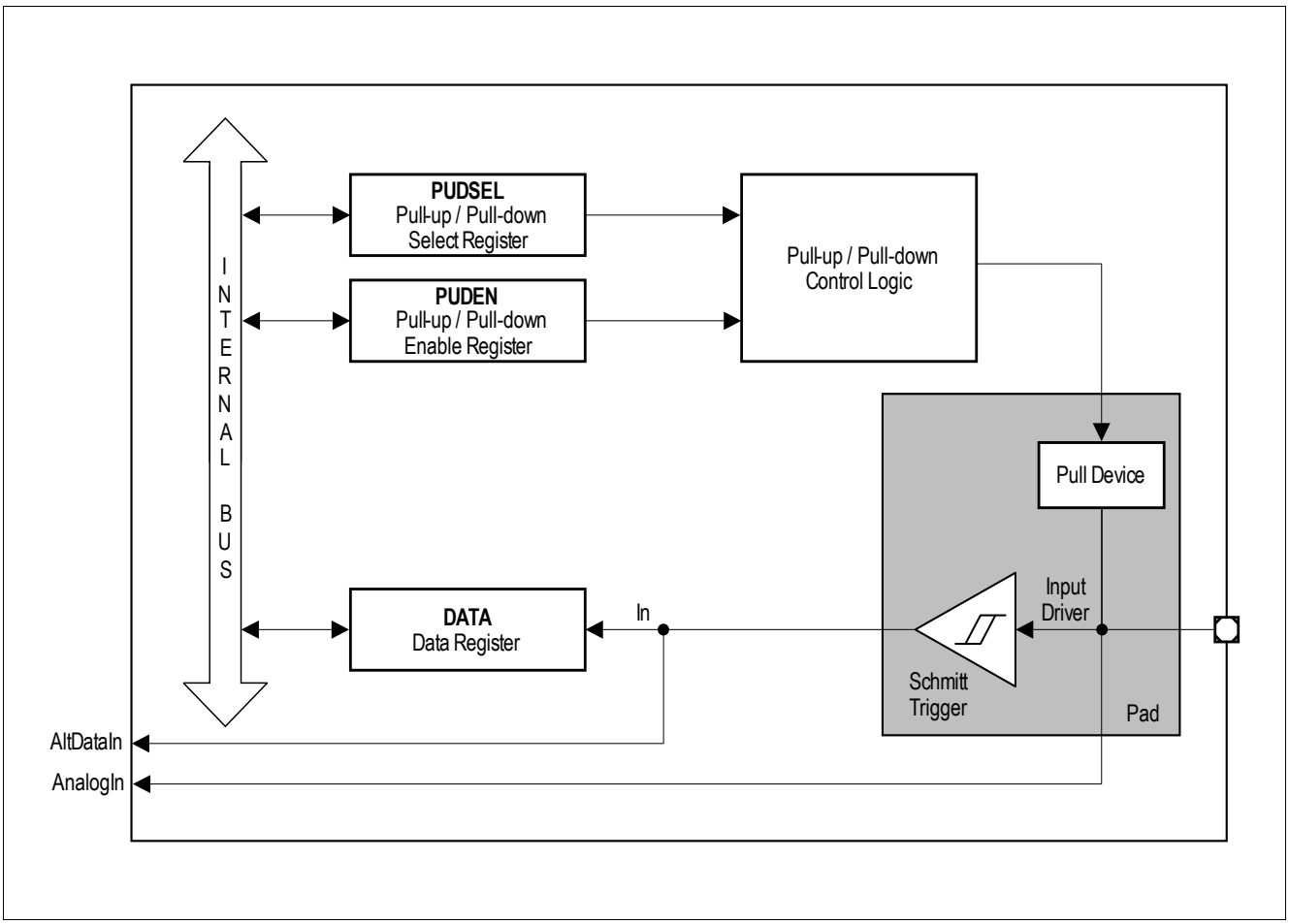

Figure 18 General Structure of Input Port (P2)

15.2.1 Block Diagram GPT1

Block GPT1 contains three timers/counters: The core timer T3 and the two auxiliary timers T2 and T4. The maximum resolution is $f_{GPT}/4$. The auxiliary timers of GPT1 may optionally be configured as reload or capture registers for the core timer.

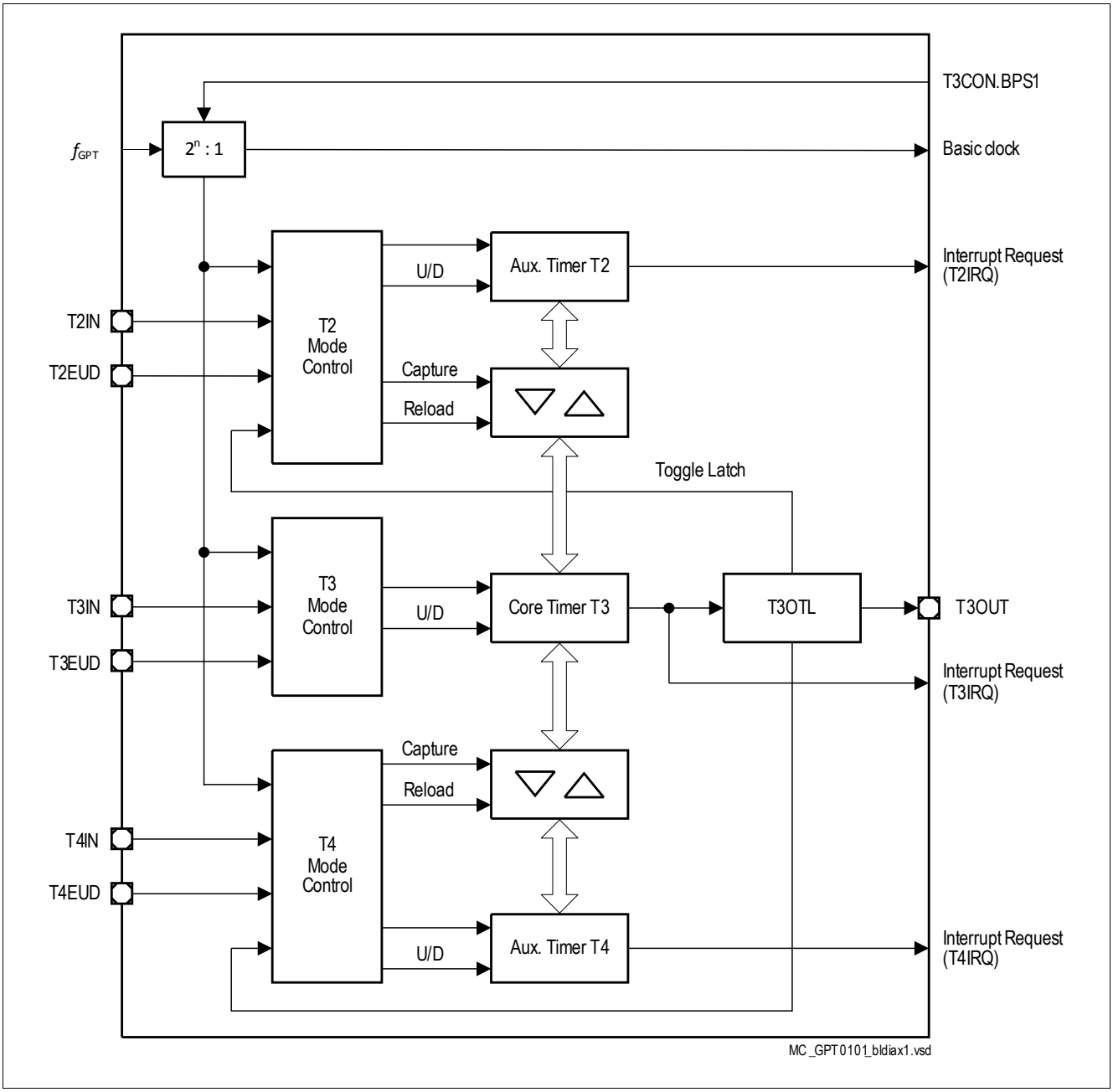

Figure 19 GPT1 Block Diagram (n = 2 … 5)

17 Timer3

17.1 Features

- 16-bit incremental timer/counter (counting up)
- Counting frequency up to f_{sys}
- Selectable clock prescaler
- 6 modes of operation
- Interrupt up on overflow
- Interrupt on compare

17.2 Introduction

The possible applications for the timer include measuring the time interval between events, counting events and generating a signal at regular intervals.

Timer3 can function as timer or counter. When functioning as a timer, Timer3 is incremented in periods based on the MI_CLK or LP_CLK clock. When functioning as a counter, Timer3 is incremented in response to a 1-to-0 transition (falling edge) at its respective input. Timer3 can be configured in four different operating modes to use in a variety of applications, see **Table 12**.

Several operating modes can be used for different tasks such as the following:

- simple time measurement between two events
- triggering of the measuring unit upon PWM/CCU6 unit
- measurement of the 100kHz LP_CLK2

17.3 Functional Description

Six modes of operation are provided to fulfill various tasks using this timer. In every mode the clocking source can be selected between MI_CLK and LP_CLK. A prescaler provides in addition capability to divide the selected clock source by 2, 4 or 8. The timer counts upwards, starting with the value in the timer count registers, until the maximum count value which depends on the selected mode of operation. Timer 3 provides two individual interrupts upon counter overflow, one for the low-byte and one for the high-byte counter register.

17.3.1 Timer3 Modes Overview

The following table provides an overview of the timer modes together with the reasonable configuration options in **Table 12**.

Table 12 Timer3 Modes

Mode	Sub-Mode	Operation
0	**No Sub-Mode**	**13-bit Timer** The timer is essentially an 8-bit counter with a divide-by-32 prescaler.
1	**a**	**16-bit Timer** The timer registers, TL3 and TH3, are concatenated to form a 16-bit counter.
1	**b**	**16-bit Timer triggered by an event** The timer registers, TL3 and TH3, are concatenated to form a 16-bit counter, which is triggered by an event to enable a single shot measurement on a preset channel with the measurement unit.

24 10-Bit Analog Digital Converter (ADC1)

24.1 Features

The principal features of the ADC1 are:

- Up to 8 analog input channels (channel 7 reserved for future use)
- Flexible results handling
  - 8-bit and 10-bit resolution
- Flexible source selection due to sequencer
  - insert one exceptional sequence (ESM)
  - insert one interrupt measurement into the current sequence (EIM), single or up to 128 times
  - software mode
- Conversion sample time (separate for each channel) adjustable to adapt to sensors and reference
- Standard external reference (VAREF) to support ratiometric measurements and different signal scales
- DMA support, transfer ADC conversion results via DMA into RAM
- Support of suspend and power saving modes
- Result data protection for slow CPU access (wait-for-read mode)
- Programmable clock divider
- Integrated sample and hold circuitry

24.2 Introduction

The TLE9877QXA40 includes a high-performance 10-bit Analog-to-Digital Converter (ADC1) with eight multiplexed analog input channels. The ADC1 uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC1 are available at AN0, AN2 - AN5.

25 High-Voltage Monitor Input

25.1 Features

- High-voltage input with V_S/2 threshold voltage
- Integrated selectable pull-up and pull-down current sources
- Wake capability for power saving modes
- Level change sensitivity configurable for transitions from low to high, high to low or both directions

25.2 Introduction

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at the high-voltage MON pin in low-power mode. The input is sensitive to a input level monitoring, this is available when the module is switched to active mode with the SFR bit EN.

To use the Wake function during low power mode of the IC, the monitoring pin is switched to Sleep Mode via the SFR bit EN.

25.2.1 Block Diagram

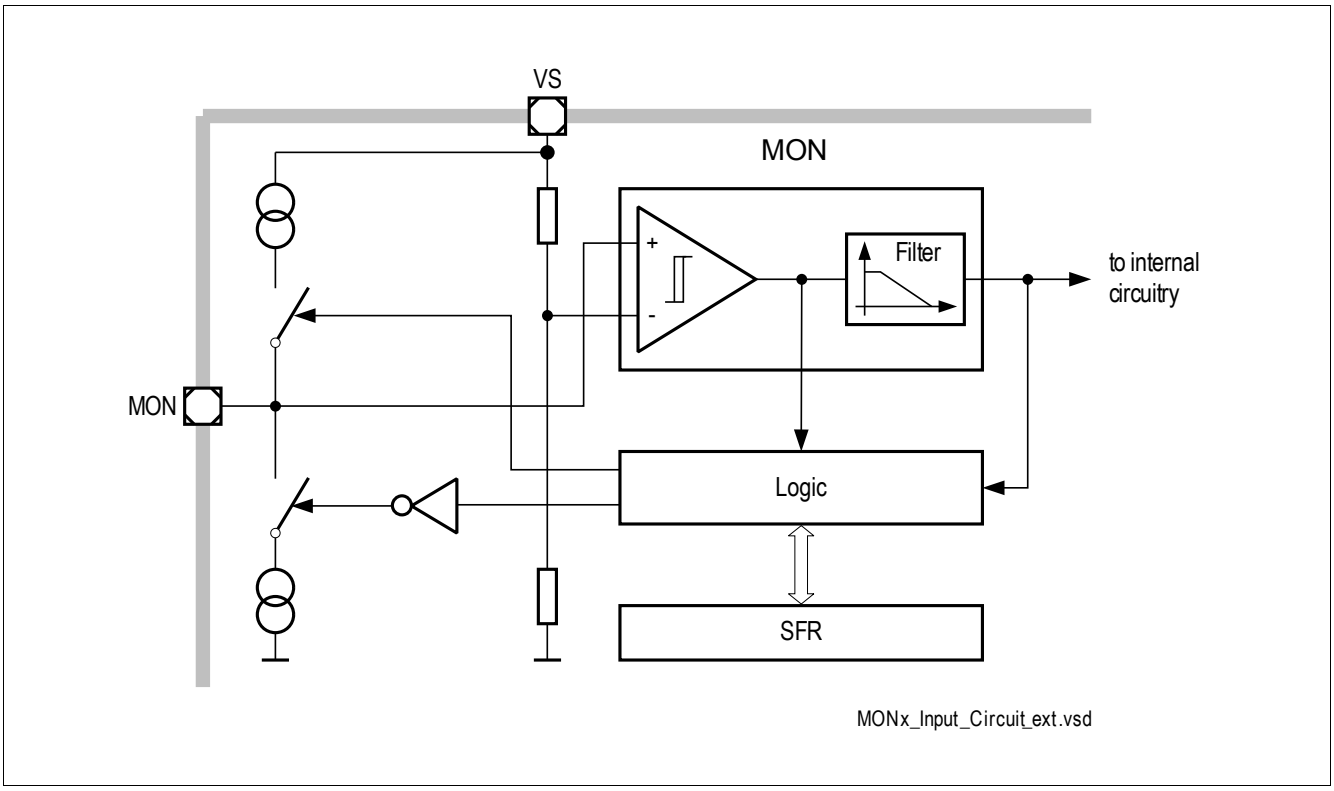

Figure 29 Monitoring Input Block Diagram

Table 19 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current consumption in Sleep Mode with cyclic wake	I_{Cyclic}	–	–	110	µA	T_J = -40°C to 85°C; V_S = 5.5 V to 18V; t_{Cyclic_ON} = 4ms; t_{Cyclic_OFF} = 2048 ms;[2)]	P_1.3.4
Current consumption in Stop Mode	I_{Stop}	–	110	160	µA	System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND; T_J = -40°C to 85°C; V_S = 5.5 V to 18V	P_1.3.10
Current consumption in Stop Mode-Extended temperature range 1	I_{Stop_extend}	–	600	1800	µA	System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND; T_J = -40 °C to 150 °C; V_S = 5.5 V to 18 V	P_1.3.20

1) Current on V_S, ADC1/2 active, timer running, LIN active (recessive).

2) Incl. leakage currents form VDH, VSD and MON

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

29.2 Power Management Unit (PMU)

This chapter includes all electrical characteristics of the Power Management Unit

29.2.1 PMU I/O Supply (VDDP) Parameters

This chapter describes all electrical parameters which are observable on SoC level. For this purpose only the pad-supply VDDP and the transition times between the system modes are specified here.

Table 22 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VDDP}	0	–	50	mA	1)	P_2.1.1
Specified output current	I_{VDDP}	0	–	30	mA	1)2)	P_2.1.22
Required decoupling capacitance	C_{VDDP1}	0.47	–	2.2	µF	3)4) ESR < 1Ω; the specified capacitor value is a typical value.	P_2.1.2
Required buffer capacitance for stability (load jumps)	C_{VDDP2}	1	–	2.2	µF	3)4) The specified capacitor value is a typical value.	P_2.1.20
Output voltage including line and load regulation @ Active Mode	V_{DDPOUT}	4.9	5.0	5.1	V	5) I_{load} < 90mA; V_S > 5.5V	P_2.1.3
Output voltage including line and load regulation @ Active Mode	V_{DDPOUT}	4.9	5.0	5.1	V	2)5) I_{load} < 70mA; V_S > 5.5V	P_2.1.23
Output voltage including line and load regulation @ Stop Mode	$V_{DDPOUTSTOP}$	4.5	5.0	5.5	V	5) I_{load} is only internal; V_S > 5.5V	P_2.1.21
Output drop @ Active Mode	$V_{SVDDPout}$	–	50	400	mV	I_{VDDP} = 30mA6); 3.5V < V_S < 5.0V	P_2.1.4
Load regulation @ Active Mode	$V_{VDDPLOR}$	-50	–	50	mV	2 ... 90mA; C = 570nF	P_2.1.5
Line regulation @ Active Mode	$V_{VDDPLIR}$	-50	–	50	mV	V_S = 5.5 ... 28V	P_2.1.6
Overvoltage detection	V_{DDPOV}	5.14	–	5.4	V	V_S > 5.5V; Overvoltage leads to SUPPLY_NMI	P_2.1.7
Overvoltage detection filter time	t_{FILT_VDDPOV}	–	735	–	µs	3)7)	P_2.1.24
Voltage OK detection	V_{DDPOK}	–	3	–	V	3)	P_2.1.25
Voltage stable detection range8)	ΔV_{DDPSTB}	- 220	–	+ 220	mV	3)	P_2.1.26
Undervoltage reset	V_{DDPUV}	2.5	2.6	2.7	V	–	P_2.1.8
Overcurrent diagnostic	I_{VDDPOC}	91	–	220	mA	–	P_2.1.9

Table 33 Electrical Characteristics LIN Transceiver (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Bus short circuit current	$I_{BUS,sc}$	40	100	150	mA	Current Limitation for driver dominant state driver on V_{BUS} = 18 V; LIN Spec 2.2 (Par. 12)	P_6.1.10
Bus short circuit filter time	$t_{BUS,sc}$	–	5	–	µs	[6]The overall bus short circuit filter time is a sum of tBUS,sc + digital filter time. The digital filter time is 4 µs (typ.)	P_6.1.71
Leakage current (loss of ground)	$I_{BUS\_NO\_GND}$	-1000	-450	1000	µA	V_S = 12 V; 0 < V_{BUS} < 18 V; LIN Spec 2.2 (Par. 15)	P_6.1.11
Leakage current	$I_{BUS\_NO\_BAT}$	–	10	20	µA	V_S = 0 V; V_{BUS} = 18 V; LIN Spec 2.2 (Par. 16)	P_6.1.12
Leakage current	$I_{BUS\_PAS\_dom}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN Spec 2.2 (Par. 13)	P_6.1.13
Leakage current	$I_{BUS\_PAS\_rec}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; LIN Spec 2.2 (Par. 14)	P_6.1.14
Bus pull-up resistance	R_{BUS}	20	30	47	kΩ	Normal mode LIN Spec 2.2 (Par. 26)	P_6.1.15
AC Characteristics - Transceiver Normal Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.16
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.17
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$; LIN Spec 2.2 (Par. 32)	P_6.1.18
Duty cycle D1 Normal Slope Mode (for worst case at 20 kbit/s)	t_{duty1}	0.396	–	–		[4] duty cycle 1 TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 5.5 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN Spec 2.2 (Par. 27)	P_6.1.19

Table 33 Electrical Characteristics LIN Transceiver (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	–	P_6.1.32
Receiver delay symmetry	$t_{sym,R}$	-1.0	–	1.5	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$;	P_6.1.33
Duty cycle D7 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry	t_{duty1}	0.399	–	–		5) duty cycle D7 THRec(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 13.5 V; t_{bit} = 8.7 µs; D7 = $t_{bus\_rec(min)}$/2 t_{bit};	P_6.1.34
Duty cycle D8 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry	t_{duty2}	–	–	0.578		5) duty cycle 8 TH_{Rec}(min) = 0.422 × V_S; TH_{Dom}(min) = 0.284 × V_S;V_S = 13.5 V; t_{bit} = 8.7 µs; D8 = $t_{bus\_rec(max)}$/2 t_{bit};	P_6.1.35
LIN input capacity	C_{LIN_IN}	–	15	30	pF	6)	P_6.1.69
TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V	P_6.1.36
Thermal Shutdown (Junction Temperature)							
Thermal shutdown temp.	T_{jSD}	190	200	215	°C	6)	P_6.1.65
Thermal shutdown hyst.	ΔT	–	10	–	K	6)	P_6.1.66

1) Maximum limit specified by design.
2) $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\ rec})/2$
3) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$
4) Bus load concerning LIN Spec 2.2:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
5) Bus load
   Load 1 = 1 nF / 500 Ω = C_{BUS} / R_{BUS}
6) Not subject to production test, specified by design.