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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, SCI, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	73
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.3M x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s726a0d216fp-v0

Items	Specification
General I/O ports	• SH726A: 57 I/Os, 8 inputs with open-drain outputs, and 8 inputs • SH726B: 74 I/Os, 8 inputs with open-drain outputs, and 12 inputs • Input or output can be selected for each bit
A/D converter	• 10-bit resolution • Input SH726A: six channels SH726B: eight channels • A/D conversion request by the external trigger or timer trigger
User break controller	• Break channels: two channels • Possible to set an address, data value, access type, and data size as break conditions.
User debugging interface	• E10A emulator support • JTAG-standard pin assignment
On-chip RAM	• 64-Kbyte memory for high-speed operation (16 Kbytes × 4) • 1.25-Mbyte large capacity memory for video display/recording and work (128-Kbytes are used for data retention) • 128-Kbyte memory for data retention (16 Kbytes× 2, 32 Kbytes×1, 64 Kbytes×1)
Boot modes	• Two boot modes (boot modes 0 and 1) Boot mode 0: Booting from memory connected to $\overline{\text{CS0}}$ area Boot mode 1: Booting from a serial flash memory
Power supply voltage	• Vcc: 1.15 to 1.35 V • PVcc: 3.0 to 3.6 V
Packages	SH726A (1) • 120-pin QFP, 16-mm square, 0.5-mm pitch JEITA package code: P-LQFP120-16 × 16-0.50 Renesas code: PLQP0120KA-A SH726A (2) • 120-pin QFP, 14-mm square, 0.4-mm pitch JEITA package code: P-LQFP120-14 × 14-0.40 Renesas code: PLQP0120LA-A SH726B • 144-pin QFP, 20-mm square, 0.5-mm pitch JEITA package code: P-LQFP144-20 × 20-0.50 Renesas code: PLQP0144KA-A

1.4 Pin Assignment

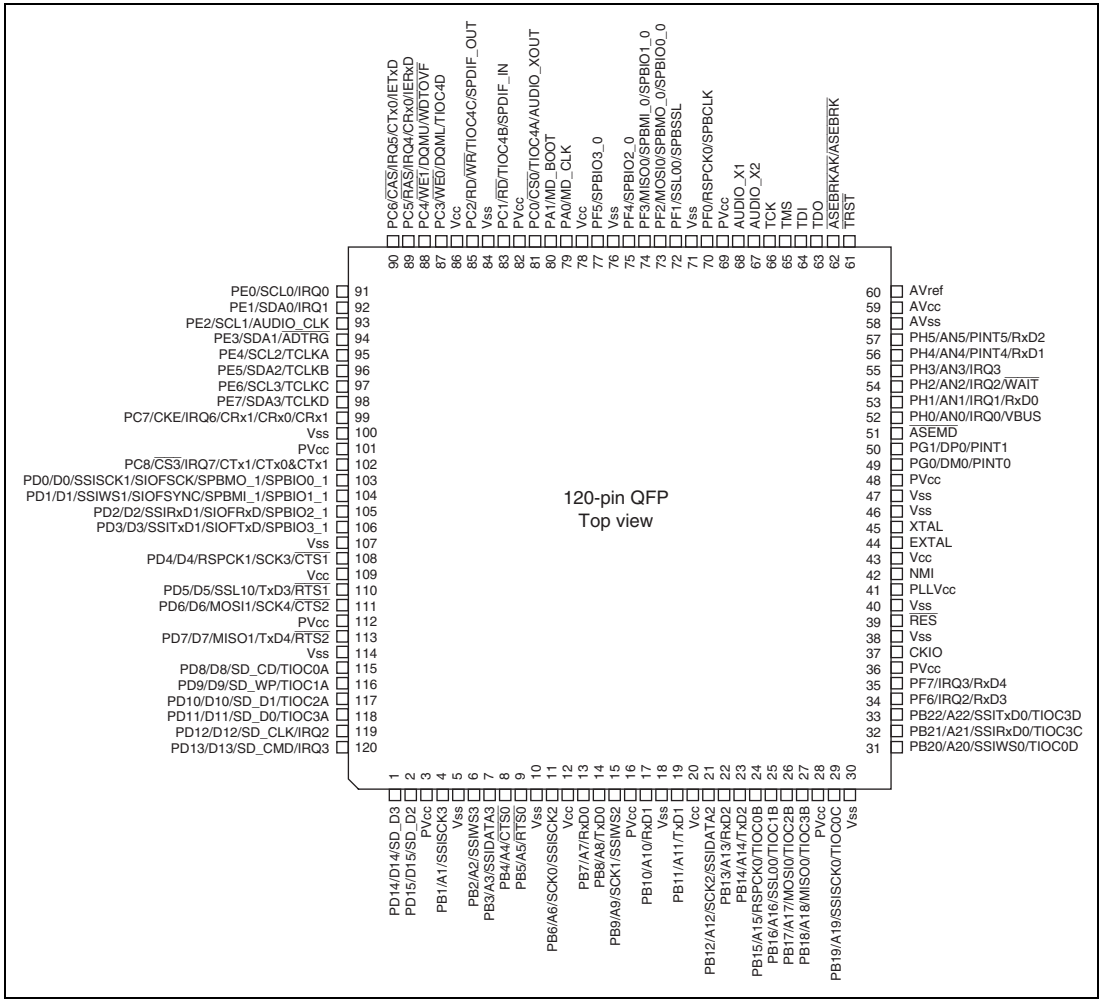


Figure 1.2 (1) Pin Assignment for the SH726A Group

Interrupt Source			Interrupt Vector		Interrupt Priority (Initial Value)	Corresponding IPR (Bit)	IPR Setting Unit Internal Priority	Default Priority
			Vector	Vector Table Address Offset				
Serial communi-cation interface with FIFO	Channel 3	BRI3	244	H'000003D0 to H'000003D3	0 to 15 (0)	IPR17 (3 to 0)	1	High
		ERI3	245	H'000003D4 to H'000003D7			2	
		RXI3	246	H'000003D8 to H'000003DB			3	
		TXI3	247	H'000003DC to H'000003DF			4	
	Channel 4	BRI4	248	H'000003E0 to H'000003E3	0 to 15 (0)	IPR18 (15 to 12)	1	
		ERI4	249	H'000003E4 to H'000003E7			2	
		RXI4	250	H'000003E8 to H'000003EB			3	
		TXI4	251	H'000003EC to H'000003EF			4	
Serial I/O with FIFO	SIOFI		252	H'000003F0 to H'000003F3	0 to 15 (0)	IPR19 (15 to 12)	—	
Renesas serial peripheral interface	Channel 0	SPEI0	253	H'000003F4 to H'000003F7	0 to 15 (0)	IPR19 (11 to 8)	1	
		SPRI0	254	H'000003F8 to H'000003FB			2	
		SPTI0	255	H'000003FC to H'000003FF			3	
	Channel 1	SPEI1	256	H'00000400 to H'00000403	0 to 15 (0)	IPR19 (7 to 4)	1	
		SPRI1	257	H'00000404 to H'00000407			2	
		SPTI1	258	H'00000408 to H'0000040B			3	Low

(3) SDRAM*

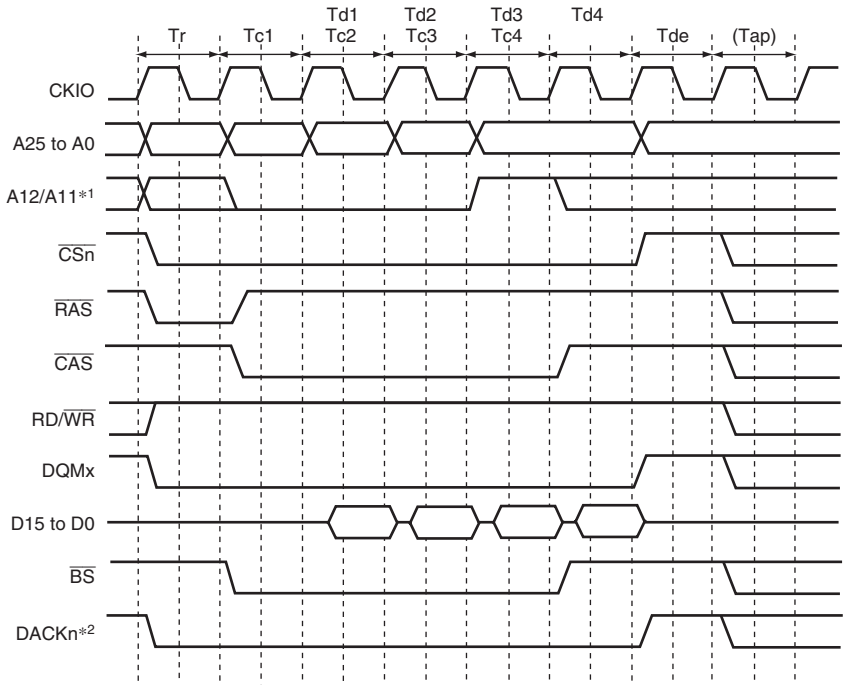
- CS2WCR

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	A2CL[1:0]		-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
9	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
8, 7	A2CL[1:0]	10	R/W	CAS Latency for Area 2 Specify the CAS latency for area 2. 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles
6 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: * If only one area is connected to the SDRAM, specify area 3. In this case, specify area 2 as normal space or SRAM with byte selection.



Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 10.11 Burst Read Basic Timing (CAS Latency 1, Auto Pre-Charge)

(a) Auto-refreshing

Refreshing is performed at intervals determined by the input clock selected by bits CKS2 to CKS0 in RTCSR, and the value set by in RTCOR. The value of bits CKS2 to CKS0 in RTCOR should be set so as to satisfy the refresh interval stipulation for the SDRAM used. First make the settings for RTCOR, RTCNT, and the RMODE and RFSH bits in SDCR, and then make the CKS2 to CKS0 and RRC2 to RRC0 settings. When the clock is selected by bits CKS2 to CKS0, RTCNT starts counting up from the value at that time. The RTCNT value is constantly compared with the RTCOR value, and if the two values are the same, a refresh request is generated and an auto-refresh is performed for the number of times specified by the RRC2 to RRC0. At the same time, RTCNT is cleared to zero and the count-up is restarted.

Figure 10.22 shows the auto-refresh cycle timing. After starting the auto refreshing, PALL command is issued in the Tp cycle to make all the banks to pre-charged state from active state when some bank is being pre-charged. Then REF command is issued in the Trr cycle after inserting idle cycles of which number is specified by the WTRP1 and WTRP0 bits in CS3WCR. A new command is not issued for the duration of the number of cycles specified by the WTRC1 and WTRC0 bits in CS3WCR after the Trr cycle. The WTRC1 and WTRC0 bits must be set so as to satisfy the SDRAM refreshing cycle time stipulation (tRC). An idle cycle is inserted between the Tp cycle and Trr cycle when the setting value of the WTRP1 and WTRP0 bits in CS3WCR is longer than or equal to 1 cycle.

(3) Relationship between Request Modes and Bus Modes by DMA Transfer Category

Table 11.9 shows the relationship between request modes and bus modes by DMA transfer category.

Table 11.9 Relationship of Request Modes and Bus Modes by DMA Transfer Category

Address Mode	Transfer Category	Request Mode	Bus Mode	Transfer Size (Bits)	Usable Channels
Dual	External device with DACK and external memory	External	B/C	8/16/32/128	0
	External device with DACK and memory-mapped external device	External	B/C	8/16/32/128	0
	External memory and external memory	All*4	B/C	8/16/32/128	0 to 15*3
	External memory and memory-mapped external device	All*4	B/C	8/16/32/128	0 to 15*3
	Memory-mapped external device and memory-mapped external device	All*4	B/C	8/16/32/128	0 to 15*3
	External memory and on-chip peripheral module	All*1	B/C*5	8/16/32/128*2	0 to 15*3
	Memory-mapped external device and on-chip peripheral module	All*1	B/C*5	8/16/32/128*2	0 to 15*3
	On-chip peripheral module and on-chip peripheral module	All*1	B/C*5	8/16/32/128*2	0 to 15*3
	On-chip memory and on-chip memory	All*4	B/C	8/16/32/128	0 to 15*3
	On-chip memory and memory-mapped external device	All*4	B/C	8/16/32/128	0 to 15*3
	On-chip memory and on-chip peripheral module	All*1	B/C*5	8/16/32/128*2	0 to 15*3
	On-chip memory and external memory	All*4	B/C	8/16/32/128	0 to 15*3
Single	External device with DACK and external memory	External	B/C	8/16/32/128	0
	External device with DACK and memory-mapped external device	External	B/C	8/16/32/128	0

[Legend]

B: Burst

C: Cycle steal

Notes: 1. External requests, auto requests, and on-chip peripheral module requests are all available. However, in the case of internal module request, along with the exception of the multi-function timer pulse unit 2 and the compare match timer as the transfer request source, the requesting module must be designated as the transfer source or the transfer destination. In the SH726A, external requests cannot be used.

(11) Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Complementary PWM Mode

Figure 12.125 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in complementary PWM mode after re-setting.

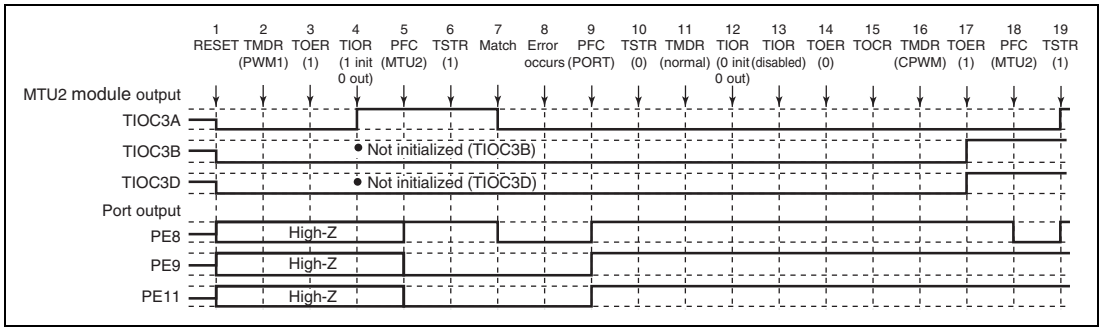


Figure 12.125 Error Occurrence in PWM Mode 1, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 12.121.

11. Set normal mode for initialization of the normal mode waveform generation section.
12. Initialize the PWM mode 1 waveform generation section with TIOR.
13. Disable operation of the PWM mode 1 waveform generation section with TIOR.
14. Disable channel 3 and 4 output with TOER.
15. Select the complementary PWM output level and cyclic output enabling/disabling with TOCR.
16. Set complementary PWM.
17. Enable channel 3 and 4 output with TOER.
18. Set the multi-function timer pulse unit 2 output with the general I/O port.
19. Operation is restarted by TSTR.

13.5.2 Conflict between Word-Write and Count-Up Processes of CMCNT

Even when the count-up occurs in the T2 cycle while writing to CMCNT in words, the writing has priority over the count-up. In this case, the count-up is not performed. Figure 13.6 shows the timing to write to CMCNT in words.

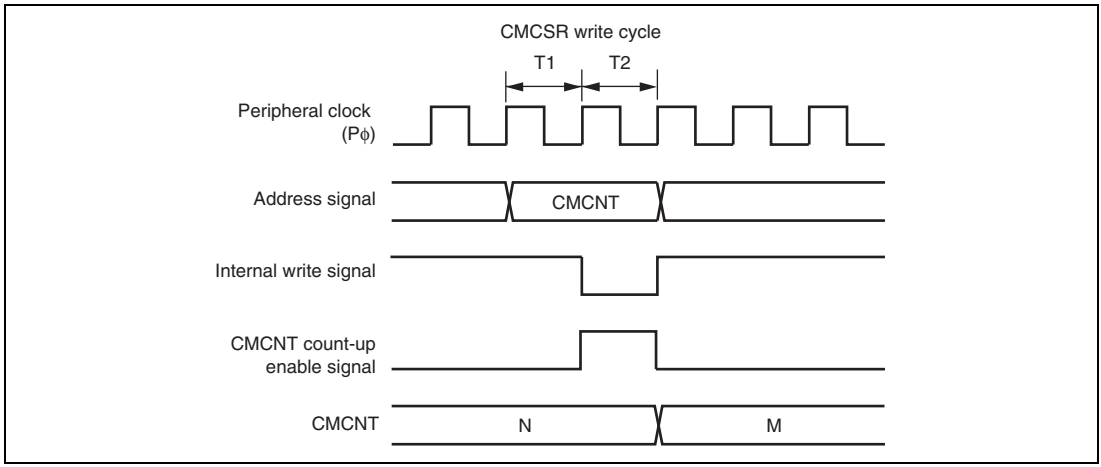


Figure 13.6 Conflict between Word-Write and Count-Up Processes of CMCNT

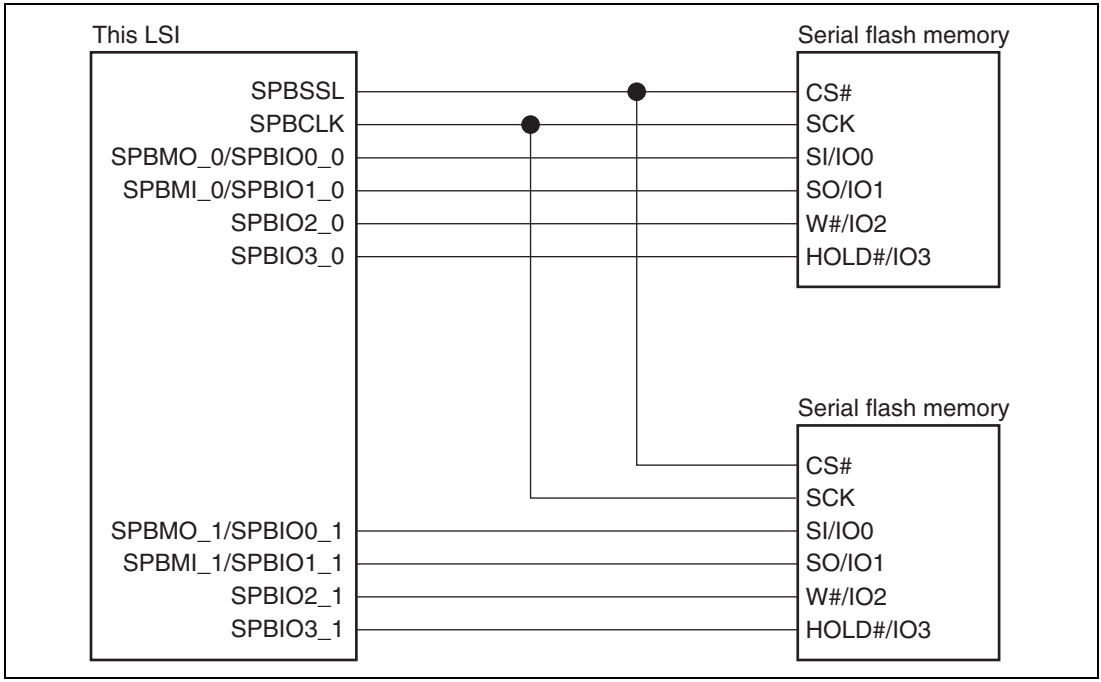


Figure 18.3 System Configuration Example with 4-Bit Data Size and Two Serial Flash Memories Connected (BSZ[1:0] Bits in CMNCR = 01)

18.5.2 Address Map

In external address space read mode, the serial flash connected is assigned in the SPI multi I/O bus space. A maximum accessible address space differs depending on the number of serial flash memories connected. In combination with DREAR, a maximum of 4 Gbytes can be accessed when one serial flash memory is connected, and a maximum of 8 Gbytes can be accessed when two memories are connected.

Table 18.4 Address Map

Number of Serial Flash Memories Connected	Internal Address	Cache	Max. Access Area
1	H'18000000 to H'1BFFFFFF	Enabled	4 Gbytes
	H'38000000 to H'3BFFFFFF	Disabled	
2	H'18000000 to H'1BFFFFFF	Enabled	8 Gbytes
	H'38000000 to H'3BFFFFFF	Disabled	

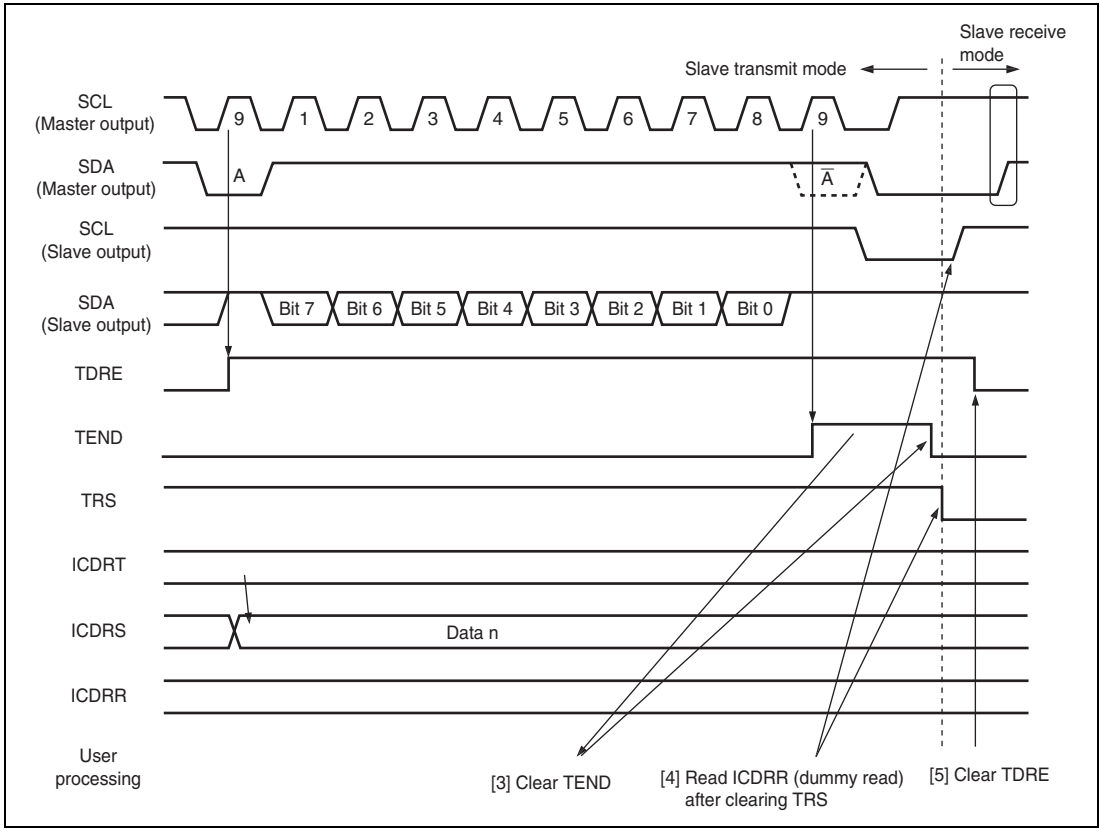


Figure 19.10 Slave Transmit Mode Operation Timing (2)

23.1.1 IEBus Communications Protocol

An overview of the IEBus is provided below.

- Communications method: Half-duplex asynchronous communications
- Multi-master system
  All units connected to the IEBus can transfer data to other units.
- Broadcast communications function (one-to-many communications)
  — Group broadcast communications: Broadcast communications to group unit
  — General broadcast communications: Broadcast communications to all units
- Mode is selectable (three modes with different transfer speeds)

Table 23.1 Mode Types

Mode	IEBϕ*1 = 12, 18, 24, 30, 36, 42, 48 MHz*2	IEBϕ*1 = 12.58, 18.87, 25.16, 31.45, 37.74, 44.03 MHz*2	Maximum Number of Transfer Bytes (byte/frame)
0	About 3.9 kbps	About 4.1 kbps	16
1	About 17 kbps	About 18 kbps	32
2	About 26 kbps	About 27 kbps	128

Notes: 1. Peripheral clock (Pϕ), or clocks for AUDIO_X1 and AUDIO_X2
2. Oscillation frequency when this LSI is used

- Access control: CSMA/CD (Carrier Sense Multiple Access with Collision Detection)
  Priority of bus mastership is as follows.
  — Broadcast communications (one-to-many communications) have priority over normal communications (one-to-one communications).
  — A smaller master address has priority.
- Communications scale
  — Number of units: Up to 50
  — Cable length: Up to 150 m (when using a twisted-pair cable)

Note: The communications scale of the actual system depends on the characteristics of the externally mounted IEBus driver/receiver and the cable used.

(b) Unlocking

When the control bits indicate the lock (H'3, H'A, or H'B) or unlock (H'6) operation and the byte data for the number of bytes specified by the message length bits are transmitted/received in a single communications frame, the slave unit is unlocked by the master unit. In this case, the bit (bit 2) relevant to locking in the byte indicating the slave status is cleared to 0.

Note that locking and unlocking are not done in broadcast communications.

Note: * There are three ways to cause a locked unit to unlock itself.
- Perform a power-on reset
- Put the unit in deep standby mode
- Issue an unlock command through the IEBus command register (IECMR)

Note that the LCK flag in IEFLG can be used to check whether the unit is locked or unlocked.

23.1.4 Bit Format

Figure 23.4 shows the bit format (conceptual diagram) configuring the IEBus communications frame.

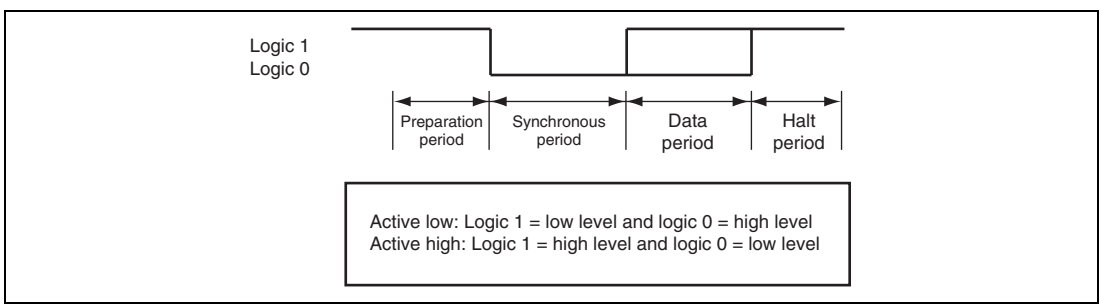


Figure 23.4 IEBus Bit Format (Conceptual Diagram)

Each period of the bit format for use of active high signals is described below.

- Preparation period: first logic 1 period (high level)
- Synchronous period: subsequent logic 0 period (low level)
- Data period: period indicating bit value (logic 1: high level, logic 0: low level)
- Halt period: last logic 1 period (high level)

27.3.29 Pipe Window Select Register (PIPESEL)

PIPE1 to PIPE 9 should be set using PIPESEL, PIPECFG, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN. After selecting the pipe using PIPESEL, functions of the pipe should be set using PIPECFG, PIPEMAXP, and PIPEPERI. PIPEnCTR, PIPEnTRE, and PIPEnTRN can be set regardless of the pipe selection in PIPESEL.

This register is initialized by a power-on reset. Here, not only the register for the selected pipe but the registers for all the pipes are initialized.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(17) Port F Control Register 0 (PFCR0)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	PF3MD[1:0]		-	-	PF2MD[1:0]		-	-	PF1MD[1:0]		-	-	PF0MD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	PF3MD[1:0]	00	R/W	PF3 Mode Select the function of the PF3. 00: PF3 01: MISO0 10: SPBMI_0/SPBIO1_0 11: Setting prohibited
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PF2MD[1:0]	00	R/W	PF2 Mode Select the function of the PF2. 00: PF2 01: MOSI0 10: SPBMO_0/SPBIO0_0 11: Setting prohibited
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	PF1MD[1:0]	00	R/W	PF1 Mode Select the function of the PF1. 00: PF1 01: SSL00 10: SPBSSL 11: Setting prohibited

(19) Port H Control Register 1 (PHCR1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	PH7MD[1:0]		-	-	PH6MD[1:0]		-	-	PH5MD[1:0]		-	-	PH4MD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	PH7MD[1:0]	00	R/W	PH7 Mode Select the function of the PH7. 00: PH7 01: AN7 10: PINT7 11: RxD4 Note: In the SH726A, bits 13 and 12 are reserved. These bits are always read as 0. The write value should always be 0.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PH6MD[1:0]	00	R/W	PH6 Mode Select the function of the PH6. 00: PH6 01: AN6 10: PINT6 11: RxD3 Note: In the SH726A, bits 9 and 8 are reserved. These bits are always read as 0. The write value should always be 0.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

32.2.5 Standby Control Register 5 (STBCR5)

STBCR5 is an 8-bit readable/writable register that controls the operation of each module.

Note: When writing to this register, see section 32.4, Usage Notes.

Bit:	7	6	5	4	3	2	1	0
	MSTP 57	MSTP 56	MSTP 55	-	MSTP 53	MSTP 52	MSTP 51	MSTP 50
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	MSTP57	1	R/W	Module Stop 57 When the MSTP57 bit is set to 1, the clock supply to channel 0 of the I^2C bus interface 3 is halted. 0: Channel 0 of the I^2C bus interface 3 runs. 1: Clock supply to channel 0 of the I^2C bus interface 3 is halted.
6	MSTP56	1	R/W	Module Stop 56 When the MSTP56 bit is set to 1, the clock supply to channel 1 of the I^2C bus interface 3 is halted. 0: Channel 1 of the I^2C bus interface 3 runs. 1: Clock supply to channel 1 of the I^2C bus interface 3 is halted.
5	MSTP55	1	R/W	Module Stop 55 When the MSTP55 bit is set to 1, the clock supply to channel 2 of the I^2C bus interface 3 is halted. 0: Channel 2 of the I^2C bus interface 3 runs. 1: Clock supply to channel 2 of the I^2C bus interface 3 is halted.
4	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

32.2.13 System Control Register 4 (SYSCR4)

SYSCR4 is an 8-bit readable/writable register that enables or disables writing to a specified page in the large-capacity on-chip RAM.

When a VRAMWEn (n = 0 to 4) bit is set to 1, writing to page n is enabled. When a VRAMWEn bit is cleared to 0, writing to page n is ignored. The initial value of a VRAMWEn bit is 1.

SYSCR4 should be set with a program located in an area other than the large-capacity on-chip RAM. Furthermore, an instruction to read SYSCR4 should be located immediately after the instruction to write to SYSCR4. If not, normal access is not guaranteed.

Note: When writing to this register, see section 32.4, Usage Notes.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	VRAMWE4	VRAMWE3	VRAMWE2	VRAMWE1	VRAMWE0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
4	VRAMWE4	1	R/W	RAM Write Enable 4 (corresponding area: page 4* in large-capacity on-chip RAM) 0: Writing to page 4 is disabled. 1: Writing to page 4 is enabled.
3	VRAMWE3	1	R/W	RAM Write Enable 3 (corresponding area: page 3* in large-capacity on-chip RAM) 0: Writing to page 3 is disabled. 1: Writing to page 3 is enabled.

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
Direct memory access controller	RDMATCR_10	—	—	—	—	—	—	—	—
	SAR_11								
	DAR_11								
	DMATCR_11	—	—	—	—	—	—	—	—
	CHCR_11	TC	—	RLDSAR	RLDDAR	—	DAF	SAF	—
		—	—	—	TEMASK	HE	HIE	—	—
		DM[1]	DM[0]	SM[1]	SM[0]	RS[3]	RS[2]	RS[1]	RS[0]
		—	—	TB	TS[1]	TS[0]	IE	TE	DE
	RSAR_11								
	RDAR_11								

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
IEBus controller	IERBFL	RBFL[7]	RBFL[6]	RBFL[5]	RBFL[4]	RBFL[3]	RBFL[2]	RBFL[1]	RBFL[0]
	IELA1	ILAL8[7]	ILAL8[6]	ILAL8[5]	ILAL8[4]	ILAL8[3]	ILAL8[2]	ILAL8[1]	ILAL8[0]
	IELA2	—	—	—	—	ILAU4[3]	ILAU4[2]	ILAU4[1]	ILAU4[0]
	IEFLG	CMX	MRQ	SRQ	SRE	LCK	—	RSS	GG
	IETSR	—	TXS	TXF	—	TXEAL	TXETTME	TXERO	TXEACK
	IEIET	—	TXSE	TXFE	—	TXEALE	TXETTMEE	TXEROE	TXEACKE
	IERSR	RXBSY	RXS	RXF	RXEDE	RXEOVE	RXERTME	RXEDLE	RXEPE
	IEIER	RXBSYE	RXSE	RXFE	RXEDEE	RXEOVEE	RXERTMEE	RXEDLEE	RXEPEE
	IECKSR	—	—	—	CKS3	—	CKS[2]	CKS[1]	CKS[0]
	IETB001 to IETB128								
	IERB001 to IERB128								
Renesas SPDIF interface	TLCA	—	—	—	—	—	—	—	—
	TRCA	—	—	—	—	—	—	—	—
	TLCS	—	—	CLAC[1]	CLAC[0]	FS[3]	FS[2]	FS[1]	FS[0]
		CHNO[3]	CHNO[2]	CHNO[1]	CHNO[0]	SRCNO[3]	SRCNO[2]	SRCNO[1]	SRCNO[0]
		CATCD[7]	CATCD[6]	CATCD[5]	CATCD[4]	CATCD[3]	CATCD[2]	CATCD[1]	CATCD[0]
		—	—	CTL[4]	CTL[3]	CTL[2]	CTL[1]	CTL[0]	—
	TRCS	—	—	CLAC[1]	CLAC[0]	FS[3]	FS[2]	FS[1]	FS[0]
		CHNO[3]	CHNO[2]	CHNO[1]	CHNO[0]	SRCNO[3]	SRCNO[2]	SRCNO[1]	SRCNO[0]
		CATCD[7]	CATCD[6]	CATCD[5]	CATCD[4]	CATCD[3]	CATCD[2]	CATCD[1]	CATCD[0]
		—	—	CTL[4]	CTL[3]	CTL[2]	CTL[1]	CTL[0]	—