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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, SCI, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	73
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.3M x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s726a2d216fp-v0

Contents

SH726A Pin No.	SH726B Pin No.	Function 1		Function 2		Function 3		Function 4	
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
13	16	PB7	I(s)/O	A7	O	RxD0	I(s)	—	—
14	17	PB8	I(s)/O	A8	O	TxD0	O	—	—
15	18	PB9	I(s)/O	A9	O	SCK1	I(s)/O	SSIWS2	I(s)/O
NC	19	PJ8	I(s)/O	TIOC3A	I(s)/O	A23	O	SCK2	I(s)/O
NC	20	PJ9	I(s)/O	TIOC3B	I(s)/O	A24	O	RxD2	I(s)
NC	21	PJ10	I(s)/O	TIOC3C	I(s)/O	A25	O	TxD2	O
16	22	PVcc							
17	23	PB10	I(s)/O	A10	O	RxD1	I(s)	—	—
18	24	Vss							
19	25	PB11	I(s)/O	A11	O	TxD1	O	—	—
20	26	Vcc							
21	27	PB12	I(s)/O	A12	O	SCK2	I(s)/O	SSIDATA2	I(s)/O
22	28	PB13	I(s)(5t)/O	A13	O	RxD2	I(s)(5t)	—	—
23	29	PB14	I(s)/O	A14	O	TxD2	O	—	—
24	30	PB15	I(s)/O	A15	O	RSPCK0	I(s)/O	TIOC0B	I(s)/O

SH726A Pin No.	SH726B Pin No.	Function 5		Function 6		Function 7		ASE Function		Circuit diagram Figure 1.3
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
13	16	—	—	—	—	—	—	—	—	(7)
14	17	—	—	—	—	—	—	—	—	(7)
15	18	—	—	—	—	—	—	—	—	(7)
NC	19	SSISCK2	I(s)/O	TEND0	O	—	—	—	—	(7)
NC	20	SSIWS2	I(s)/O	DREQ0	I(s)	—	—	—	—	(7)
NC	21	SSIDATA2	I(s)/O	DACK0	O	—	—	—	—	(7)
16	22									
17	23	—	—	—	—	—	—	—	—	(7)
18	24									
19	25	—	—	—	—	—	—	—	—	(7)
20	26									
21	27	—	—	—	—	—	—	—	—	(7)
22	28	—	—	—	—	—	—	—	—	(7)
23	29	—	—	—	—	—	—	—	—	(7)
24	30	—	—	—	—	—	—	—	—	(7)

Bit	Bit Name	Initial Value	R/W	Description
10 to 7	W[3:0]	1010	R/W	Number of Access Wait Cycles Specify the number of wait cycles to be inserted in the first access cycle. 0000: No cycle 0001: 1 cycle 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles 0101: 5 cycles 0110: 6 cycles 0111: 8 cycles 1000: 10 cycles 1001: 12 cycles 1010: 14 cycles 1011: 18 cycles 1100: 24 cycles 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)
6	WM	0	R/W	External Wait Mask Specification Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycle is 0. 0: External wait input is valid 1: External wait input is ignored
5 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

10.5 Operation

10.5.1 Endian/Access Size and Data Alignment

This LSI supports both big endian, in which the most significant byte (MSB) of data is that in the direction of the 0th address, and little endian, in which the least significant byte (LSB) is that in the direction of the 0th address. In the initial state after a power-on reset, all areas will be in big endian mode. Endian mode can be changed by setting the CSnBCR register as long as the target space is not being accessed.

Data bus width can be selected from 8 bits and 16 bits for the normal memory and SRAM with byte selection. It is fixed to 16 bits for SDRAM.

Endian specification and data bus width varies depending on boot mode. For details, refer to section 10.3.2, Data Bus Width and Endian Specification for Each Area Depending on Boot Mode and Settings of Pins Related to This Module.

Data alignment is performed in accordance with the data bus width selected for the device. This also means that four read operations are required to read longword data from a byte-width device. In this LSI, data alignment and conversion of data length is performed automatically between the respective interfaces.

Tables 10.5 to 10.8 show the relationship between device data width and access unit. Note that the correspondence between addresses and strobe signals for the 16-bit bus width depends on the endian setting. For example, with big endian and a 16-bit bus width, $\overline{WE1}$ corresponds to the 0th address, which is represented by $\overline{WE0}$ when little endian has been selected.

Since instructions are fetched with both 32- and 16-bit accesses, their alignment in the little-endian area is difficult. Execute instructions from big-endian area.

Table 10.10 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (2)-2

Setting				
BSZ [1:0]	**A2/3 ROW [1:0]**	**A2/3 COL [1:0]**		
10 (16 bits)	**01 (12 bits)**	**10 (10 bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A27	A17		Unused
A16	A26	A16		
A15	A25	A15		
A14	A24*2	A24*2	A13 (BA1)	Specifies bank
A13	A23*2	A23*2	A12 (BA0)	
A12	A22	A12	A11	Address
A11	A21	L/H*1	A10/AP	Specifies address/precharge
A10	A20	A10	A9	Address
A9	A19	A9	A8	
A8	A18	A8	A7	
A7	A17	A7	A6	
A6	A16	A6	A5	
A5	A15	A5	A4	
A4	A14	A4	A3	
A3	A13	A3	A2	
A2	A12	A2	A1	
A1	A11	A1	A0	
A0	A10	A0		Unused
Example of connected memory				
256-Mbit product (4 Mwords × 16 bits × 4 banks, column 10 bits product): 1				

Notes: 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
2. Bank address specification

11.3.3 DMA Transfer Count Registers (DMATCR)

The DMA transfer count registers (DMATCR) are 32-bit readable/writable registers that specify the number of DMA transfers. The transfer count is 1 when the setting is H'00000001, 16,777,215 when H'00FFFFFF is set, and 16,777,216 (the maximum) when H'00000000 is set. During a DMA transfer, these registers indicate the remaining transfer count.

The upper eight bits of DMATCR are always read as 0, and the write value should always be 0. To transfer data in 16 bytes, one 16-byte transfer (128 bits) counts one.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

11.3.4 DMA Channel Control Registers (CHCR)

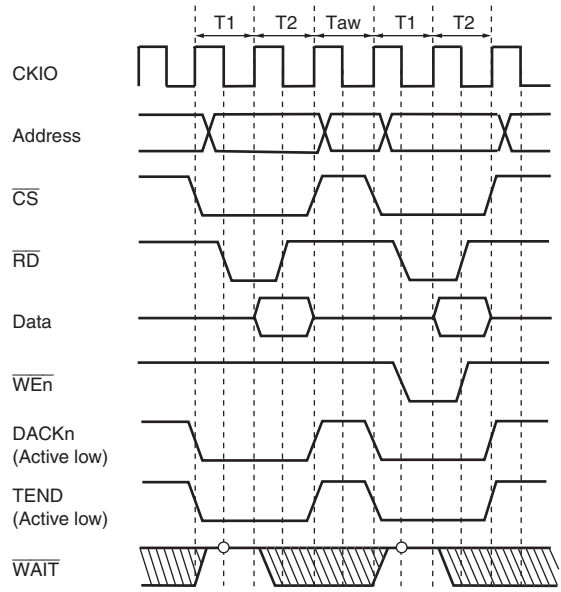
The DMA channel control registers (CHCR) are 32-bit readable/writable registers that control the DMA transfer mode.

The DO, AM, AL, DL, DS, and TL bits which specify the DREQ, DACK, and TEND external pin functions can be read and written to in channel 0, but they are reserved in channels 1 to 15.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TC	-	RLD SAR	RLD DAR	-	DAF	SAF	-	DO	TL	-	TE MASK	HE	HIE	AM	AL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R	R/W	R/W	R	R/W	R/W	R	R/W	R/(W)*	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DM[1:0]		SM[1:0]		RS[3:0]				DL	DS	TB	TS[1:0]		IE	TE	DE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/(W)*	R/W

Note: * Only 0 can be written to clear the flag after 1 is read.



Note: TEND is asserted for the last unit of DMA transfer. If a transfer unit is divided into multiple bus cycles and the CS is negated between the bus cycles, TEND is also divided.

Figure 11.16 Bus State Controller Normal Memory Access (No Wait, Idle Cycle 1, Longword Access to 16-Bit Device)

Table 12.44 PWM Output Registers and Output Pins

		Output Pins	
Channel	**Registers**	**PWM Mode 1**	**PWM Mode 2**
0	TGRA_0	TIOC0A	TIOC0A
	TGRB_0		TIOC0B
	TGRC_0	TIOC0C	TIOC0C
	TGRD_0		TIOC0D
1	TGRA_1	TIOC1A	TIOC1A
	TGRB_1		TIOC1B
2	TGRA_2	TIOC2A	TIOC2A
	TGRB_2		TIOC2B
3	TGRA_3	TIOC3A	Cannot be set
	TGRB_3		Cannot be set
	TGRC_3	TIOC3C	Cannot be set
	TGRD_3		Cannot be set
4	TGRA_4	TIOC4A	Cannot be set
	TGRB_4		Cannot be set
	TGRC_4	TIOC4C	Cannot be set
	TGRD_4		Cannot be set

Note: In PWM mode 2, PWM output is not possible for the TGR register in which the period is set.

(26) Operation when Error Occurs during Reset-Synchronized PWM Mode Operation, and Operation is Restarted in Normal Mode

Figure 12.140 shows an explanatory diagram of the case where an error occurs in reset-synchronized PWM mode and operation is restarted in normal mode after re-setting.

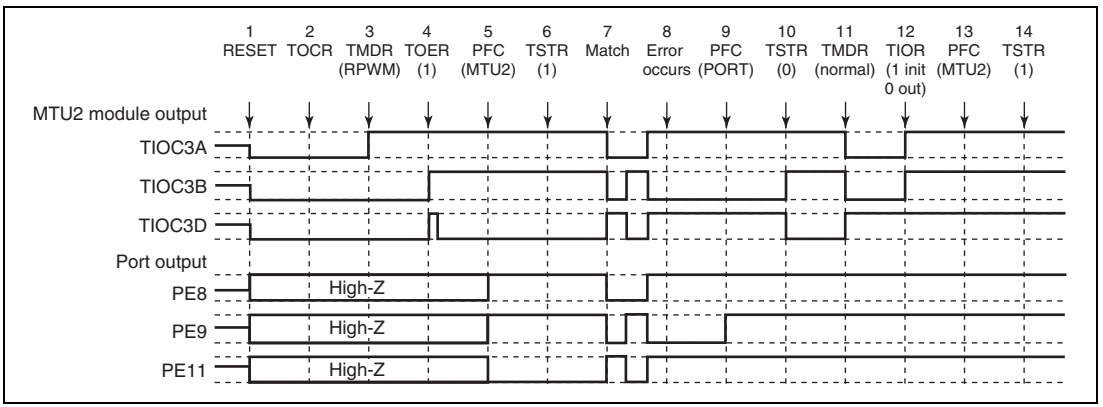


Figure 12.140 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Normal Mode

1. After a reset, the module output is low and ports are in the high-impedance state.
2. Select the reset-synchronized PWM output level and cyclic output enabling/disabling with TOCR.
3. Set reset-synchronized PWM.
4. Enable channel 3 and 4 output with TOER.
5. Set the multi-function timer pulse unit 2 output with the general I/O port.
6. The count operation is started by TSTR.
7. The reset-synchronized PWM waveform is output on compare-match occurrence.
8. An error occurs.
9. Set port output with the general I/O port and output the inverse of the active level.
10. The count operation is stopped by TSTR. (This module outputs the same value as the reset-synchronized PWM output initial value.)
11. Set normal mode. (The positive phase output from this module is low, and negative phase output is high.)
12. Initialize the pins with TIOR.
13. Set the multi-function timer pulse unit 2 output with the general I/O port.
14. Operation is restarted by TSTR.

(2) Data Enable

In external address space read mode, transfer enable or disable of the command, optional command, address, and option data can be controlled with the CDE, OCDE, ADE[3:0], and OPDE[3:0] bits in DRENR, respectively. Similarly, in SPI operating mode, enable or disable of the command, optional command, address, option data, and transfer data can be controlled with the CDE, OCDE, ADE[3:0], OPDE[3:0], and SPIDE[3:0] bits in SMENR, respectively. However, disabling all the above parameters is prohibited in SPI operating mode. At least one of them must be enabled. For the address and option data in external address space read mode; and the address, option data, and transfer data in SPI operating mode, the enable bit setting allowed is determined according to the transfer data size. For the allowed setting combinations of the enable bits and transfer data size, refer to the description of the pertinent register.

If data is disabled, that data is skipped, and input and output of the next data is carried out. The command, optional command, address, and option data are always output. In external address space read mode, data is always input; and in SPI operating mode, input and output of data is determined based on the settings of the SPIRE and SPIWE bits in SMCR.

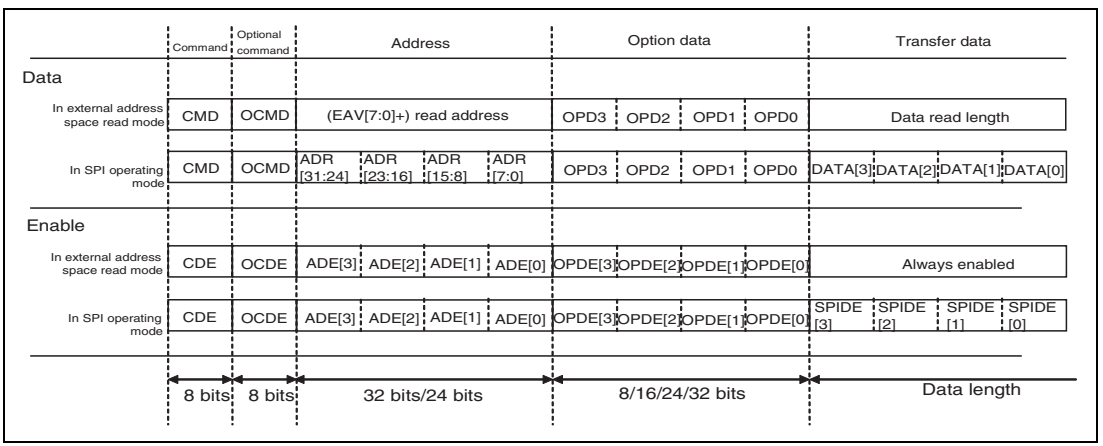
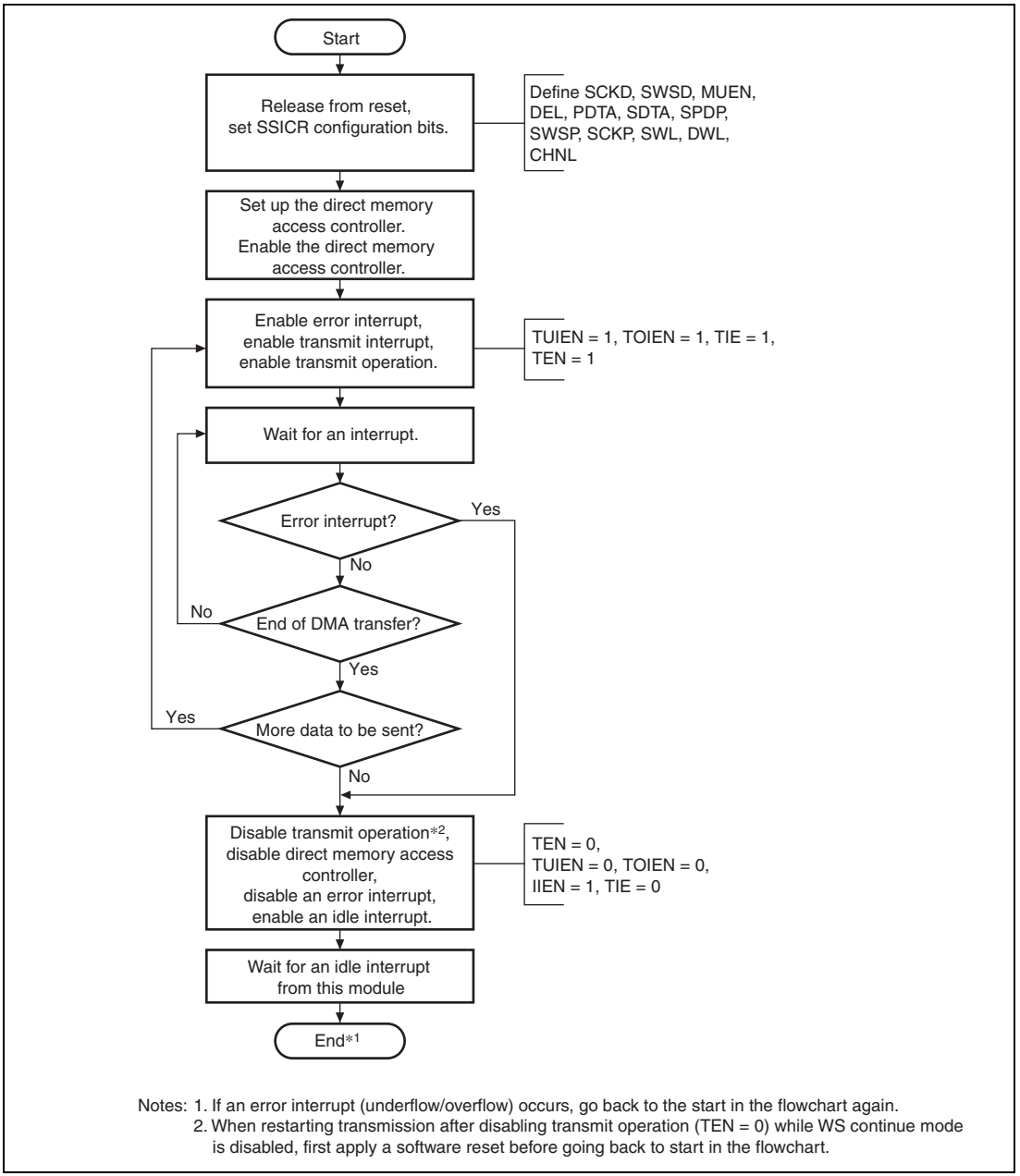


Figure 18.17 Data and Enable

Bit	Bit Name	Initial Value	R/W	Description
5	MST	0	R/W	Master/Slave Select
4	TRS	0	R/W	Transmit/Receive Select In master mode with the I²C bus format, when arbitration is lost, MST and TRS are both reset by hardware, causing a transition to slave receive mode. Modification of the TRS bit should be made between transfer frames. When seven bits after the start condition is issued in slave receive mode match the slave address set to SAR and the 8th bit is set to 1, TRS is automatically set to 1. If an overrun error occurs in master receive mode with the clocked synchronous serial format, MST is cleared and the mode changes to slave receive mode. Operating modes are described below according to MST and TRS combination. When clocked synchronous serial format is selected and MST = 1, clock is output. 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode
3 to 0	CKS[3:0]	0000	R/W	Transfer Clock Select These bits should be set according to the necessary transfer rate (table 19.3) in master mode.

(1) Transmission Using Direct Memory Access Controller



Notes: 1. If an error interrupt (underflow/overflow) occurs, go back to the start in the flowchart again.
2. When restarting transmission after disabling transmit operation (TEN = 0) while WS continue mode is disabled, first apply a software reset before going back to start in the flowchart.

Figure 20.23 Transmission Using Direct Memory Access Controller

24.3 Functional Block Diagram

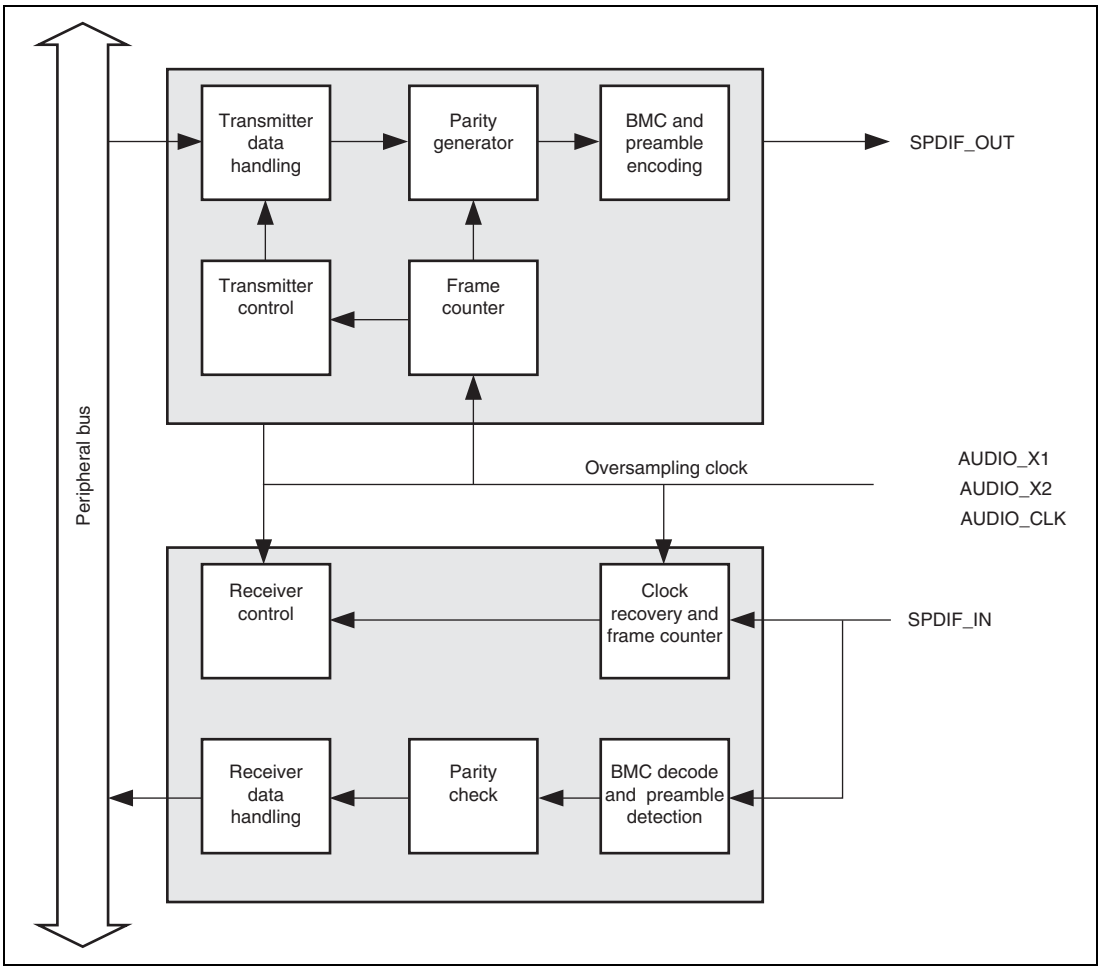


Figure 24.2 Functional Block Diagram

25.3.26 Pre-ECC Correction Subheader: Channel Number (Byte 21) Data Register (SHEAD05)

The pre-ECC correction subheader: channel number (byte 21) data register (SHEAD05) indicates the channel number value in the subheader before ECC correction (byte 21).

Bit:	7	6	5	4	3	2	1	0
	SHEAD05[7:0]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SHEAD05 [7:0]	All 0	R	Indicate channel number value in the subheader before ECC correction (byte 21). For sectors not in Mode 2, this register contains the byte of data at the corresponding position.

25.3.27 Pre-ECC Correction Subheader: Sub-Mode (Byte 22) Data Register (SHEAD06)

The pre-ECC correction subheader: sub-mode (byte 22) data register (SHEAD06) indicates the sub-mode value in the subheader before ECC correction (byte 22).

Bit:	7	6	5	4	3	2	1	0
	SHEAD06[7:0]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SHEAD06 [7:0]	All 0	R	Sub-Mode Value in Subheader Before ECC Correction (Byte 22) For sectors not in Mode 2, this register contains the byte of data at the corresponding position.

(5) Control Transfer Stage Transition Interrupt

Figure 27.7 shows a diagram of how this module handles the control transfer stage transition. This module controls the control transfer sequence and generates control transfer stage transition interrupts. Control transfer stage transition interrupts can be enabled or disabled individually using INTENB0. The transfer stage that made a transition can be confirmed using the CTSQ bit in INTSTS0.

The control transfer stage transition interrupts are generated only when the function controller function is selected.

The control transfer sequence errors are described below. If an error occurs, the PID bit in DCPCTR is set to B'1x (STALL).

1. During control read transfers
- At the IN token of the data stage, an OUT token is received when there have been no data transfers at all.
- An IN token is received at the status stage
- A packet is received at the status stage for which the data packet is DATAPID = DATA0

2. During control write transfers
- At the OUT token of the data stage, an IN token is received when there have been no ACK response at all
- A packet is received at the data stage for which the first data packet is DATAPID = DATA0
- At the status stage, an OUT token is received

3. During no-data control transfers
- At the status stage, an OUT token is received

At the control write transfer stage, if the number of receive data exceeds the wLength value of the USB request, it cannot be recognized as a control transfer sequence error. At the control read transfer status stage, packets other than zero-length packets are received by an ACK response and the transfer ends normally.

When a CTRT interrupt occurs in response to a sequence error, the CTSQ = 110 value is retained until CTRT = 0 is written from the system (the interrupt status is cleared). Therefore, while CTSQ = 110 is being held, the CTRT interrupt that ends the setup stage will not be generated even if a new USB request is received. (This module retains the setup stage end, and after the interrupt status has been cleared, a CTRT interrupt is generated.)

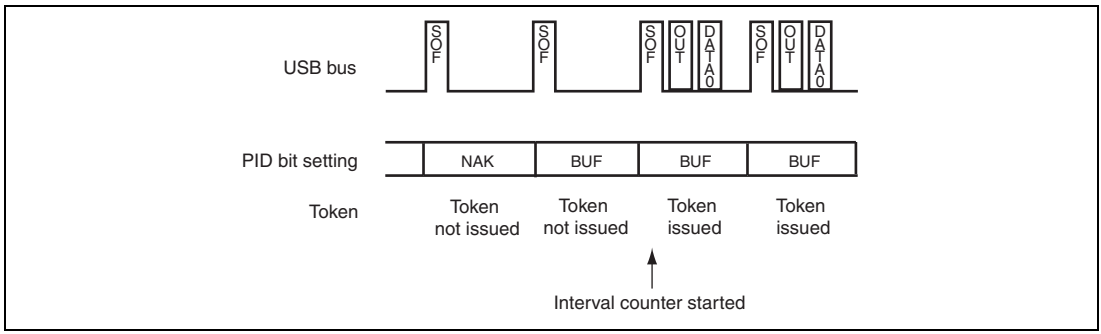


Figure 27.8 Token Issuance when IITV = 0

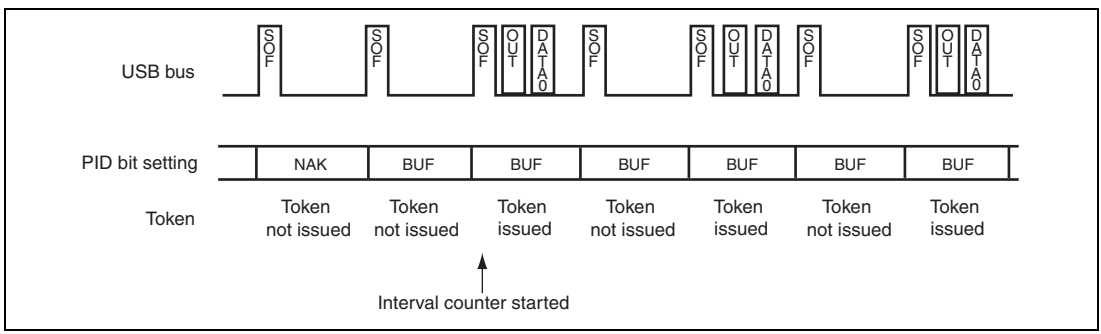


Figure 27.9 Token Issuance when IITV = 1

31.2.2 I/O Registers

I/O registers are used to set the pins on each port as inputs or outputs. Table 31.13 shows pins corresponding to each bit. All the bits shown in table 31.14 are reserved.

I/O registers are enabled when the pin function is general I/O or TIOC I/O of the multifunction timer pulse unit 2. They are disabled in the other cases. If a bit in I/O register is set to 1, the corresponding pin function is output. If it is cleared to 0, the corresponding pin function is input.

Table 31.13 Pins corresponding to Each Bit in I/O Registers

Register Name	Abbreviation	Bit	Bit Name	Corresponding Pin
Port A I/O register 0	PAIOR0	8	PA1IOR	PA1
		0	PA0IOR	PA0
Port B I/O register 1	PBIOR1	6 to 0	PB22IOR to PB16IOR	PB22 to PB16
Port B I/O register 0	PBIOR0	15 to 1	PB15IOR to PB1IOR	PB15 to PB1
Port C I/O register 0	PCIOR0	8 to 0	PC8IOR to PC0IOR	PC8 to PC0
Port D I/O register 0	PDIOR0	15 to 0	PD15IOR to PD0IOR	PD15 to PD0
Port E I/O register 0	PEIOR0	7 to 0	PE7IOR to PE0IOR	PE7 to PE0
Port F I/O register 0	PFIOR0	7 to 0	PF7IOR to PF0IOR	PF7 to PF0
Port J I/O register 0	PJIOR0	14 to 0	PJ14IOR to PJ0IOR	PJ14 to PJ0
Port K I/O register 0	PKIOR0	1, 0	PK1IOR, PK0IOR	PK1, PK0

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
USB 2.0 host/function module	Pipe 5 control register	PIPE5CTR	16	H'FFFFC078	16
	Pipe 6 control register	PIPE6CTR	16	H'FFFFC07A	16
	Pipe 7 control register	PIPE7CTR	16	H'FFFFC07C	16
	Pipe 8 control register	PIPE8CTR	16	H'FFFFC07E	16
	Pipe 9 control register	PIPE9CTR	16	H'FFFFC080	16
	Pipe 1 transaction counter enable register	PIPE1TRE	16	H'FFFFC090	16
	Pipe 1 transaction counter register	PIPE1TRN	16	H'FFFFC092	16
	Pipe 2 transaction counter enable register	PIPE2TRE	16	H'FFFFC094	16
	Pipe 2 transaction counter register	PIPE2TRN	16	H'FFFFC096	16
	Pipe 3 transaction counter enable register	PIPE3TRE	16	H'FFFFC098	16
	Pipe 3 transaction counter register	PIPE3TRN	16	H'FFFFC09A	16
	Pipe 4 transaction counter enable register	PIPE4TRE	16	H'FFFFC09C	16
	Pipe 4 transaction counter register	PIPE4TRN	16	H'FFFFC09E	16
	Pipe 5 transaction counter enable register	PIPE5TRE	16	H'FFFFC0A0	16
	Pipe 5 transaction counter register	PIPE5TRN	16	H'FFFFC0A2	16
	Device address 0 configuration register	DEVADD0	16	H'FFFFC0D0	16
	Device address 1 configuration register	DEVADD1	16	H'FFFFC0D2	16
	Device address 2 configuration register	DEVADD2	16	H'FFFFC0D4	16
	Device address 3 configuration register	DEVADD3	16	H'FFFFC0D6	16
	Device address 4 configuration register	DEVADD4	16	H'FFFFC0D8	16
	Device address 5 configuration register	DEVADD5	16	H'FFFFC0DA	16
Sampling rate converter	Input data register_0	SRCID_0	32	H'FFFE7000	16, 32
	Output data register_0	SRCOD_0	32	H'FFFE7004	16, 32
	Input data control register_0	SRCIDCTRL_0	16	H'FFFE7008	16
	Output data control register_0	SRCODCTRL_0	16	H'FFFE700A	16
	Control register_0	SRCCTRL_0	16	H'FFFE700C	16
	Status register_0	SRCSTAT_0	16	H'FFFE700E	16
	Input data register_1	SRCID_1	32	H'FFFE7800	16, 32
	Output data register_1	SRCOD_1	32	H'FFFE7804	16, 32
	Input data control register_1	SRCIDCTRL_1	16	H'FFFE7808	16
	Output data control register_1	SRCODCTRL_1	16	H'FFFE780A	16

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
IEBus controller	IERBFL	RBFL[7]	RBFL[6]	RBFL[5]	RBFL[4]	RBFL[3]	RBFL[2]	RBFL[1]	RBFL[0]
	IELA1	ILAL8[7]	ILAL8[6]	ILAL8[5]	ILAL8[4]	ILAL8[3]	ILAL8[2]	ILAL8[1]	ILAL8[0]
	IELA2	—	—	—	—	ILAU4[3]	ILAU4[2]	ILAU4[1]	ILAU4[0]
	IEFLG	CMX	MRQ	SRQ	SRE	LCK	—	RSS	GG
	IETSR	—	TXS	TXF	—	TXEAL	TXETTME	TXERO	TXEACK
	IEIET	—	TXSE	TXFE	—	TXEALE	TXETTMEE	TXEROE	TXEACKE
	IERSR	RXBSY	RXS	RXF	RXEDE	RXEOVE	RXERTME	RXEDLE	RXEPE
	IEIER	RXBSYE	RXSE	RXFE	RXEDEE	RXEOVEE	RXERTMEE	RXEDLEE	RXEPEE
	IECKSR	—	—	—	CKS3	—	CKS[2]	CKS[1]	CKS[0]
	IETB001 to IETB128								
	IERB001 to IERB128								
Renesas SPDIF interface	TLCA	—	—	—	—	—	—	—	—
	TRCA	—	—	—	—	—	—	—	—
	TLCS	—	—	CLAC[1]	CLAC[0]	FS[3]	FS[2]	FS[1]	FS[0]
		CHNO[3]	CHNO[2]	CHNO[1]	CHNO[0]	SRCNO[3]	SRCNO[2]	SRCNO[1]	SRCNO[0]
		CATCD[7]	CATCD[6]	CATCD[5]	CATCD[4]	CATCD[3]	CATCD[2]	CATCD[1]	CATCD[0]
		—	—	CTL[4]	CTL[3]	CTL[2]	CTL[1]	CTL[0]	—
	TRCS	—	—	CLAC[1]	CLAC[0]	FS[3]	FS[2]	FS[1]	FS[0]
		CHNO[3]	CHNO[2]	CHNO[1]	CHNO[0]	SRCNO[3]	SRCNO[2]	SRCNO[1]	SRCNO[0]
		CATCD[7]	CATCD[6]	CATCD[5]	CATCD[4]	CATCD[3]	CATCD[2]	CATCD[1]	CATCD[0]
		—	—	CTL[4]	CTL[3]	CTL[2]	CTL[1]	CTL[0]	—

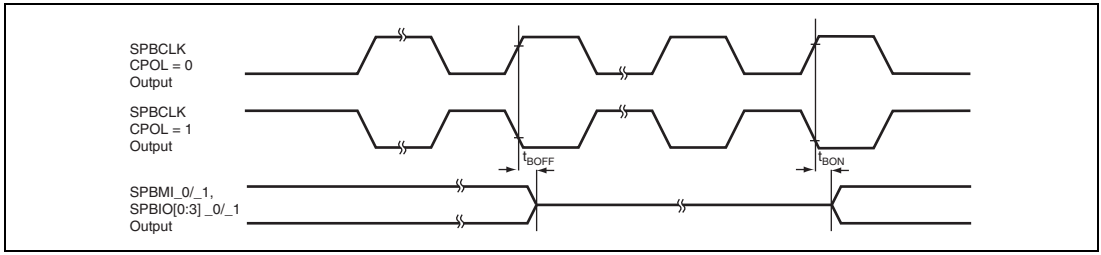


Figure 35.48 Buffer On/Off Timing (CPHAT = 1, CPHAR = 1)