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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	EBI/EMI, I²C, IEBus, SCI, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	73
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.3M x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s726a2p216fp-vz

General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.
The NC (not connected) pins are either not connected to any of the internal circuitry or are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.
Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test registers may have been be allocated to these addresses. Do not access these registers; the system's operation is not guaranteed if they are accessed.

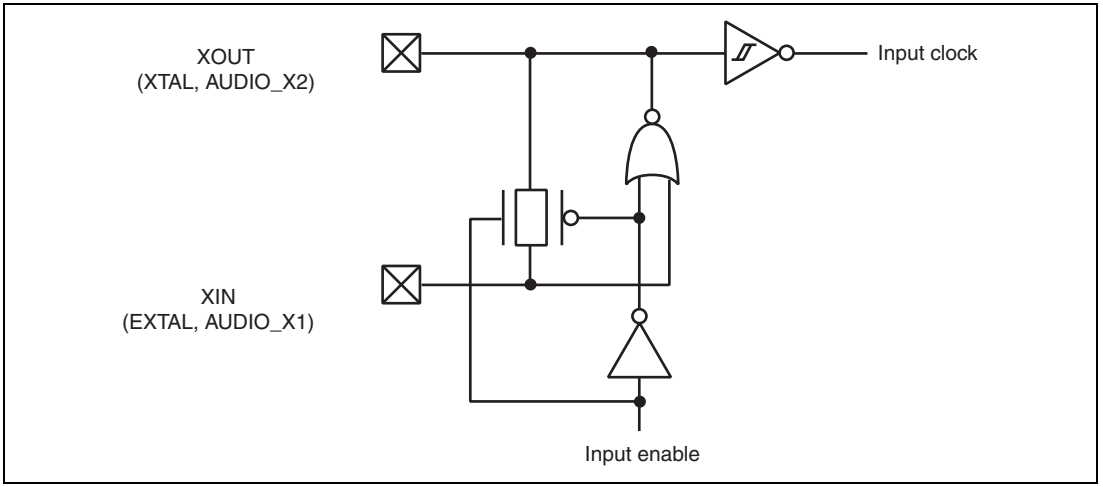

Figure 1.3 (10) Simplified Circuit Diagram (Oscillation Buffer 1)

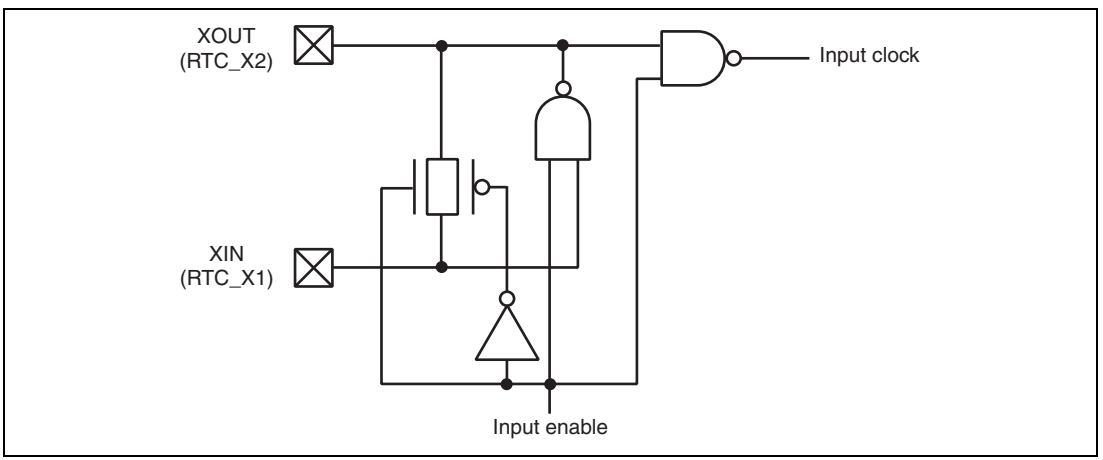

Figure 1.3 (11) Simplified Circuit Diagram (Oscillation Buffer 2)

10.3 Area Overview

10.3.1 Address Map

In the architecture, this LSI has a 32-bit address space, which is divided into cache-enabled, cache-disabled, and on-chip spaces (on-chip RAM, on-chip peripheral modules, and reserved areas) according to the upper bits of the address.

External address spaces CS0 to CS4 are cache-enabled when internal address A29 = 0 or cache-disabled when A29 = 1.

The kind of memory to be connected and the data bus width are specified in each partial space. The address map for the external address space is listed below.

Table 10.2 Address Map

Internal Address	Space	Memory to be Connected	Cache
H'00000000 to H'03FFFFFF	CS0	Normal space, SRAM with byte selection, burst ROM (asynchronous or synchronous)	Cache-enabled
H'04000000 to H'07FFFFFF	CS1*2	Normal space, SRAM with byte selection	
H'08000000 to H'0BFFFFFF	CS2*2	Normal space, SRAM with byte selection, SDRAM	
H'0C000000 to H'0FFFFFFF	CS3	Normal space, SRAM with byte selection, SDRAM	
H'10000000 to H'13FFFFFF	CS4*2	Normal space, SRAM with byte selection, burst ROM (asynchronous)	
H'14000000 to H'1FFFFFFF	Other	SPI multi I/O bus space, on-chip RAM, reserved area*1	
H'20000000 to H'23FFFFFF	CS0	Normal space, SRAM with byte selection, burst ROM (asynchronous or synchronous)	Cache-disabled
H'24000000 to H'27FFFFFF	CS1*2	Normal space, SRAM with byte selection	
H'28000000 to H'2BFFFFFF	CS2*2	Normal space, SRAM with byte selection, SDRAM	
H'2C000000 to H'2FFFFFFF	CS3	Normal space, SRAM with byte selection, SDRAM	
H'30000000 to H'33FFFFFF	CS4*2	Normal space, SRAM with byte selection, burst ROM (asynchronous)	

Bit	Bit Name	Initial Value	R/W	Description
10 to 7	W[3:0]	1010	R/W	Number of Access Wait Cycles Specify the number of wait cycles to be inserted in the first access cycle. 0000: No cycle 0001: 1 cycle 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles 0101: 5 cycles 0110: 6 cycles 0111: 8 cycles 1000: 10 cycles 1001: 12 cycles 1010: 14 cycles 1011: 18 cycles 1100: 24 cycles 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)
6	WM	0	R/W	External Wait Mask Specification Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycle is 0. 0: External wait input is valid 1: External wait input is ignored
5 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	HW[1:0]	00	R/W	Delay Cycles from $\overline{RD}$, $\overline{WEn}$ Negation to Address, $\overline{CS4}$ Negation Specify the number of delay cycles from $\overline{RD}$ and $\overline{WEn}$ negation to address and $\overline{CS4}$ negation. 00: 0.5 cycles 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles

Table 12.23 TIORH_3 (Channel 3)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_3 Function**	**TIOC3A Pin Function**
0	0	0	0	Output compare register	Output retained*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	X	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges

[Legend]

X: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

(2) Examples of Buffer Operation

(a) When TGR is an output compare register

Figure 12.17 shows an operation example in which PWM mode 1 has been designated for channel 0, and buffer operation has been designated for TGRA and TGRC. The settings used in this example are TCNT clearing by compare match B, 1 output at compare match A, and 0 output at compare match B. In this example, the TTSA bit in TBTM is cleared to 0.

As buffer operation has been set, when compare match A occurs the output changes and the value in buffer register TGRC is simultaneously transferred to timer general register TGRA. This operation is repeated each time that compare match A occurs.

For details of PWM modes, see section 12.4.5, PWM Modes.

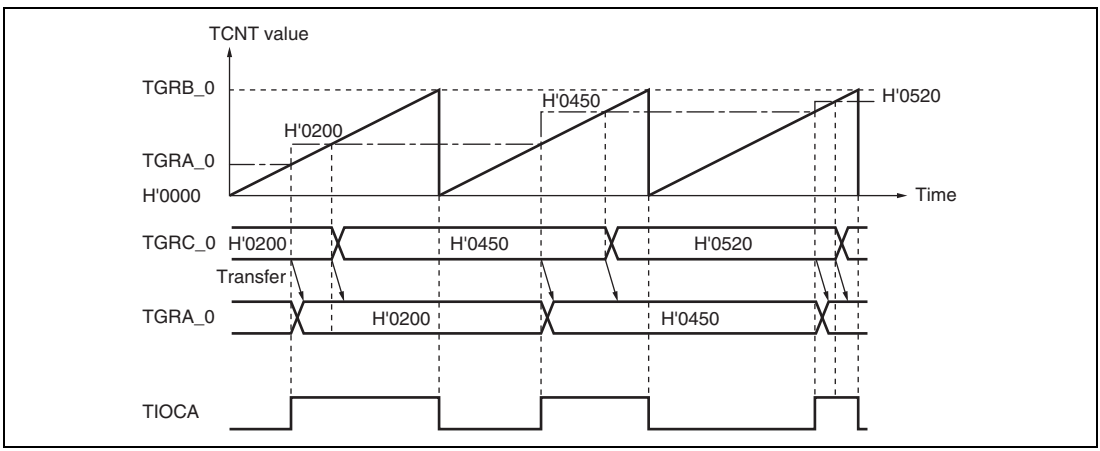

Figure 12.17 Example of Buffer Operation (1)

(b) When TGR is an input capture register

Figure 12.18 shows an operation example in which TGRA has been designated as an input capture register, and buffer operation has been designated for TGRA and TGRC.

Counter clearing by TGRA input capture has been set for TCNT, and both rising and falling edges have been selected as the TIOCA pin input capture input edge.

As buffer operation has been set, when the TCNT value is stored in TGRA upon the occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC.

15.3.4 Hour Counter (RHRCNT)

RHRCNT is used for setting/counting in the BCD-coded hour section. The count operation is performed by a carry for each 1 hour of the minute counter.

The assignable range is from 00 through 23 (practically in BCD), otherwise operation errors occur. Carry out write processing after stopping the count operation through the setting of the START bit in RCR2.

Bit:	7	6	5	4	3	2	1	0
	-	-	10 hours		1 hour			
Initial value:	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	10 hours	Undefined	R/W	Counting Ten's Position of Hours Counts on 0 to 2 for ten's position of hours.
3 to 0	1 hour	Undefined	R/W	Counting One's Position of Hours Counts on 0 to 9 once per hour. When a carry is generated, 1 is added to the ten's position.

15.3.6 Date Counter (RDAYCNT)

RDAYCNT is used for setting/counting in the BCD-coded date section. The count operation is performed by a carry for each day of the hour counter.

The assignable range is from 01 through 31 (practically in BCD), otherwise operation errors occur. Carry out write processing after stopping the count operation through the setting of the START bit in RCR2.

The range of date changes with each month and in leap years. Confirm the correct setting. Leap years are recognized by dividing the year counter (RYRCNT) values by 400, 100, and 4 and obtaining a fractional result of 0.

Bit:	7	6	5	4	3	2	1	0
	-	-	10 days		1 day			
Initial value:	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	10 days	Undefined	R/W	Counting Ten's Position of Dates
3 to 0	1 day	Undefined	R/W	Counting One's Position of Dates Counts on 0 to 9 once per date. When a carry is generated, 1 is added to the ten's position.

17.3.4 Status Register (SPSR)

SPSR indicates the operating status.

Bit:	7	6	5	4	3	2	1	0
	SPRF	TEND	SPTEF	—	—	MODF	—	OVRF
Initial value:	0	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R/(W)*	R	R/(W)*

Note: * Only 0 can be written to clear the flag after reading 1.

Bit	Bit Name	Initial Value	R/W	Description
7	SPRF	0	R	Receive Buffer Full Flag Indicates that the number of receive data units in the receive buffer (SPRX) is equal to or greater than the receive buffer data triggering number specified in the buffer control register (SPBFCR). 0: The number of receive data units in the receive buffer is less than the receive buffer data triggering number. 1: The number of receive data units in the receive buffer is equal to or greater than the receive buffer data triggering number. [Clearing conditions] • The receive buffer data is read until the number of data units in the receive buffer becomes less than the specified receive buffer data triggering number. • Receive buffer data reset is enabled. • Power-on reset [Setting condition] • The number of data units in the receive buffer is equal to or greater than the specified receive buffer data triggering number.

18.4.4 Data Read Control Register (DRCR)

DRCR is a 32-bit register that sets the operation in external address space read mode.

The bits except the SSLN bit should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	SSLN	-	-	-	-	RBURST[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	W	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	RCF	RBE	-	-	-	-	-	-	-	SSLE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	W	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	SSLN	0	W	SPBSSL Negation Asserted SPBSSL can be negated by writing 1 to this bit when both the RBE and SSLE bits are 1. This bit is always read as 0. Note: To start next access after SPBSSL negation using this bit, read SSLF in CMNSR = 0 to confirm that the SPBSSL has been negated.
23 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

18.5.10 Data Format

This module can input and output data in the order of command, optional command, address, option data, and data.

(1) Data Registers

Table 18.6 shows the input and output data.

Table 18.6 Data Registers

Data		External Address Space Read Operation	SPI Operation
Command (8 bits)		CMD[7:0] bits in DRCMR	CMD[7:0] bits in SMCMR
Optional command (8 bits)		OCMD[7:0] bits in DRCMR	OCMD[7:0] bits in SMCMR
Address (32/24 bits)	BSZ[1:0] = 00 (one flash memory connected)	32 bits: DREAR.EAV[6:1 to 0] bits + lower [25 to 24:0] bits of the read address. 24 bits: Lower [23:0] bits of the read address	32 bits: ADR[31:0] bits in SMADR 24 bits: ADR[23:0] bits in SMADR
	BSZ[1:0] = 01 (two flash memories connected)	32 bits: DREAR.EAV[7:1 to 0] bits + lower [25 to 24:1] bits of the read address. 24 bits: Lower [24:1] bits of the read address	
Option data (8 bits × 4)		DROPR	SMOPR
Transfer data		Normal read: 8, 16, and 32 bits Burst read: 64 × RBURST bits	Read: SMRDR0, SMRDR1 Write: SMWDR0, SMWDR1

Bit	Bit Name	Initial Value	R/W	Description
0	RDF	0	R/(W)*	Receive Data Full Indicates that, when the FIFO is operating for reception, the received data is transferred to the receive FIFO data register (SSIFRDR) and the number of data bytes in the FIFO data register has become greater than the receive trigger number specified by RTRG[1:0] in the FIFO control register (SSIFCR). 0: Number of received data bytes in SSIFRDR is less than the set receive trigger number. [Clearing conditions] • Power-on reset • 0 is written to RDF after the receive FIFO is empty with writing 1 to RFRST. • 0 is written to RDF after data is read from SSIFRDR until the number of data bytes in SSIFRDR becomes less than the set receive trigger number. • The direct memory access controller is activated by receive data full (RXI) interrupt, and data is read from SSIFRDR until the number of data bytes in SSIFRDR becomes less than the set receive trigger number. 1: Number of received data bytes in SSIFRDR is equal to or greater than the set receive trigger number. [Setting condition] • Data of the number of bytes that is equal to or greater than the set receive trigger number is stored in SSIFRDR.* Note: * Since SSIFRDR is an 8-stage FIFO register, the amount of data that can be read from it while RDF = 1 is the set receive trigger number of bytes at maximum. Continuing to read data from SSIFRDR after reading all the data will result in undefined data to be read. The number of data bytes in SSIFRDR is indicated in the RDC bits in SSIFSR.

Note: * The bit can be read or written to. Writing 0 initializes the bit, but writing 1 is ignored.

When this module acts as a transmitter, each word written to SSITDR is transmitted to the serial audio bus in the order they are written. When this module acts as a receiver, each word received by the serial audio bus is read in the order received from the SSIRDR register.

Figures 20.6 to 20.8 show how the data on 4, 6, and 8 channels are transferred to the serial audio bus. Note that there are no padding bits in the first example, the second example is left-aligned and the third is right-aligned. The other conditions in these examples have been selected arbitrarily.

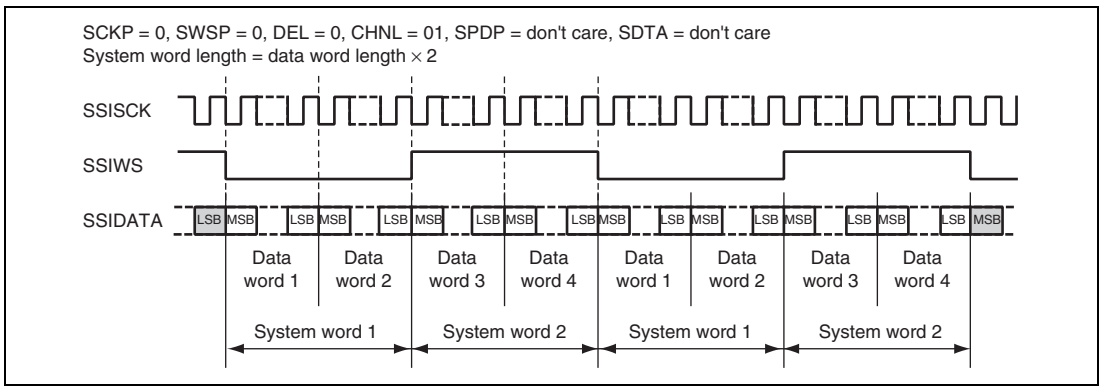

Figure 20.6 Multi-Channel Format (4 Channels Without Padding)

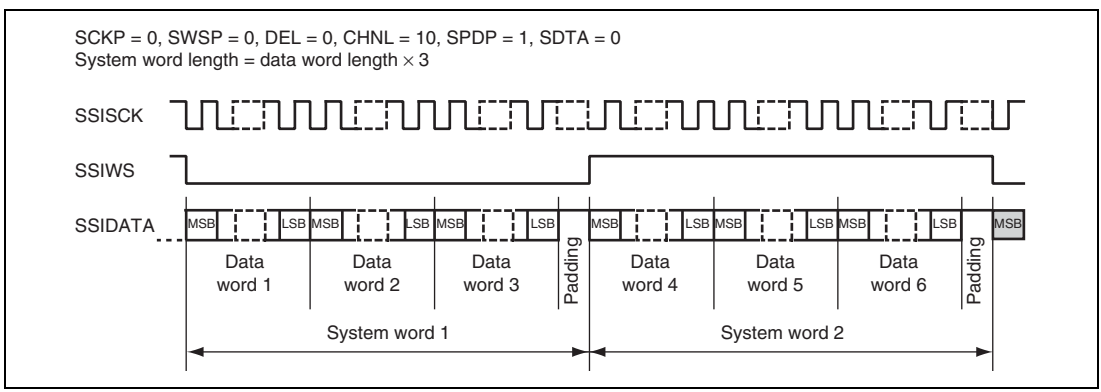

Figure 20.7 Multi-Channel Format (6 Channels with High Padding)

[Legend]

x: Don't care

Note: 1. Only 0 can be written to clear the flag after 1 is read.

2. Set the A/D conversion time to minimum or more values to meet the absolute accuracy of the A/D conversion characteristics.

3. Settings prohibited in the SH726A Group.

27.3.10 Interrupt Enable Registers 1 and 2 (INTENB1 and INTENB2)

INTENB1 is a register that enables or disables the various interrupts when the host controller function is selected on the port 0 side. INTENB2 is a register that enables or disables the various interrupts when the host controller function is selected on the port 1 side. INTENB1 also sets the interrupt mask for setup transaction.

On detecting the interrupt corresponding to the bit in these registers that has been set to 1, these modules generate the USB interrupt.

These modules set 1 to each status bit in INTSTS1 and INTSTS2 when a detection condition of the corresponding interrupt source has been satisfied regardless of the set value in INTENB1 and INTENB2 (regardless of whether the interrupt output is enabled or disabled).

While the status bit in INTSTS1 and INTSTS2 corresponding to the interrupt source indicates 1, these modules generate the USB interrupt when the corresponding interrupt enable bit in INTENB1 and INTENB2 is modified from 0 to 1.

When the function controller function is selected, the interrupts should not be enabled. These registers are initialized by a power-on reset.

(1) INTENB1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	BCHGE	—	DTCHE	ATTCHE	—	—	—	—	EOFERRE	SIGNE	SACKE	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	BCHGE	0	R/W	USB Bus Change Interrupt Enable Enables or disables the USB interrupt request when the BCHG interrupt is detected. 0: Interrupt request disabled 1: Interrupt request enabled
13	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6	EOFERRE	0	R/W	EOF Error Detection Interrupt Enable Enables or disables the USB interrupt request when the EOFERR interrupt is detected. 0: Interrupt request disabled 1: Interrupt request enabled
5 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: The INTENB2 register bits can be set to 1 only when the host controller function is selected; do not set these bits to 1 to enable the corresponding interrupt output when the function controller function is selected.

Bit	Bit Name	Initial Value	R/W	Description
9, 8	PG2MD[1:0]	00	R/W	PG2 Mode Select the function of the PG2. 00: PG2* 01: DM1 10: PINT2* 11: Setting prohibited Note: In the SH726A, bits 9 and 8 are reserved. These bits are always read as 0. The write value should always be 0.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	PG1MD[1:0]	00	R/W	PG1 Mode Select the function of the PG1. 00: PG1* 01: DP0 10: PINT1* 11: Setting prohibited
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	PG0MD[1:0]	00	R/W	PG0 Mode Select the function of the PG0. 00: PG0* 01: DM0 10: PINT0* 11: Setting prohibited

Note: * When selecting pin functions and the USB module is to be used, ensure that the USB module does not require any pins for which non-USB functions are selected.
For details, refer to section 27.5.1, USB Pin Control.

Bit	Bit Name	Initial Value	R/W	Description
1	RAME1	1	R/W	RAM Enable 1 (corresponding area: page 1* in high-speed on-chip RAM) 0: Access to page 1 is disabled. 1: Access to page 1 is enabled.
0	RAME0	1	R/W	RAM Enable 0 (corresponding area: page 0* in high-speed on-chip RAM) 0: Access to page 0 is disabled. 1: Access to page 0 is enabled.

Note: * For addresses in each page, see section 30, On-Chip RAM.

Index

Numerics

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