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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I²C, IEBus, SCI, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	73
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.3M x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s726a3d216fp-v0

SH726A Pin No.	SH726B Pin No.	Function 1		Function 2		Function 3		Function 4	
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
13	16	PB7	I(s)/O	A7	O	RxD0	I(s)	—	—
14	17	PB8	I(s)/O	A8	O	TxD0	O	—	—
15	18	PB9	I(s)/O	A9	O	SCK1	I(s)/O	SSIWS2	I(s)/O
NC	19	PJ8	I(s)/O	TIOC3A	I(s)/O	A23	O	SCK2	I(s)/O
NC	20	PJ9	I(s)/O	TIOC3B	I(s)/O	A24	O	RxD2	I(s)
NC	21	PJ10	I(s)/O	TIOC3C	I(s)/O	A25	O	TxD2	O
16	22	PVcc							
17	23	PB10	I(s)/O	A10	O	RxD1	I(s)	—	—
18	24	Vss							
19	25	PB11	I(s)/O	A11	O	TxD1	O	—	—
20	26	Vcc							
21	27	PB12	I(s)/O	A12	O	SCK2	I(s)/O	SSIDATA2	I(s)/O
22	28	PB13	I(s)(5t)/O	A13	O	RxD2	I(s)(5t)	—	—
23	29	PB14	I(s)/O	A14	O	TxD2	O	—	—
24	30	PB15	I(s)/O	A15	O	RSPCK0	I(s)/O	TIOC0B	I(s)/O

SH726A Pin No.	SH726B Pin No.	Function 5		Function 6		Function 7		ASE Function		Circuit diagram Figure 1.3
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
13	16	—	—	—	—	—	—	—	—	(7)
14	17	—	—	—	—	—	—	—	—	(7)
15	18	—	—	—	—	—	—	—	—	(7)
NC	19	SSISCK2	I(s)/O	TEND0	O	—	—	—	—	(7)
NC	20	SSIWS2	I(s)/O	DREQ0	I(s)	—	—	—	—	(7)
NC	21	SSIDATA2	I(s)/O	DACK0	O	—	—	—	—	(7)
16	22									
17	23	—	—	—	—	—	—	—	—	(7)
18	24									
19	25	—	—	—	—	—	—	—	—	(7)
20	26									
21	27	—	—	—	—	—	—	—	—	(7)
22	28	—	—	—	—	—	—	—	—	(7)
23	29	—	—	—	—	—	—	—	—	(7)
24	30	—	—	—	—	—	—	—	—	(7)

SH726A Pin No.	SH726B Pin No.	Function 1		Function 2		Function 3		Function 4	
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
112	136	PVcc							
113	137	PD7	I(s)/O	D7	I/O	MISO1	I(s)/O	TxD4	O
114	138	Vss							
115	139	PD8	I(s)/O	D8	I/O	SD_CD	I(s)	TIOC0A	I(s)/O
116	140	PD9	I(s)/O	D9	I/O	SD_WP	I(s)	TIOC1A	I(s)/O
117	141	PD10	I(s)/O	D10	I/O	SD_D1	I(s)/O	TIOC2A	I(s)/O
118	142	PD11	I(s)/O	D11	I/O	SD_D0	I(s)/O	TIOC3A	I(s)/O
119	143	PD12	I(s)/O	D12	I/O	SD_CLK	O	IRQ2	I(s)
120	144	PD13	I(s)/O	D13	I/O	SD_CMD	I(s)/O	IRQ3	I(s)

SH726A Pin No.	SH726B Pin No.	Function 5		Function 6		Function 7		ASE Function		Circuit diagram Figure 1.3
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
112	136									
113	137	$\overline{\text{RTS2}}$	I(s)/O	—	—	—	—	—	—	(8)
114	138									
115	139	—	—	—	—	—	—	—	—	(8)
116	140	—	—	—	—	—	—	—	—	(8)
117	141	—	—	—	—	—	—	—	—	(8)
118	142	—	—	—	—	—	—	—	—	(8)
119	143	—	—	—	—	—	—	—	—	(8)
120	144	—	—	—	—	—	—	—	—	(8)

[Legend]

(s): Schmitt

(a): Analog

(o): Open drain

(5t): 5-V tolerant

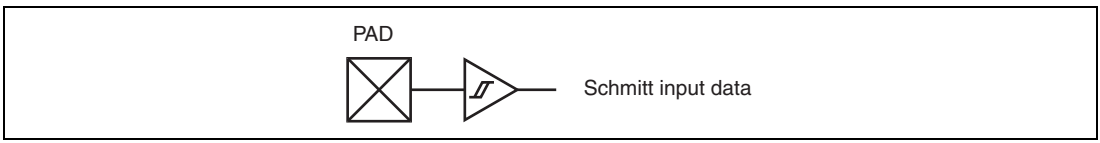
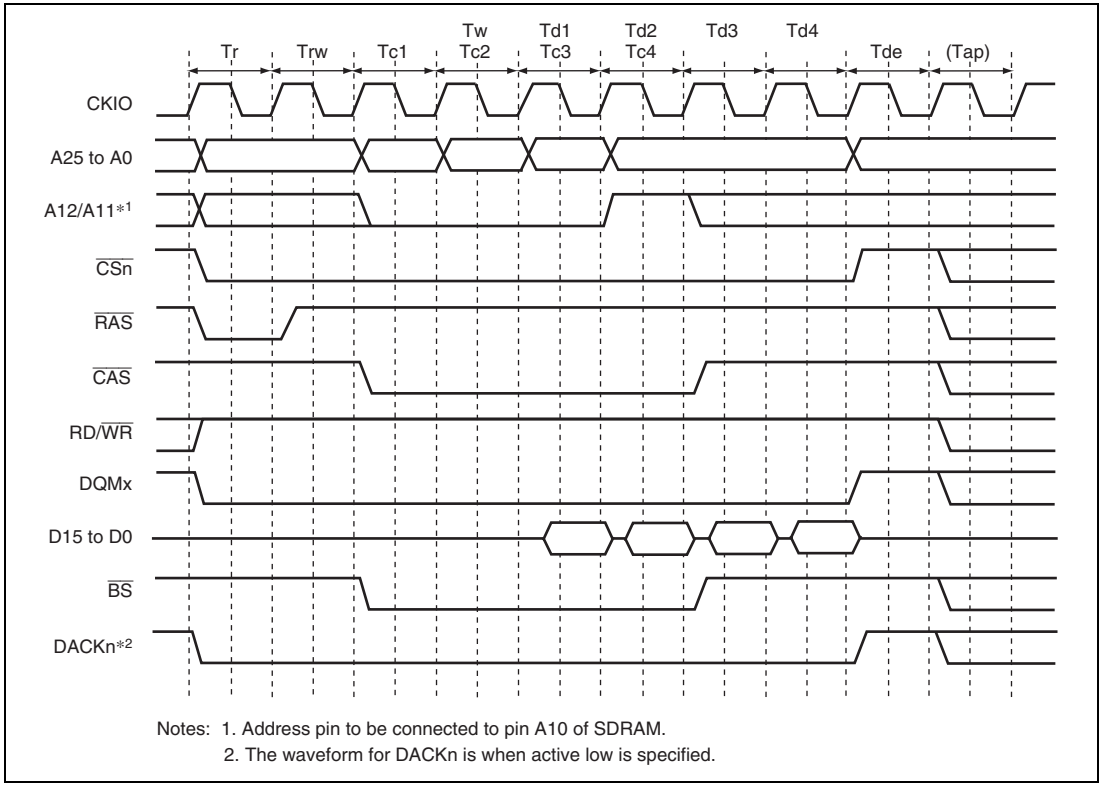


Figure 1.3 (1) Simplified Circuit Diagram (Schmitt Input Buffer)

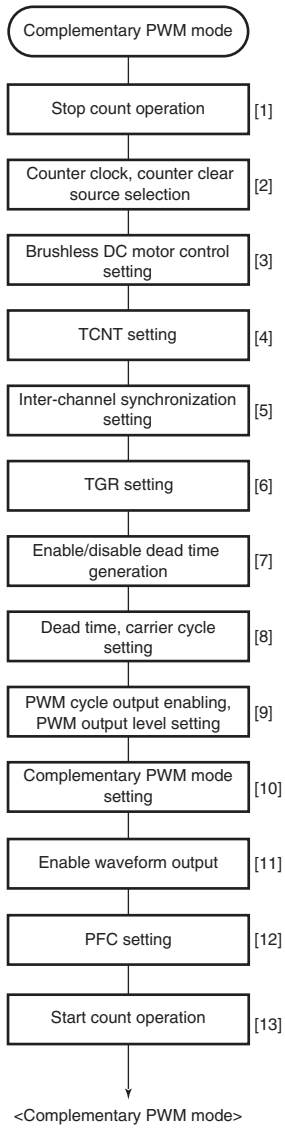


Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 10.12 Burst Read Wait Specification Timing (CAS Latency 2, WTRCD[1:0] = 1 Cycle, Auto Pre-Charge)

(1) Example of Complementary PWM Mode Setting Procedure

An example of the complementary PWM mode setting procedure is shown in figure 12.38.



[1] Clear bits CST3 and CST4 in the timer start register (TSTR) to 0, and halt timer counter (TCNT) operation. Perform complementary PWM mode setting when TCNT_3 and TCNT_4 are stopped.

[2] Set the same counter clock and clock edge for channels 3 and 4 with bits TPSC2-TPSC0 and bits CKEG1 and CKEG0 in the timer control register (TCR). Use bits CCLR2-CCLR0 to set synchronous clearing only when restarting by a synchronous clear from another channel during complementary PWM mode operation.

[3] When performing brushless DC motor control, set bit BDC in the timer gate control register (TGCR) and set the feedback signal input source and output chopping or gate signal direct output.

[4] Set the dead time in TCNT_3. Set TCNT_4 to H'0000.

[5] Set only when restarting by a synchronous clear from another channel during complementary PWM mode operation. In this case, synchronize the channel generating the synchronous clear with channels 3 and 4 using the timer synchro register (TSYR).

[6] Set the output PWM duty in the duty registers (TGRB_3, TGRA_4, TGRB_4) and buffer registers (TGRD_3, TGRC_4, TGRD_4). Set the same initial value in each corresponding TGR.

[7] This setting is necessary only when no dead time should be generated. Make appropriate settings in the timer dead time enable register (TDER) so that no dead time is generated.

[8] Set the dead time in the dead time register (TDDR), 1/2 the carrier cycle in the timer cycle data register (TCDR) and timer cycle buffer register (TCBR), and 1/2 the carrier cycle plus the dead time in TGRA_3 and TGRC_3. When no dead time generation is selected, set 1 in TDDR and 1/2 the carrier cycle + 1 in TGRA_3 and TGRC_3.

[9] Select enabling/disabling of toggle output synchronized with the PWM cycle using bit PSYE in the timer output control register 1 (TOCR1), and set the PWM output level with bits OLSP and OLSN. When specifying the PWM output level by using TOLBR as a buffer for TOCR_2, see figure 12.3.

[10] Select complementary PWM mode in timer mode register 3 (TMDR_3). Do not set in TMDR_4.

[11] Set enabling/disabling of PWM waveform output pin output in the timer output master enable register (TOER).

[12] Set the port control register and the port I/O register.

[13] Set bits CST3 and CST4 in TSTR to 1 simultaneously to start the count operation.

Figure 12.38 Example of Complementary PWM Mode Setting Procedure

Section 15 Realtime Clock

This LSI has a realtime clock and a 4-MHz crystal oscillator.

15.1 Features

- Clock and calendar functions (BCD format): Seconds, minutes, hours, date, day of the week, month, and year.
- 1-Hz to 64-Hz timer (binary format)
  64-Hz counter indicates the state of the divider circuit between 64 Hz and 1 Hz
- Start/stop function
- 30-second adjust function
- Alarm interrupt: Frame comparison of seconds, minutes, hours, date, day of the week, month, and year can be used as conditions for the alarm interrupt
- Periodic interrupts: the interrupt cycle may be 1/64 second, 1/16 second, 1/4 second, 1/2 second, 1 second, or 2 seconds
- Carry interrupt: a carry interrupt indicates when a carry occurs during a counter read
- Automatic leap year adjustment
- Any of the external clock signal dedicated for the clock function or the internal signal can be selected as the operating clock signal for the clock function.
- Recovery from deep standby mode can be performed by an alarm interrupt.

Bit	Bit Name	Initial Value	R/W	Description
5	TDFE	1	R/(W)*	Transmit FIFO Data Empty Indicates that data has been transferred from the transmit FIFO data register (SCFTDR) to the transmit shift register (SCTSR), the quantity of data in SCFTDR has become less than the transmission trigger number specified by the TTRG[1:0] bits in the FIFO control register (SCFCR), and writing of transmit data to SCFTDR is enabled. 0: The quantity of transmit data written to SCFTDR is greater than the specified transmission trigger number [Clearing conditions] • TDFE is cleared to 0 when data exceeding the specified transmission trigger number is written to SCFTDR after 1 is read from TDFE and then 0 is written • TDFE is cleared to 0 when direct memory access controller is activated by transmit FIFO data empty interrupt (TXI) and write data exceeding the specified transmission trigger number to SCFTDR 1: The quantity of transmit data in SCFTDR is less than or equal to the specified transmission trigger number*[1] [Setting conditions] • TDFE is set to 1 by a power-on reset • TDFE is set to 1 when the quantity of transmit data in SCFTDR becomes less than or equal to the specified transmission trigger number as a result of transmission Note: 1. Since SCFTDR is a 16-byte FIFO register, the maximum quantity of data that can be written when TDFE is 1 is "16 minus the specified transmission trigger number". If an attempt is made to write additional data, the data is ignored. The quantity of data in SCFTDR is indicated by the upper 8 bits of SCFDR.

- SSL control function
  One SSL signal for each channel
  In master mode, outputs SSL signal.
  In slave mode, inputs SSL signal.
  Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay)
  Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units)
  Controllable delay from RSPCK stoppage to SSL output negation (SSL negation delay)
  Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units)
  Controllable wait for next-access SSL output assertion (next-access delay)
  Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units)
  Function for changing SSL polarity
- Control in master transfer
  A transfer of up to four commands can be executed sequentially in looped execution.
  For each command, the following can be set:
  SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB first, burst, RSPCK delay, SSL negation delay, and next-access delay.
  A transfer can be initiated by writing to the transmit buffer.
  A transfer can be initiated by clearing the SPTEF bit.
  MOSI signal value specifiable in SSL negation
- Interrupt sources
  Maskable interrupt sources:
  Receive interrupt (receive buffer full)
  Transmit interrupt (transmit buffer empty)
  Error interrupt (mode fault, overrun)
- Others
  Provides loop back mode
  Provides a function for disabling (initializing) this module

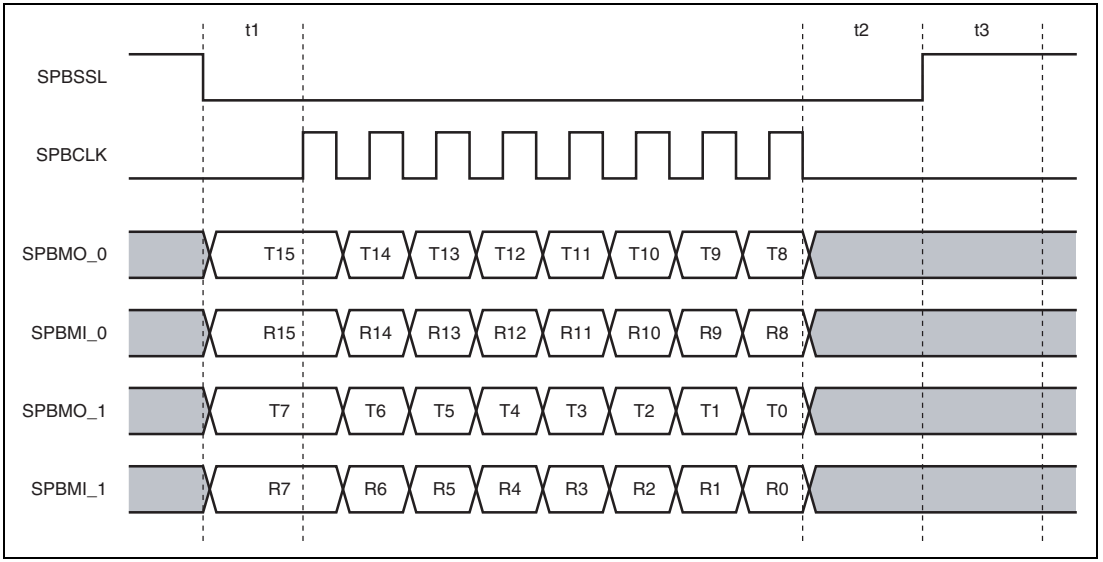


Figure 18.19 Transfer Format Example with 1-Bit Data Size and Two Serial Flash Memories Connected

19.5 Interrupt Requests

There are six interrupt requests in this module; transmit data empty, transmit end, receive data full, NACK detection, STOP recognition, and arbitration lost/overrun error. Table 19.4 shows the contents of each interrupt request.

Table 19.4 Interrupt Requests

Interrupt Request	Abbreviation	Interrupt Condition	I²C Bus Format	Clocked Synchronous Serial Format
Transmit data Empty	TXI	(TDRE = 1) • (TIE = 1)	√	√
Transmit end	TEI	(TEND = 1) • (TEIE = 1)	√	√
Receive data full	RXI	(RDRF = 1) • (RIE = 1)	√	√
STOP recognition	STPI	(STOP = 1) • (STIE = 1)	√	—
NACK detection	NAKI	{(NACKF = 1) + (AL = 1)} • (NAKIE = 1)	√	—
Arbitration lost/ overrun error			√	√

When the interrupt condition described in table 19.4 is 1, the CPU executes an interrupt exception handling. Note that a TXI or RXI interrupt can activate the direct memory access controller if the setting for direct memory access controller activation has been made. In such a case, an interrupt request is not sent to the CPU. Interrupt sources should be cleared in the exception handling. The TDRE and TEND bits are automatically cleared to 0 by writing the transmit data to ICDRT. The RDRF bit is automatically cleared to 0 by reading ICDRR. The TDRE bit is set to 1 again at the same time when the transmit data is written to ICDRT. Therefore, when the TDRE bit is cleared to 0, then an excessive data of one byte may be transmitted.

(1) Reception Using Direct Memory Access Controller

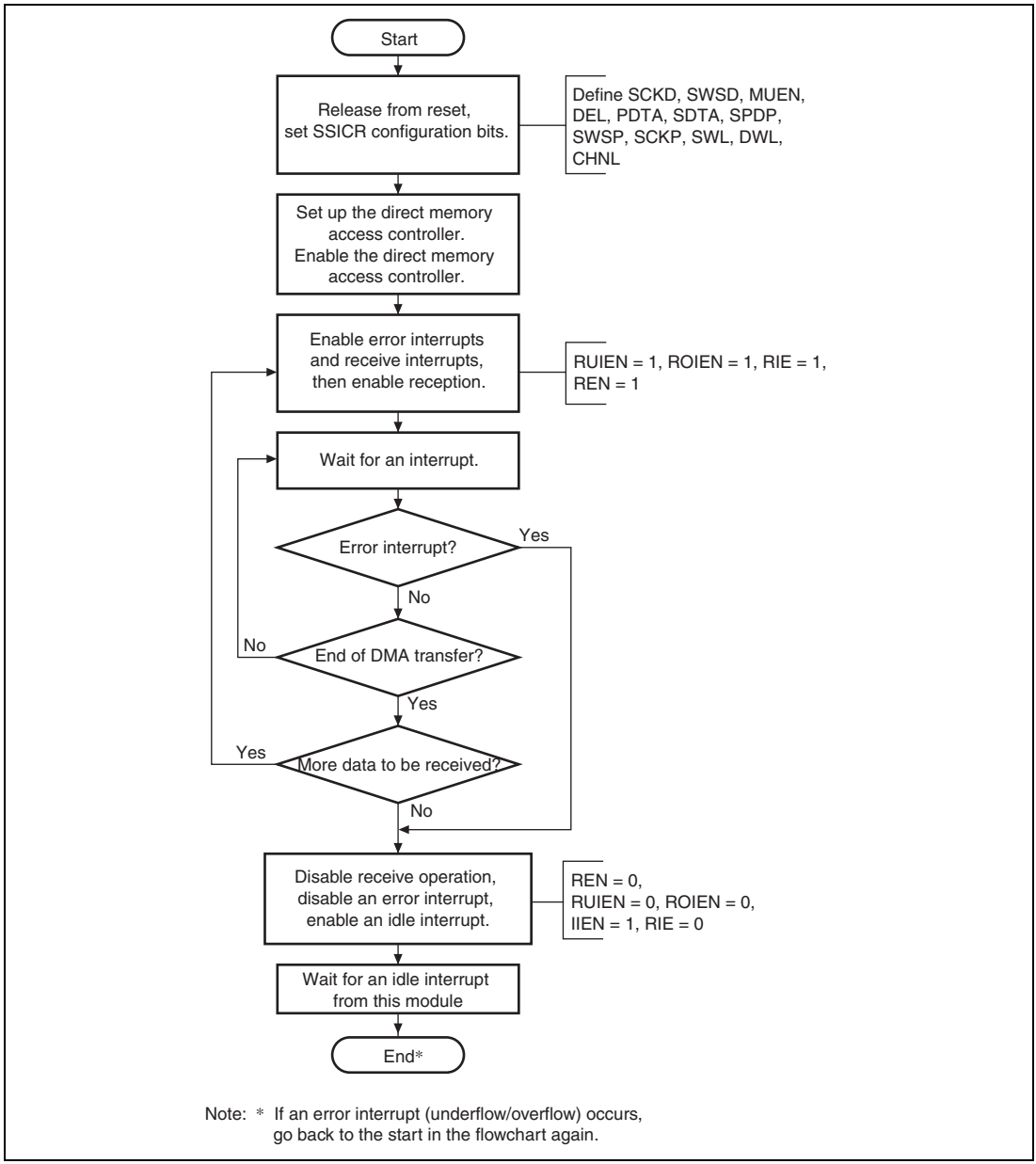


Figure 20.25 Reception Using Direct Memory Access Controller

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	MD_SEC [2:0]	010	R/W	Sector Type 000: Setting prohibited 001: Mode 0 010: Mode 1 011: Long (Mode 0, Mode 1, or Mode 2 with no EDC/ECC data) 100: Setting prohibited 101: Mode 2 Form 1 110: Mode 2 Form 2 111: Mode 2 with automatic form detection If the form cannot be determined when set to B'111, it is processed as Mode 2 not XA.

25.3.4 EDC/ECC Check Control Register (CROMCTL1)

The EDC/ECC check control register (CROMCTL1) controls EDC/ECC checking. The setting of this register becomes valid at the sector-to-sector transition

Bit:	7	6	5	4	3	2	1	0
	M2F2 EDC	MD_DEC[2:0]			-	-	MD_PQREP[1:0]	
Initial value:	1	1	0	1	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	M2F2EDC	1	R/W	For Mode 2 Form 2, disables the EDC function for sectors where all bits of the EDC are 0. When this bit set to 1 and all bits of the EDC for a Mode 2 Form 2 sector are 0, an IERR interrupt is not generated even if the result of EDC checking is ‘fail’.

Bit	Bit Name	Initial Value	R/W	Description
4	ST_ ECCNG	0	R	Indicates that error correction was not possible. This bit is also set to 1 on detection of a short sector.
3	ST_ECCP	0	R	Indicates that P-parity errors were not corrected in ECC correction. This bit is only valid when synchronization is normal (the sector is neither short nor long). This bit is set to 1 when the result of syndrome calculation for P parity is non-0.
2	ST_ECCQ	0	R	Indicates that Q-parity errors were not corrected in ECC correction. This bit is only valid when synchronization is normal (the sector is neither short nor long). This bit is set to 1 when the result of syndrome calculation for Q parity is other than all 0s.
1	ST_EDC1	0	R	Indicates that the result of the EDC check before ECC correction was ‘fail’. This bit is also set to 1 if a short sector is encountered while EDC is enabled.
0	ST_EDC2	0	R	Indicates that the result of the EDC check after ECC correction was ‘fail’.

Figure 26.1 shows a block diagram of the A/D converter.

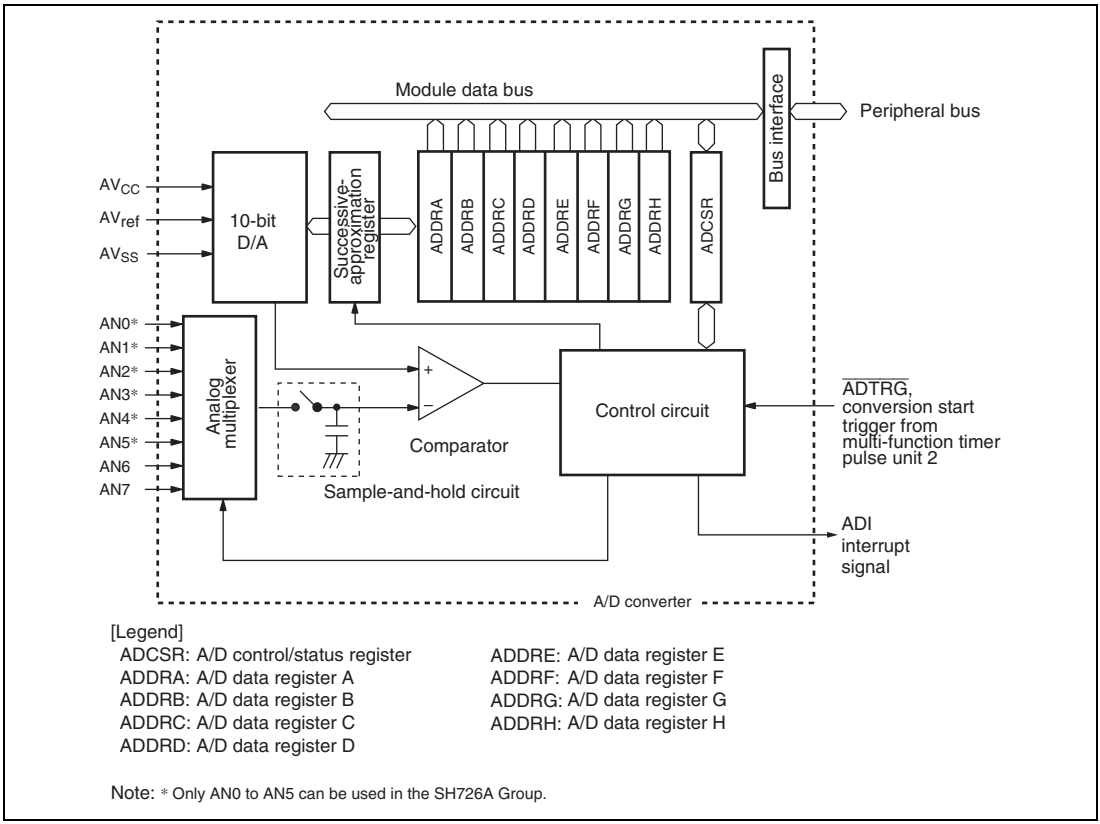


Figure 26.1 Block Diagram of A/D Converter

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TRNCNT[15:0]	All 0	R/W	This module increments the value of these bits by one when all of the following conditions are satisfied on receiving the packet. • TRENB is 1. • (TRNCNT set value ≠ current counter value + 1) on receiving the packet. • The payload of the received packet agrees with the set value in the MXPS bits. This module clears the value of these bits to 0 when any of the following conditions are satisfied. • All the following conditions are satisfied. TRENB is 1. (TRNCNT set value = current counter value + 1) on receiving the packet. The payload of the received packet agrees with the set value in the MXPS bits. • All the following conditions are satisfied. TRENB is 1. This module has received a short packet. • The following condition is satisfied. The TRCLR bit has been set to 1. For the pipe in the transmitting direction, set these bits to 0. When the transaction counter is not used, set these bits to 0. Modify these bits while TRENB is 0. To modify the value of these bits, set TRNCNT to 1 before setting TRENB to 1.

The interval counting starts at the different timing depending on the IITV bit setting (similar to the timing during OUT transfers).

The interval counting is cleared on any of the following conditions in function controller mode.

- When a power-on reset is applied.
- When the ACLRM bit is set to 1.
- When this module detects a USB bus reset.

(4) Setup of Data to be Transmitted using Isochronous Transfer when the Function Controller Function is Selected

With isochronous data transmission using this module in function controller function, after data has been written to the buffer memory, a data packet can be sent with the next frame in which an SOF packet is detected. This function is called the isochronous transfer transmission data setup function, and it makes it possible to designate the frame from which transmission began.

If a double buffer is used for the buffer memory, transmission will be enabled for only one of the two buffers even after the writing of data to both buffers has been completed, that buffer memory being the one to which the data writing was completed first. For this reason, even if multiple IN tokens are received, the only buffer memory that can be sent is one packet's worth of data.

When an IN token is received, if the buffer memory is in the transmission enabled state, this module transmits the data. If the buffer memory is not in the transmission enabled state, however, a zero-length packet is sent and an underrun error occurs.

Figure 27.12 shows an example of transmission using the isochronous transfer transmission data setup function with this module, when IITV = 0 (every frame) has been set.

Bit	Bit Name	Initial Value	R/W	Description
6	RTCAR	0	R/W	Cancel by Realtime Clock Alarm Interrupt 0: Deep standby mode is not canceled by a realtime clock alarm interrupt. 1: Deep standby mode is canceled by a realtime clock alarm interrupt.
5	PC8	0	R/W	Cancel by Change on PC8 0: Deep standby mode is not canceled by change on the PC8 pin. 1: Deep standby mode is canceled by change on the PC8 pin.
4	PC7	0	R/W	Cancel by Change on PC7 0: Deep standby mode is not canceled by change on the PC7 pin. 1: Deep standby mode is canceled by change on the PC7 pin.
3	PC6	0	R/W	Cancel by Change on PC6 0: Deep standby mode is not canceled by change on the PC6 pin. 1: Deep standby mode is canceled by change on the PC6 pin.
2	PC5	0	R/W	Cancel by Change on PC5 0: Deep standby mode is not canceled by change on the PC5 pin. 1: Deep standby mode is canceled by change on the PC5 pin.
1	PJ13	0	R/W	Cancel by Change on PJ13 0: Deep standby mode is not canceled by change on the PJ13 pin. 1: Deep standby mode is canceled by change on the PJ13 pin. Note: This bit can be used only in the SH726B.

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
Renesas serial peripheral interface	Pin control register_1	SPPCR_1	8	H'FFFF8802	8, 16
	Status register_1	SPSR_1	8	H'FFFF8803	8, 16
	Data register_1	SPDR_1	32	H'FFFF8804	8, 16, 32
	Sequence control register_1	SPSCR_1	8	H'FFFF8808	8, 16
	Sequence status register_1	SPSSR_1	8	H'FFFF8809	8, 16
	Bit rate register_1	SPBR_1	8	H'FFFF880A	8, 16
	Data control register_1	SPDCR_1	8	H'FFFF880B	8, 16
	Clock delay register_1	SPCKD_1	8	H'FFFF880C	8, 16
	Slave select negation delay register_1	SSLND_1	8	H'FFFF880D	8, 16
	Next-access delay register_1	SPND_1	8	H'FFFF880E	8
	Command register_10	SPCMD_10	16	H'FFFF8810	16
	Command register_11	SPCMD_11	16	H'FFFF8812	16
	Command register_12	SPCMD_12	16	H'FFFF8814	16
	Command register_13	SPCMD_13	16	H'FFFF8816	16
	Buffer control register_1	SPBFCR_1	8	H'FFFF8820	8, 16
	Buffer data count setting register_1	SPBFDR_1	16	H'FFFF8822	16
	Control register_2	SPCR_2	8	H'FFFFB000	8, 16
	Slave select polarity register_2	SSLP_2	8	H'FFFFB001	8, 16
	Pin control register_2	SPPCR_2	8	H'FFFFB002	8, 16
	Status register_2	SPSR_2	8	H'FFFFB003	8, 16
	Data register_2	SPDR_2	32	H'FFFFB004	8, 16, 32
	Sequence control register_2	SPSCR_2	8	H'FFFFB008	8, 16
	Sequence status register_2	SPSSR_2	8	H'FFFFB009	8, 16
	Bit rate register_2	SPBR_2	8	H'FFFFB00A	8, 16
	Data control register_2	SPDCR_2	8	H'FFFFB00B	8, 16
	Clock delay register_2	SPCKD_2	8	H'FFFFB00C	8, 16
	Slave select negation delay register_2	SSLND_2	8	H'FFFFB00D	8, 16
	Next-access delay register_2	SPND_2	8	H'FFFFB00E	8
	Command register_20	SPCMD_20	16	H'FFFFB010	16
	Command register_21	SPCMD_21	16	H'FFFFB012	16
	Command register_22	SPCMD_22	16	H'FFFFB014	16

Item		Power Supply	Symbol	Typ.	Max.	Unit	Test Conditions
Current consumption in deep standby mode	Ta > 50 °C	PVcc + AVcc + AVref	PIdstby	3.5	16	μA	RTC is not operating
				7.5	20	μA	RTC_X1 external selected*2
				0.8	—	mA	RTC_X1 4 MHz selected Small gain*1
				1	—	mA	EXTAL 12 MHz selected Small gain*1
				3.5	—	mA	EXTAL 48 MHz selected Large gain*1
	Ta ≤ 50 °C	Vcc + PLLVcc	Idstby	2	17	μA	RAM 0 Kbytes retained, RTC_X1 external selected*2
				3.5	27	μA	RAM 16 Kbytes retained, RTC_X1 external selected*2
				5	37	μA	RAM 32 Kbytes retained, RTC_X1 external selected*2
				8	56	μA	RAM 64 Kbytes retained, RTC_X1 external selected*2
				14	95	μA	RAM 128 Kbytes retained, RTC_X1 external selected*2
				When EXTAL 12 MHz is selected, 5 μA and 6 μA are added to the "Typ." and "Max." values above, respectively. When EXTAL 48 MHz is selected, 20 μA and 25 μA are added to the "Typ." and "Max." values above, respectively. When RTC_X1 4 MHz is selected, 2 μA and 2.5 μA are added to the "Typ." and "Max." values above, respectively.		
		PVcc + AVcc + AVref	PIdstby	3	12	μA	RTC is not operating
				7	16	μA	RTC_X1 external selected*2
				0.8	—	mA	RTC_X1 4 MHz selected Small gain*1
				1	—	mA	EXTAL 12 MHz selected Small gain*1
				3.5	—	mA	EXTAL 48 MHz selected Large gain*1

35.4 AC Characteristics

Signals input to this LSI are basically handled as signals in synchronization with a clock. The setup and hold times for input pins must be followed.

- Conditions for AC characteristics
  V_{cc} = PLLV_{cc} = 1.15 to 1.35 V, PV_{cc} = 3.0 to 3.6 V, AV$_{cc}$ = 3.0 to 3.6 V, V_{ss} = AV$_{ss}$ = 0 V, T_a = –40 to 85 °C

Table 35.4 Operating Frequency

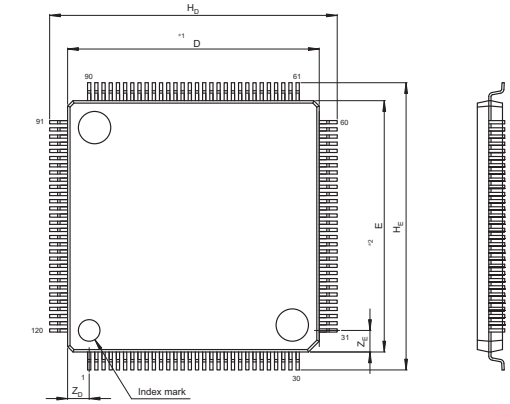
Item		Symbol	Min.	Max.	Unit	Remarks
Operating frequency	CPU clock (Iϕ)	f	60.00	216.00	MHz	
	Bus clock (Bϕ)		60.00	72.00	MHz	
	Peripheral clock (Pϕ)		15.00	36.00	MHz	

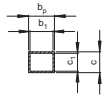
35.4.1 Clock Timing

Table 35.5 Clock Timing

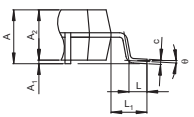
Item	Symbol	Min.	Max.	Unit	Figure
EXTAL clock input frequency (clock mode is 0)	f_{EX}	10.00	12.00	MHz	Figure 35.1
EXTAL clock input cycle time (clock mode is 0)	t_{EXcyc}	83.33	100.00	ns	
EXTAL clock input frequency (clock mode is 1) (when EXTAL is supplied to USB 2.0 host/function module)	f_{EX}	48 MHz ± 500 ppm			
EXTAL clock input frequency (clock mode is 1) (when EXTAL isn't supplied to USB 2.0 host/function module)		40.00	48.00	MHz	
EXTAL clock input cycle time (clock mode is 1) (when EXTAL isn't supplied to USB 2.0 host/function module)	t_{EXcyc}	20.83	25.00	ns	
AUDIO_X1 clock input frequency (crystal resonator connected)	f_{EX}	10.00	50.00	MHz	
AUDIO_X1 clock input cycle time (crystal resonator connected)	t_{EXcyc}	20.00	100.00	ns	
AUDIO_X1, AUDIO_CLK clock input frequency (external clock input)	f_{EX}	1.00	50.00	MHz	

JEITA Package Code	RENESAS Code	MASS[Typ.]
P-LQFP120-14x14-0.40	PLQP0120LA-A	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.13	0.18	0.23
b_1	—	0.16	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.4	—
x	—	—	0.07
y	—	—	0.08
Z_D	—	1.2	—
Z_E	—	1.2	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A.2 Package Dimensions of the SH726A (2)