Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151c6u3

IWDG: Independent watchdog
LCD: Liquid crystal display
POR/PDR: Power on reset / power down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

3.1 Low-power modes

The medium-density STM8L151x4/6 and STM8L152x4/6 devices support five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: The CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt, event or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode). Wait consumption: refer to *Table 21*.
- **Low power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power run mode consumption: refer to *Table 22*.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power wait mode consumption: refer to *Table 23*.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset. Active-halt consumption: refer to *Table 24* and *Table 25*.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs. Halt consumption: refer to *Table 26*.

3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources can be used to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 kHz Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC and LCD clock sources:** the above four sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Note: ADC1 can be served by DMA1.

3.10 Digital-to-analog converter (DAC)

- 12-bit DAC with output buffer
- Synchronized update capability using TIM4
- DMA capability
- External triggers for conversion
- Input reference voltage V_{REF+} for better resolution

Note: DAC can be served by DMA1.

3.11 Ultra-low-power comparators

The medium-density STM8L151x4/6 and STM8L152x4/6 embed two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage or internal reference voltage sub multiple (1/4, 1/2, 3/4)

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC and the internal reference voltage V_{REFINT}. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (*Section 3.13: Touch sensing*).

3.13 Touch sensing

Medium-density STM8L151x4/6 and STM8L152x4/6 devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (example, glass, plastic). The capacitive variation introduced by a finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. In medium-density STM8L151x4/6

Figure 6. STM8L151G4, STM8L151G6 WLCSP28 package pinout

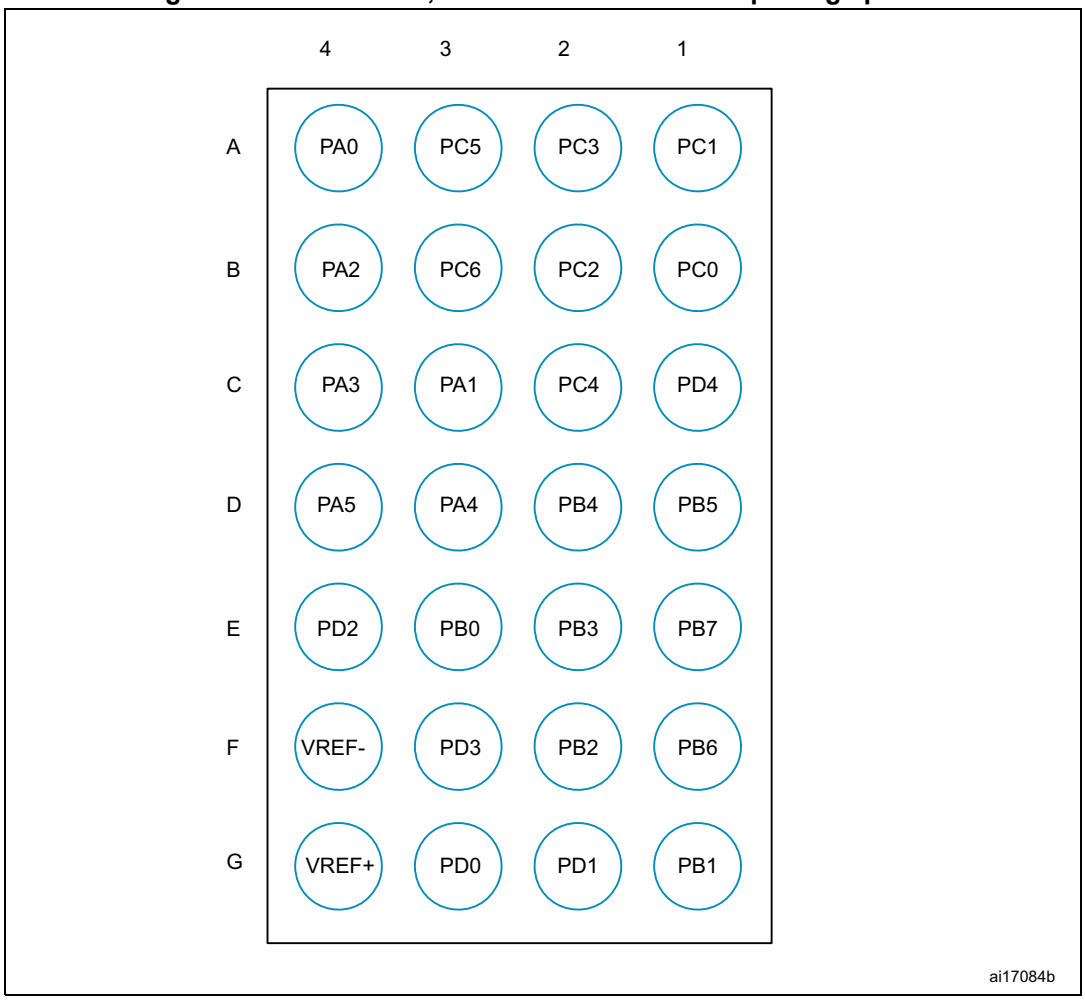


Figure 7. STM8L152C4, STM8L152C6 48-pin pinout (with LCD)

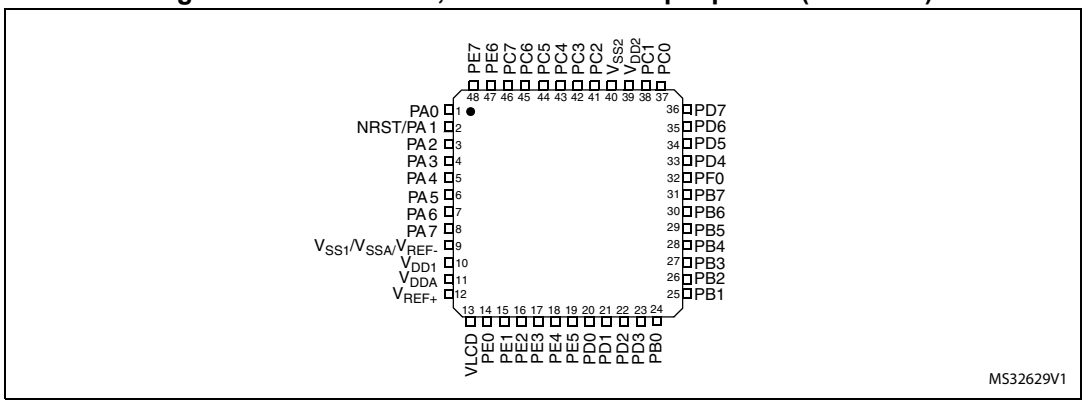


Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	9	G2	PD1/TIM1_CH3/[*TIM3_ETR*](4)/LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D1**	Timer 1 channel 3 / *[Timer 3 - external trigger]* / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input
22	11	10	E4	PD2/TIM1_CH1 /LCD_SEG8(2)/ ADC1_IN20/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D2**	Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20 / Comparator 1 positive input
23	12	-	-	PD3/ TIM1_ETR/ LCD_SEG9(2)/ADC1_IN19/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D3**	Timer 1 - external trigger / LCD segment 9 / ADC1_IN19 / Comparator 1 positive input
-	-	11	F3	PD3/ TIM1_ETR/ LCD_SEG9(2)/ ADC1_IN19/TIM1_BKIN/ COMP1_INP/ RTC_CALIB	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D3**	Timer 1 - external trigger / LCD segment 9 / ADC1_IN19 / Timer 1 break input / RTC calibration / Comparator 1 positive input
33	21	20	C1	PD4/TIM1_CH2 /LCD_SEG18(2)/ ADC1_IN10/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/ Comparator 1 positive input
34	22	-	-	PD5/TIM1_CH3 /LCD_SEG19(2)/ ADC1_IN9/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D5**	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ Comparator 1 positive input
35	23	-	-	PD6/TIM1_BKIN /LCD_SEG20(2)/ ADC1_IN8/RTC_CALIB/ /VREFINT/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D6**	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration / Internal voltage reference output / Comparator 1 positive input

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52D2	TIM1	TIM1_DCR2	TIM1 DMA1 control register 2	0x00
0x00 52D3		TIM1_DMA1R	TIM1 DMA1 address for burst mode	0x00
0x00 52D4 to 0x00 52DF	Reserved area (12 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 bytes)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5300 to 0x00 533F	Reserved area (64 bytes)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option bytes can also be modified 'on the fly' by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

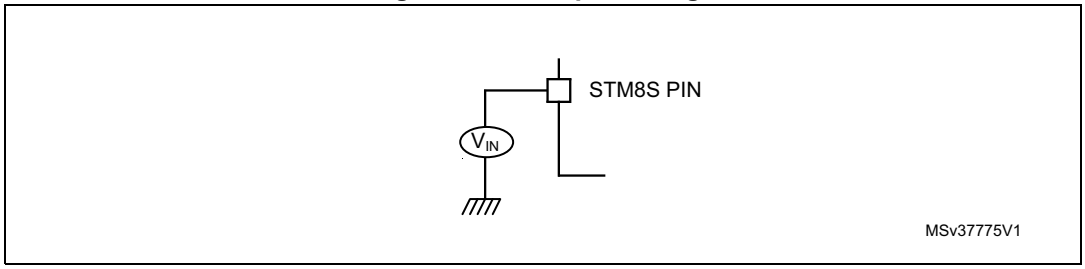
Table 12. Option byte addresses

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved										0x00
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x00
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 11. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 15: Voltage characteristics*, *Table 16: Current characteristics*, and *Table 17: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

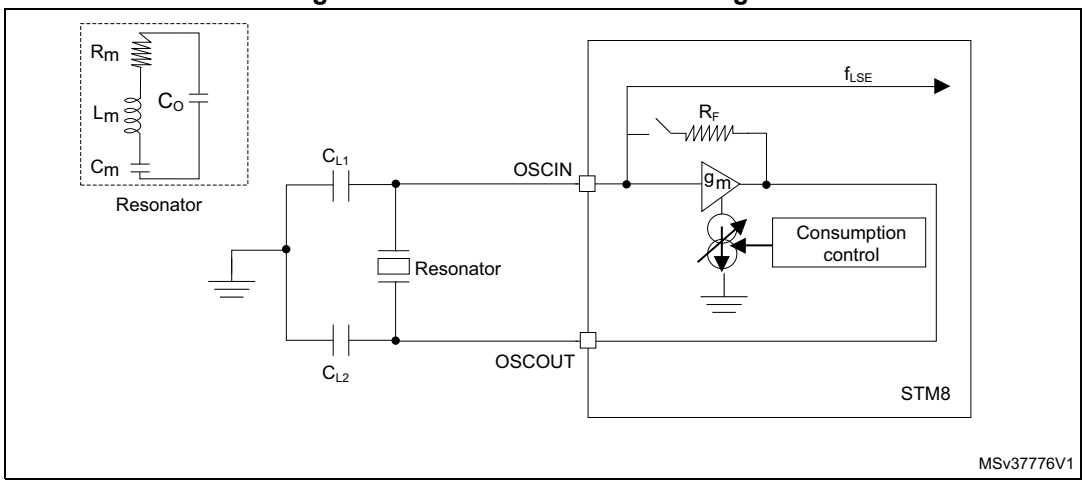
Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 15. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage (including V_{DDA} and V_{DD2})(1)	- 0.3	4.0	V
V_{IN}(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on five-volt tolerant (FT) pins (PA7 and PE0)	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on 3.6 V tolerant (TT) pins	V_{SS} - 0.3	4.0	
	Input voltage on any other pin	V_{SS} - 0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 115*		

1. All power (V_{DD1}, V_{DD2}, V_{DDA}) and ground (V_{SS1}, V_{SS2}, V_{SSA}) pins must always be connected to the external power supply.
2. V_{IN} maximum must always be respected. Refer to *Table 16.* for maximum allowed injected current values.

Figure 18. LSE oscillator circuit diagram



Internal clock sources

Subject to general operating conditions for V_{DD}, and T_A.

High speed internal RC oscillator (HSI)

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	-1 (2)	-	1(2)	%
		V_{DD} = 3.0 V, 0 °C ≤T_A ≤ 55 °C	-1.5	-	1.5	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 70 °C	-2	-	2	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 85 °C	-2.5	-	2	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 125 °C	-4.5	-	2	%
		1.65 V ≤V_{DD} ≤ 3.6 V, -40 °C ≤T_A ≤ 125 °C	-4.5	-	3	%
TRIM	HSI user trimming step(3)	Trimming code ≠ multiple of 16	-	0.4	0.7	%
		Trimming code = multiple of 16	-		± 1.5	%
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)	-	-	3.7	6(4)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	100	140(4)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Tested in production.
3. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.
4. Guaranteed by design.

Figure 23. Typical pull-up resistance R_{PU} vs V_{DD} with $V_{IN}=V_{SS}$

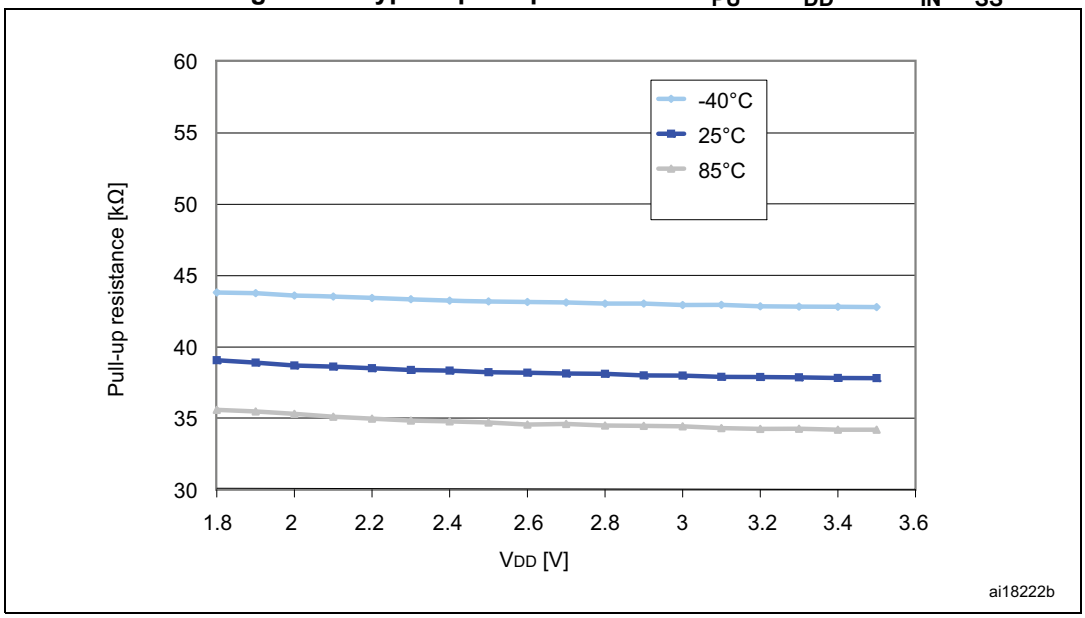
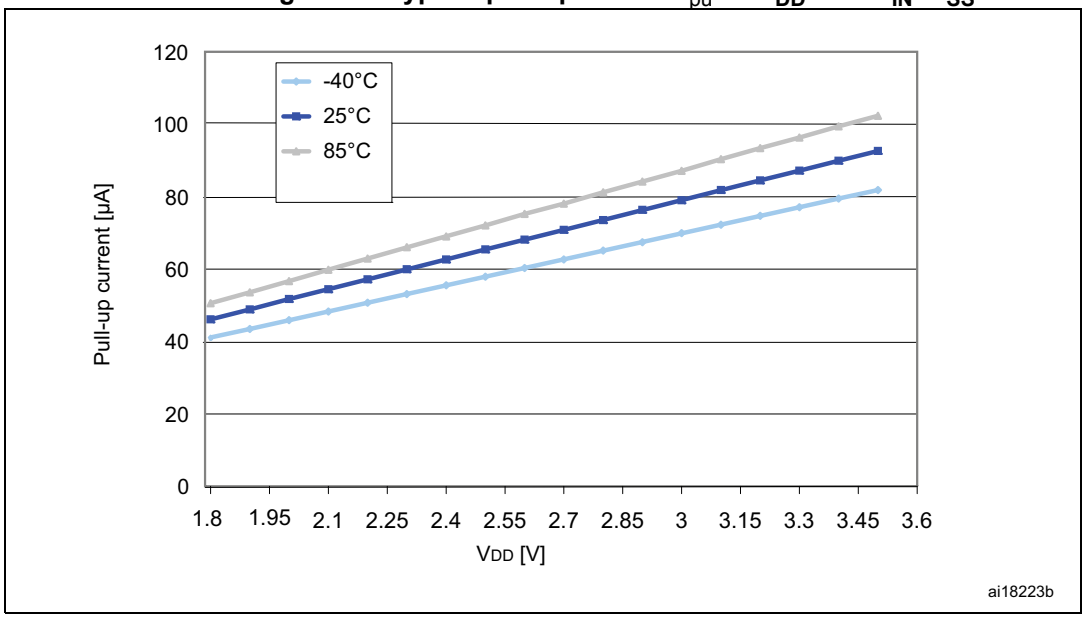


Figure 24. Typical pull-up current I_{pu} vs V_{DD} with $V_{IN}=V_{SS}$



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
High sink	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	V
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	V
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	V
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 40. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 41. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Figure 34. SPI1 timing diagram - slave mode and CPHA=0

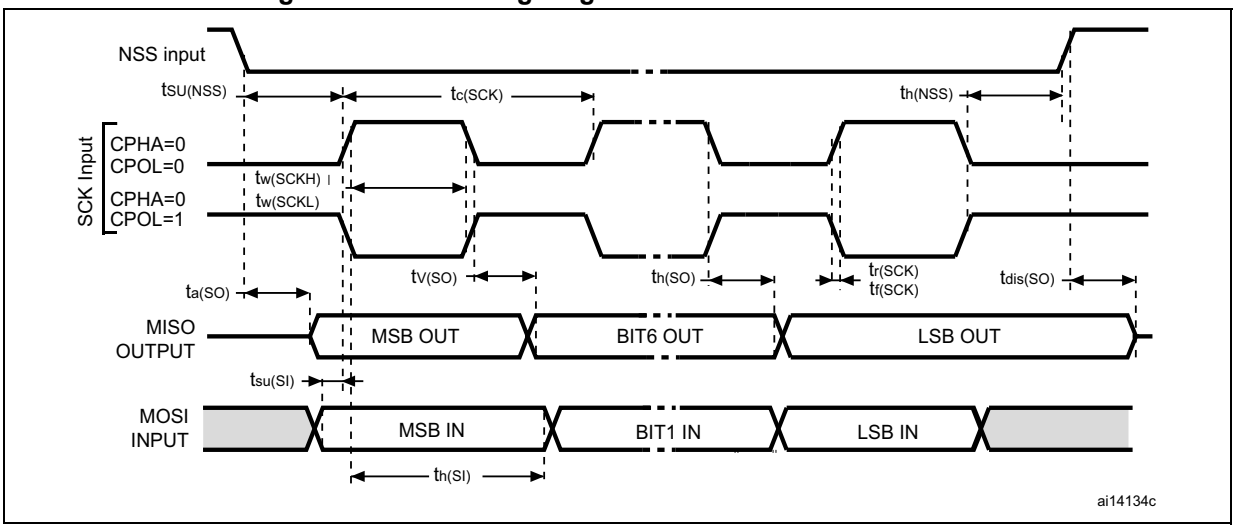
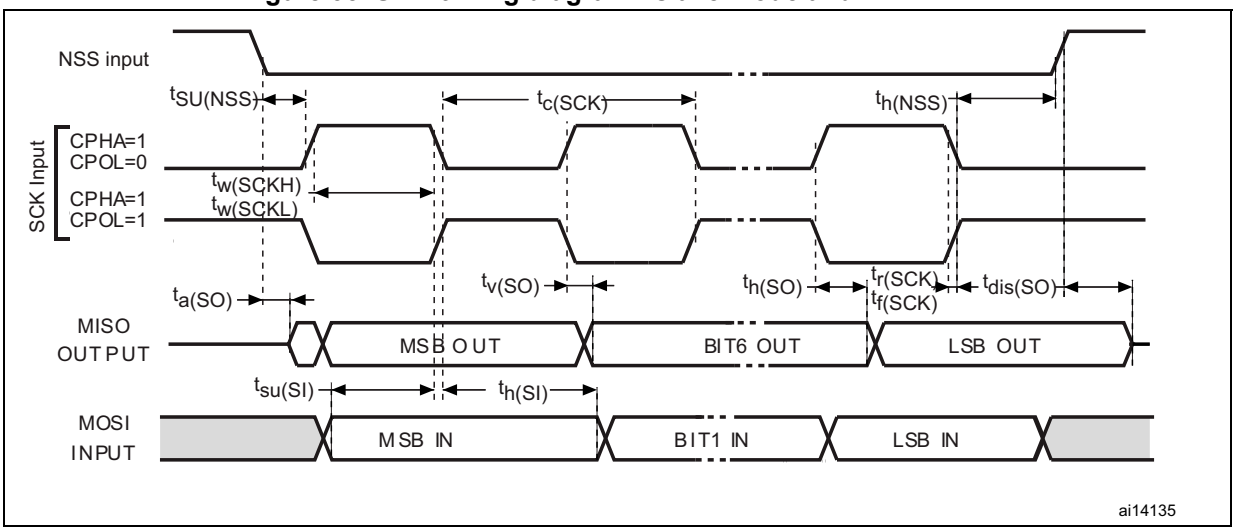


Figure 35. SPI1 timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

9.3.10 Embedded reference voltage

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 46. Reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	µA
$T_{S\_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(2)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202(3)	1.224	1.242(3)	V
I_{LPBUF}(2)	Internal reference voltage low power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(2)	Buffer output current(4)	-	-	-	1	µA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(2)	Internal reference voltage buffer startup time once enabled (1)	-	-	-	10	µs
$ACC_{VREFINT}$	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte(5)	-	-	-	± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	-40 °C ≤T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤T_A ≤ 50 °C	-	-	20	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours	-	-	-	TBD	ppm

1. Defined when ADC output reaches its final value ±1/2LSB
2. Data guaranteed by design.
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guaranty less than 1% V_{REFOUT} deviation.
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

9.3.11 Temperature sensor

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 47. TS characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{90}(1)	Sensor reference voltage at 90°C ±5 °C,	0.580	0.597	0.614	V
T_L	V_{SENSOR} linearity with temperature	-	±1	±2	°C
Avg_slope (2)	Average slope	1.59	1.62	1.65	mV/°C
$I_{DD(TEMP)}$(2)	Consumption	-	3.4	6	µA
T_{START}(2)(3)	Temperature sensor startup time	-	-	10	µs
T_{S_TEMP}(2)	ADC sampling time when reading the temperature sensor	10	-	-	µs

1. Tested in production at V_{DD} = 3 V ±10 mV. The 8 LSB of the V_{90} ADC conversion result are stored in the TS_Factory_CONV_V90 byte.
2. Data guaranteed by design.
3. Defined for ADC output reaching its final value ±1/2LSB.

9.3.12 Comparator characteristics

In the following table, data is guaranteed by design, not tested in production, unless otherwise specified.

Table 48. Comparator 1 characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	1.65	-	3.6	V
T_A	Temperature range	-40	-	125	°C
R_{400K}	R_{400K} value	300	400	500	kΩ
R_{10K}	R_{10K} value	7.5	10	12.5	
V_{IN}	Comparator 1 input voltage range	0.6	-	V_{DDA}	V
V_{REFINT}	Internal reference voltage(2)	1.202	1.224	1.242	
t_{START}	Comparator startup time	-	7	10	µs
t_d	Propagation delay(3)	-	3	10	
V_{offset}	Comparator offset error	-	±3	±10	mV
I_{COMP1}	Current consumption(4)	-	160	260	nA

1. Based on characterization.
2. Tested in production at V_{DD} = 3 V ±10 mV.
3. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
4. Comparator consumption only. Internal reference voltage not included.

9.3.13 12-bit DAC characteristics

In the following table, data is guaranteed by design, not tested in production.

Table 50. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	-	1.8	-	V_{DDA}	
I_{VREF}	Current consumption on V_{REF+} supply	V_{REF+} = 3.3 V, no load, middle code (0x800)	-	130	220	µA
		V_{REF+} = 3.3 V, no load, worst code (0x000)	-	220	350	
I_{VDDA}	Current consumption on V_{DDA} supply	V_{DDA} = 3.3 V, no load, middle code (0x800)	-	210	320	
		V_{DDA} = 3.3 V, no load, worst code (0x000)	-	320	520	
T_A	Temperature range	-	-40	-	125	°C
R_L	Resistive load(1) (2)	DACOUT buffer ON	5	-	-	kΩ
R_O	Output impedance	DACOUT buffer OFF	-	8	10	kΩ
C_L	Capacitive load(3)	-	-	-	50	pF
DAC_OUT	DAC_OUT voltage(4)	DACOUT buffer ON	0.2	-	V_{DDA}-0.2	V
		DACOUT buffer OFF	0	-	V_{REF+} -1 LSB	V
$t_{settling}$	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches the final value ±1LSB)	R_L ≥5 kΩ, C_L≤ 50 pF	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT (@95%) change when small variation of the input code (from code i to i+1LSB).	R_L ≥ 5 kΩ, C_L ≤50 pF	-		1	Msps
t_{WAKEUP}	Wakeup time from OFF state. Input code between lowest and highest possible codes.	R_L ≥5 kΩ, C_L≤50 pF	-	9	15	µs
PSRR+	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	R_L≥ 5 kΩ, C_L≤50 pF	-	-60	-35	dB

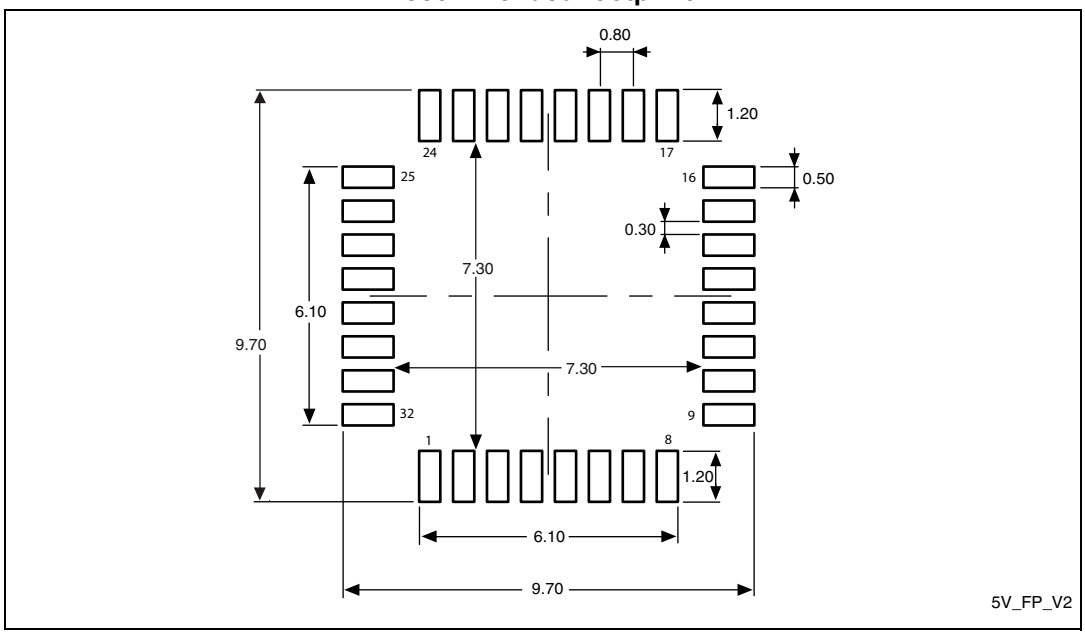
1. Resistive load between DACOUT and GNDA.
2. Output on PF0 (48-pin package only).
3. Capacitive load at DACOUT pin.
4. It gives the output excursion of the DAC.

Table 62. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 50. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint

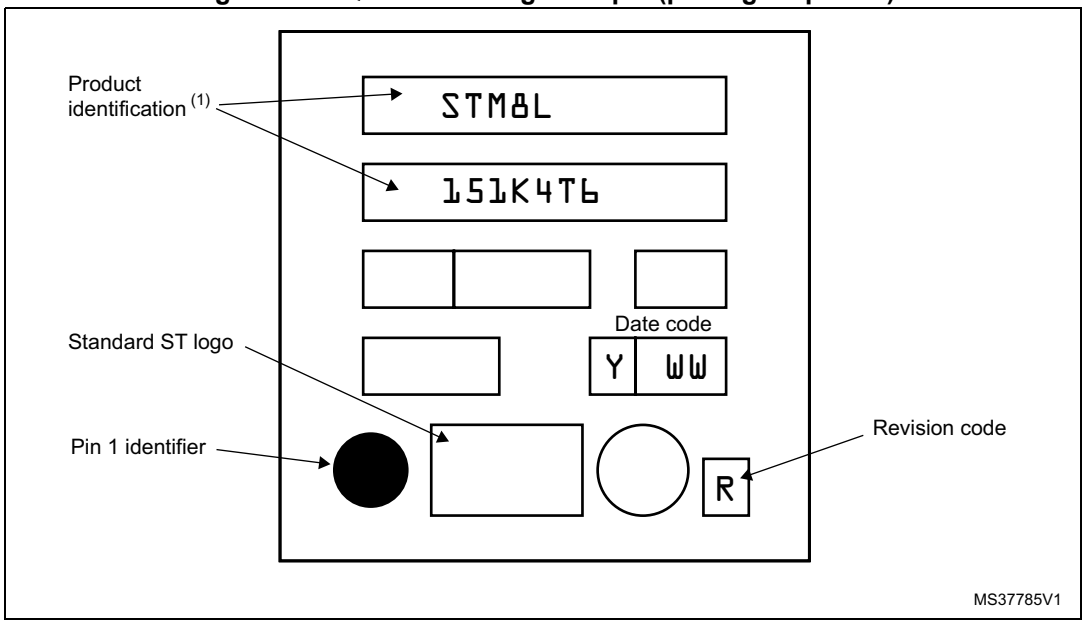


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 51. LQFP32 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering

Table 69. Document revision history (continued)

Date	Revision	Changes
11-Mar-2011	6 cont'd	Modified OPT1 and OPT4 description in *Table: Option byte description.* Updated *Section: Electrical parameters* "standard I/Os" replaced with "high sink I//Os". Updated $R_{HN\ and}$ R_{HN} descriptions in *Table: LCD characteristics.* Added Tape & Reel option to *Figure: Medium density STM8L15x ordering information scheme*.
06-Sep-2011	7	*Features:* updated bullet point concerning capacitive sensing channels. *Section: Low power modes:* updated Wait mode and Halt mode definitions. *Section: Clock management:* added 'kHz' to 32.768 in the 'System clock sources bullet point'. *Section: System configuration controller and routing interface:* replaced last sentence concerning management of charge transfer acquisition sequence. Added *Section: Touchsensing* *Section Development support:* updated the *Bootloader.* *Table: Medium density STM8L15x pin description:* added LQFP32 to second column (same pinout as UFQFPN32); "Timer X - trigger" replaced by "Timer X - external trigger"; added note at the end of this table concerning the slope control of all GPIO pins. *Table: Interrupt mapping:* merged footnotes 1 and 2; updated some of the source blocks and descriptions. *Section: Option bytes*: replaced PM0051 by PM0054 and UM0320 by UM0470. *Table: Option byte description:* replaced the factory default setting (0xAA) for OPT0. *NRST pin:* updated text above the *Figure*; updated *Figure: Recommended NRST pin configuration*. *Table: TS characteristics:* removed typ and max values for the parameter T_{S_TEMP}; added min value for same. *Table: Comparator 1 characteristics:* added typ value for 'Comparator offset error'; added footnote *1.* *Table: Comparator 2 characteristics:* updated t_{START}, t_{dslow}, t_{dfast}, V_{offset}, I_{COMP2}; added footnotes *1.* and *3.* *Table: DAC characteristics:* updated max value for DAC_OUT voltage (DACOUT buffer ON). *Section: 12-bit ADC1 characteristics:* updated. Replaced *Figure: UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline* and *Figure: UFQFPN48 7 x 7 mm recommended footprint (dimensions in mm)*. *Figure: Medium density STM8L15x ordering information scheme*: removed 'TR = Tape & Reel".

Table 69. Document revision history (continued)

Date	Revision	Changes
10-Feb-2012	8	*Features:* replaced "'Dynamic consumption' with 'Consumption'. *Table: Medium density STM8L15x pin description*: updated OD column of NRST/PA1 pin. *Table: Interrupt mapping:* removed tamper 1, tamper 2 and tamper 3. *Figure: UFQFPN48 package outline:* replaced. *Table: UFQFPN48 package mechanical data:* updated title. *Figure: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5):* removed the line over A1. *Figure: UFQFPN28 package outline:* replaced to improve readability of UFQFPN28 package dimensions A, L, and L1. *Figure: Recommended UFQFPN28 footprint (dimensions in mm)*: updated title. *Figure: WLCSP28 package outline:* updated title. *Table: WLCSP28 package mechanical data:* updated title.
02-Mar-2012	9	Updated *Table: UFQFPN48 package mechanical data.* Updated *Figure: UFQFPN28 package outline, Figure: Recommended UFQFPN28 footprint (dimensions in mm)* and *Table: UFQFPN28 package mechanical data.* *Table: WLCSP28 package mechanical data:* Min and Max values removed for e1, e2, e3, e4, F and G dimensions.
30-Mar-2012	10	*Figure: SPI1 timing diagram - master mode(1):* changed SCK signals to 'output' instead of 'input'. *Figure: Medium density STM8L15x ordering information scheme*: added 'Tape & reel' to package section.
26-Apr-2012	11	Updated *Table: WLCSP28 package mechanical data.*
12-Nov-2013	12	Updated *Table: WLCSP28 package mechanical data.* Updated *Table: Medium-density STM8L15x pin description.* Updated *Table 2: Medium density STM8L15x low power device features and peripheral counts*. Added *Figure: Recommended LQFP48 footprint* and *Figure: Recommended LQFP32 footprint.*
12-Aug-2013	13	Changed the default setting value of OPT5 to 0x00 in *Table: Option byte addresses*. Added tTEMP 'BOR detector enabled' and 'disabled' characteristics in *Table: Embedded reset and power control block characteristics*. Updated E2, D2 and ddd in *Table: UFQFPN48 package mechanical data*