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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151c6u3tr

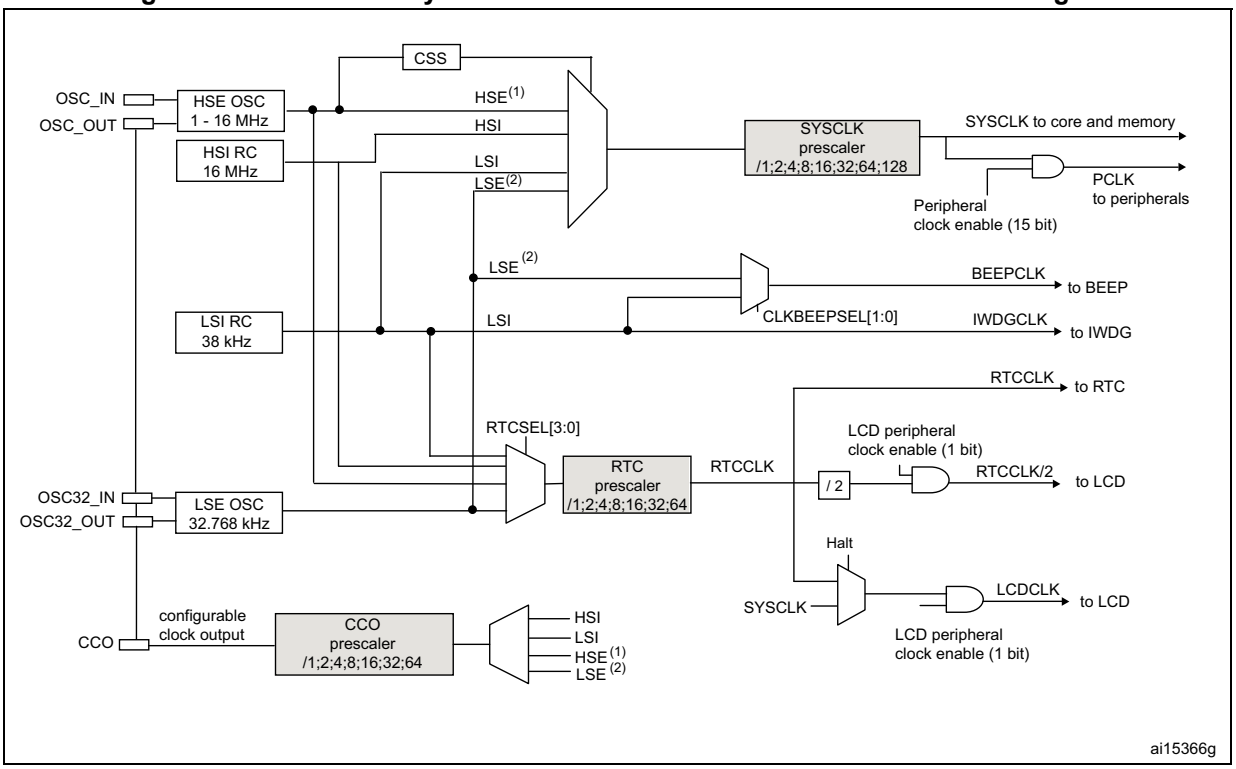
IWDG: Independent watchdog
LCD: Liquid crystal display
POR/PDR: Power on reset / power down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

3.1 Low-power modes

The medium-density STM8L151x4/6 and STM8L152x4/6 devices support five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: The CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt, event or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode). Wait consumption: refer to *Table 21*.
- **Low power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power run mode consumption: refer to *Table 22*.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power wait mode consumption: refer to *Table 23*.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset. Active-halt consumption: refer to *Table 24* and *Table 25*.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs. Halt consumption: refer to *Table 26*.

Figure 2. Medium-density STM8L151x4/6 and STM8L152x4/6 clock tree diagram



1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to *Section HSE clock* in the STM8L15x and STM8L16x reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to *Section LSE clock* in the STM8L15x and STM8L16x reference manual (RM0031).

3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from every second to every year

and STM8L152x4/6 devices, the acquisition sequence is managed by software and it involves analog I/O groups and the routing interface.

Reliable touch sensing solutions can be quickly and easily implemented using the free STM8 Touch Sensing Library.

3.14 Timers

Medium-density STM8L151x4/6 and STM8L152x4/6devices contain one advanced control timer (TIM1), two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 3 compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	up/down	Any integer from 1 to 65536	Yes	3 + 1	3
TIM2			Any power of 2 from 1 to 128		2	None
TIM3						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

3.14.1 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 3 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- 1 additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

3.19 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The single-wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1 interface. The reference document for the bootloader is *UM0560: STM8 bootloader user manual*.

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
30	-	-	-	PB6/[*SPI1_MOSI*](4)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out/slave in]*/ LCD segment 16 / ADC1_IN12 / Comparator 1 positive input
-	19	18	F1	PB6/*[SPI1_MOSI]*(4)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP/ DAC_OUT	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out]*/ slave in / LCD segment 16 / ADC1_IN12 / DAC output / Comparator 1 positive input
31	20	19	E1	PB7/*[SPI1_MISO]*(4)/ LCD_SEG17(2)/ ADC1_IN11/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B7**	*[SPI1 master in- slave out]* / LCD segment 17 / ADC1_IN11 / Comparator 1 positive input
37	25	21	B1	PC0(5)/I2C1_SDA	I/O	FT	**X**		X		T(7)		**Port C0**	I2C1 data
38	26	22	A1	PC1(5)/I2C1_SCL	I/O	FT	**X**		X		T(7)		**Port C1**	I2C1 clock
41	27	23	B2	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREFINT	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6 / Comparator 1 positive input / Internal voltage reference output
42	28	24	A2	PC3/USART1_TX/ LCD_SEG23(2)/ ADC1_IN5/COMP1_INP/ COMP2_INM	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5 / Comparator 1 positive input / Comparator 2 negative input
43	29	25	C2	PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24(2)/ ADC1_IN4/COMP2_INM/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C4**	USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52D2	TIM1	TIM1_DCR2	TIM1 DMA1 control register 2	0x00
0x00 52D3		TIM1_DMA1R	TIM1 DMA1 address for burst mode	0x00
0x00 52D4 to 0x00 52DF	Reserved area (12 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 bytes)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5300 to 0x00 533F	Reserved area (64 bytes)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00

Table 11. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
19	TIM2	TIM2 update/overflow/ trigger/break interrupt	-	-	Yes	Yes	0x00 8054
20	TIM2	TIM2 capture/ compare interrupt	-	-	Yes	Yes	0x00 8058
21	TIM3	TIM3 update/overflow/ trigger/break interrupt	-	-	Yes	Yes	0x00 805C
22	TIM3	TIM3 capture/ compare interrupt	-	-	Yes	Yes	0x00 8060
23	TIM1	Update /overflow/trigger/ COM	-	-	-	Yes	0x00 8064
24	TIM1	Capture/compare	-	-	-	Yes	0x00 8068
25	TIM4	TIM4 update/overflow/ trigger interrupt	-	-	Yes	Yes	0x00 806C
26	SPI1	SPI1 TX buffer empty/ RX buffer not empty/ error/wakeup interrupt	Yes	Yes	Yes	Yes	0x00 8070
27	USART1	USART1 transmit data register empty/ transmission complete interrupt	-	-	Yes	Yes	0x00 8074
28	USART1	USART1 received data ready/overrun error/ idle line detected/parity error/global error interrupt	-	-	Yes	Yes	0x00 8078
29	I^2C1	I^2C1 interrupt(3)	Yes	Yes	Yes	Yes	0x00 807C

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode. In WFE mode, the interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When the interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
2. The interrupt from PVD is logically OR-ed with Port E and F interrupts. Register EXTI_CONF allows to select between Port E and Port F interrupt (see *External interrupt port select register (EXTI_CONF)* in the RM0031).
3. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	- 5 / +0	mA
	Injected current on five-volt tolerant (FT) pins (PA7 and PE0) (1)	- 5 / +0	
	Injected current on 3.6 V tolerant (TT) pins (1)	- 5 / +0	
	Injected current on any other pin (2)	- 5 / +5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) (3)	± 25	

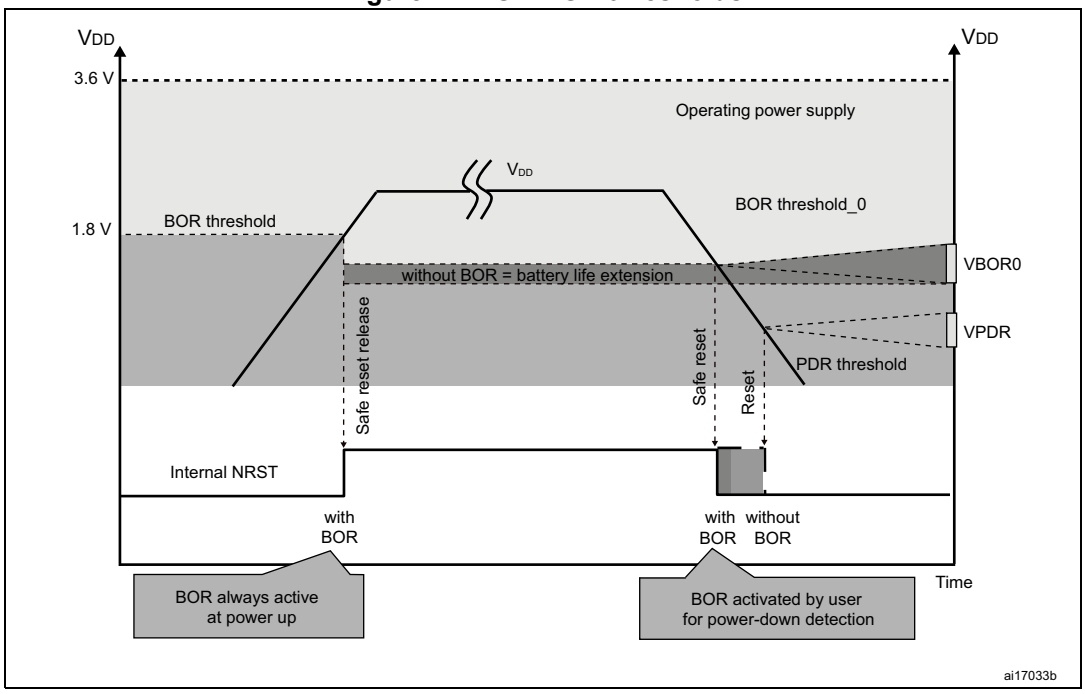
1. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15.* for maximum allowed input voltage values.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15.* for maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

1. Data guaranteed by design.
2. Data based on characterization results.

Figure 12. POR/BOR thresholds



9.3.3 Supply current characteristics

Total current consumption

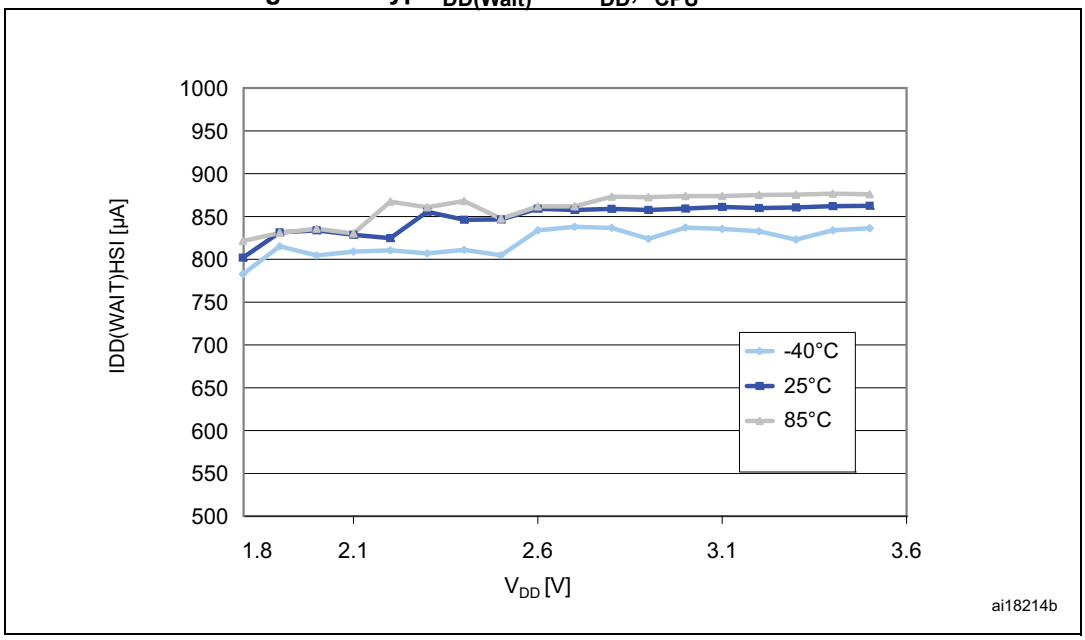
The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

In the following table, data is based on characterization results, unless otherwise specified.

Subject to general operating conditions for V_{DD} and T_A.

Figure 14. Typ. $I_{DD(Wait)}$ vs. V_{DD}, f_{CPU} = 16 MHz [1)]



1. Typical current consumption measured with code executed from Flash memory.

Figure 15. Typ. $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source)

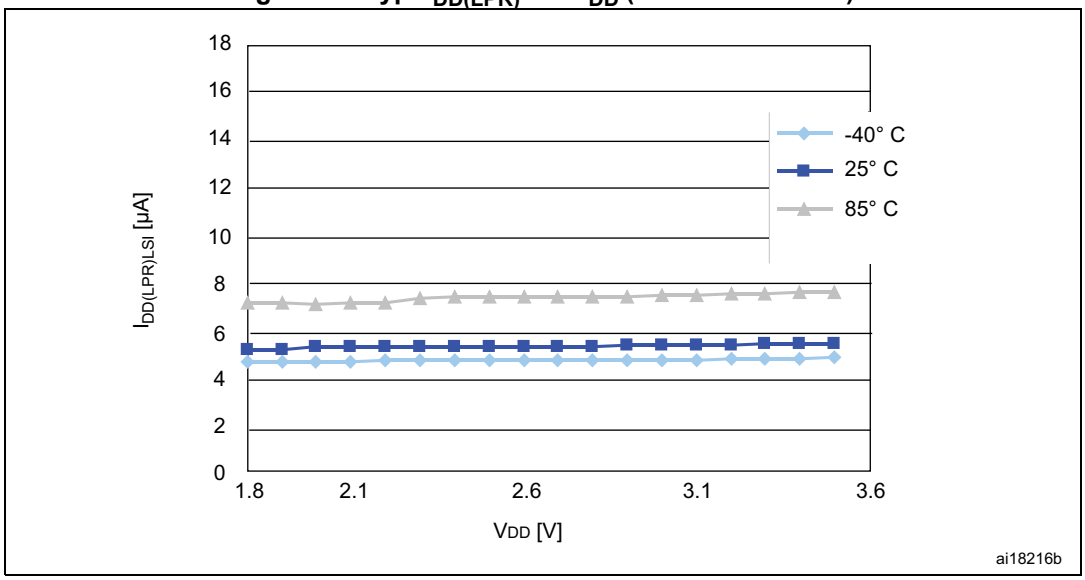
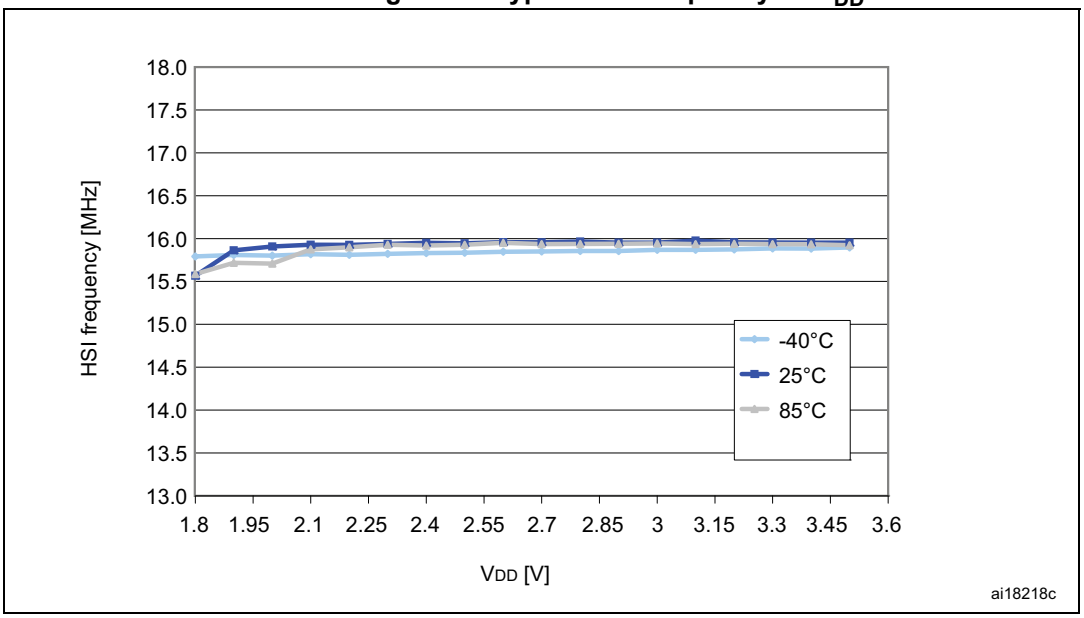


Figure 19. Typical HSI frequency vs V_{DD}



Low speed internal RC oscillator (LSI)

In the following table, data is based on characterization results, not tested in production.

Table 34. LSI oscillator characteristics

Symbol	Parameter (1)	Conditions(1)	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	200(2)	µs
$I_{DD(LSI)}$	LSI oscillator frequency drift(3)	0 °C ≤T_A ≤85 °C	-12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

9.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 35. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory

Table 36. Flash program and data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1 or 64 bytes (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 64 bytes (block) write cycles (on erased byte)	-	-	3	-	ms
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-	0.7	-	
t_{RET} (2)	Data retention (program memory) after 10000 erase/write cycles at T_A= –40 to +85 °C (6 suffix)	T_{RET} = +85 °C	30(1)	-	-	years
	Data retention (program memory) after 10000 erase/write cycles at T_A= –40 to +125 °C (3 suffix)	T_{RET} = +125 °C	5(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A= –40 to +85 °C (6 suffix)	T_{RET} = +85 °C	30(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A= –40 to +125 °C (3 suffix)	T_{RET} = +125 °C	5(1)	-	-	
N_{RW} (3)	Erase/write cycles (program memory)	T_A = –40 to +85 °C (6 suffix), T_A = –40 to +125 °C (3 suffix)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)		300(1) (4)	-	-	

1. Data based on characterization results.
2. Conforming to JEDEC JESD22a117
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.
4. Data based on characterization performed on the whole data memory.

9.3.6 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

Table 37. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on true open-drain pins (PC0 and PC1)	-5	+0	mA
	Injected current on all five-volt tolerant (FT) pins	-5	+0	
	Injected current on all 3.6 V tolerant (TT) pins	-5	+0	
	Injected current on any other pin	-5	+5	

9.3.7 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 24*).

Figure 21. Typical V_{IL} and V_{IH} vs V_{DD} (high sink I/Os)

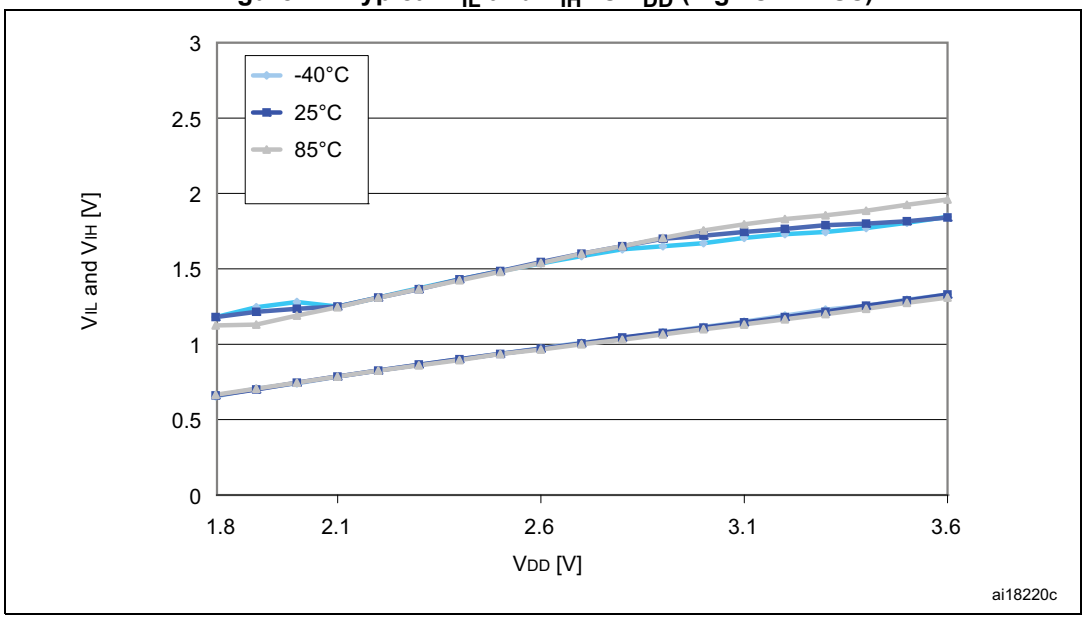
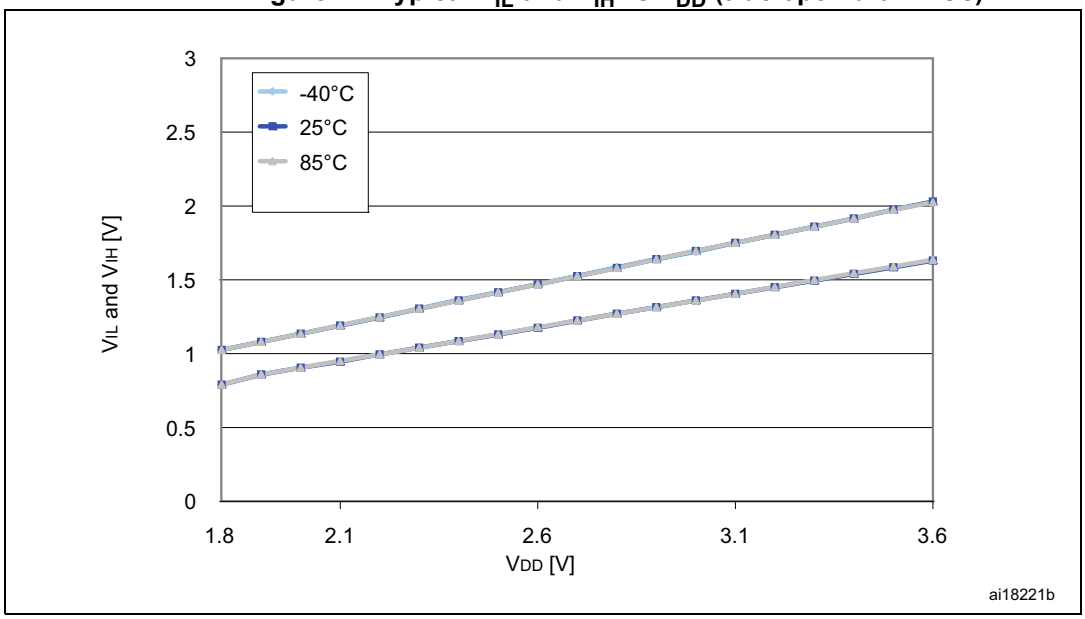


Figure 22. Typical V_{IL} and V_{IH} vs V_{DD} (true open drain I/Os)



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
High sink	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	V
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	V
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	V
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 40. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 41. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

9.3.9 LCD controller (STM8L152xx only)

In the following table, data is guaranteed by design. Not tested in production.

Table 45. LCD characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	V
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	V
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	V
V_{LCD3}	LCD internal reference voltage 3	-	2.9	-	V
V_{LCD4}	LCD internal reference voltage 4	-	3.0	-	V
V_{LCD5}	LCD internal reference voltage 5	-	3.1	-	V
V_{LCD6}	LCD internal reference voltage 6	-	3.2	-	V
V_{LCD7}	LCD internal reference voltage 7	-	3.3	-	V
C_{EXT}	V_{LCD} external capacitance	0.1	-	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	µA
R_{HN} (2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN} (3)	Low value resistive network (high drive)	-	360	-	kΩ
V_{33}	Segment/Common higher level voltage	-	-	V_{LCDx}	V
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	V
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	V
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	V
V_0	Segment/Common lowest level voltage	0	-	-	V

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8L152xx only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 45*.

In the following table, data is guaranteed by design, not tested in production.

Table 49. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
T_A	Temperature range	-	-40	-	125	°C
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay in slow mode(2)	1.65 V ≤V_{DDA} ≤2.7 V	-	1.8	3.5	
		2.7 V ≤V_{DDA} ≤3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay in fast mode(2)	1.65 V ≤V_{DDA} ≤2.7 V	-	0.8	2	
		2.7 V ≤V_{DDA} ≤3.6 V	-	1.2	4	
V_{offset}	Comparator offset error	-	-	±4	±20	mV
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Based on characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Figure 41. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

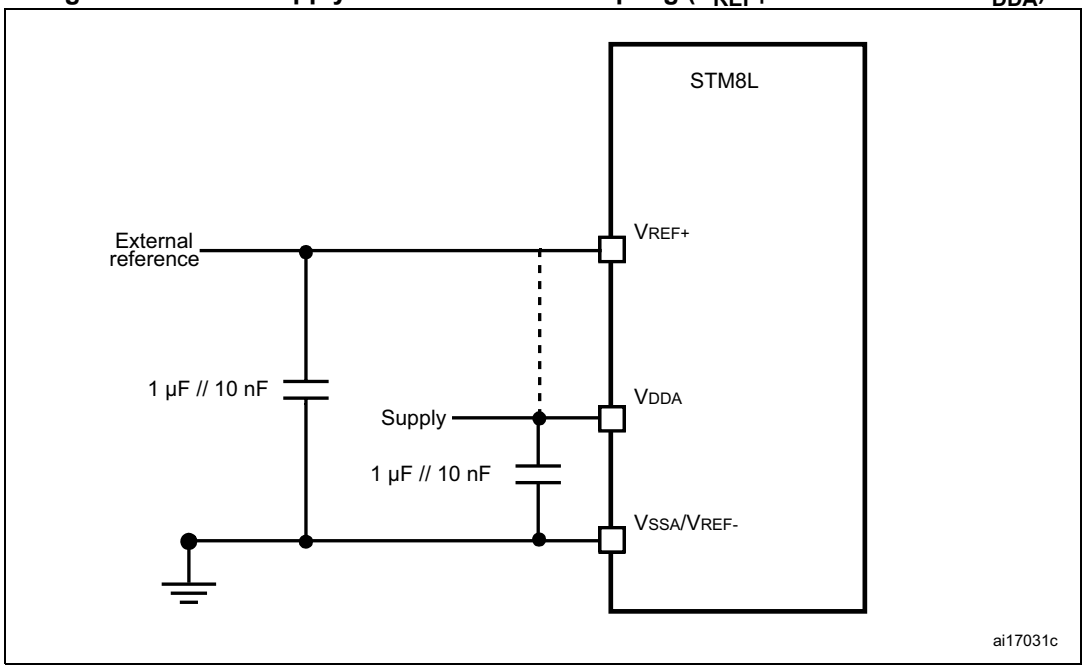
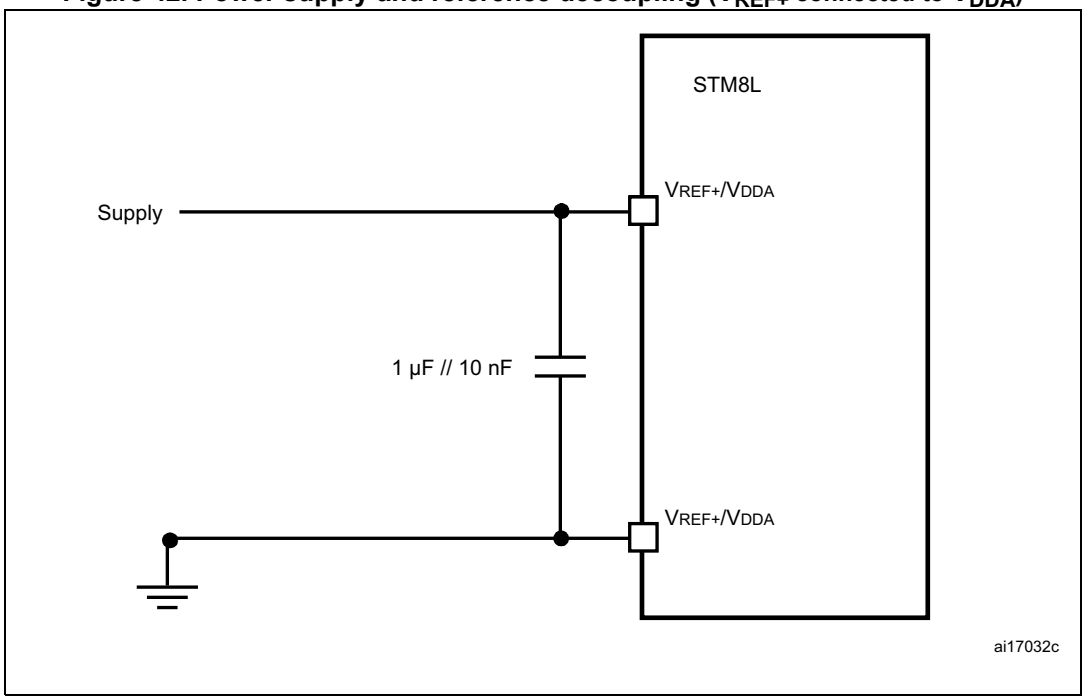
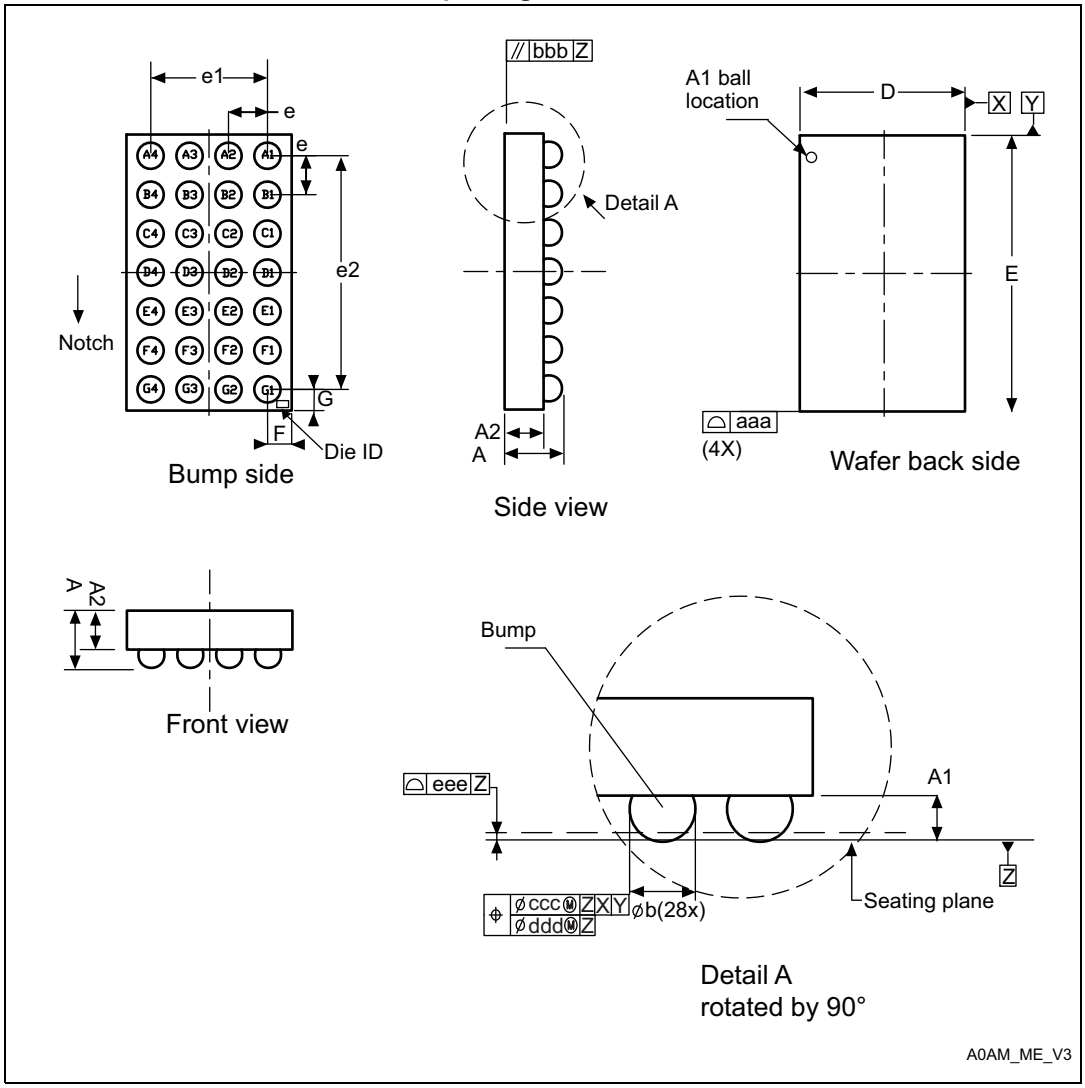


Figure 42. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



10.7 WLCSP28 package information

Figure 58. WLCSP28 - 28-pin, 1.703 x 2.841 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.