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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151c6u6tr

2.1 Device overview

Table 2. Medium-density STM8L151x4/6 and STM8L152x4/6 low-power device features and peripheral counts

Features		STM8L151Gx		STM8L15xKx		STM8L15xCx	
Flash (Kbyte)		16	32	16	32	16	32
Data EEPROM (Kbyte)		1					
RAM (Kbyte)		2					
LCD		No		4x17 (1)		4x28 (1)	
Timers	Basic	1 (8-bit)					
	General purpose	2 (16-bit)					
	Advanced control	1 (16-bit)					
Communication interfaces	SPI	1					
	I2C	1					
	USART	1					
GPIOs		26(3)		30 (2)(3) or 29 (1)(3)		41(3)	
12-bit synchronized ADC (number of channels)		1 (18)		1 (22 (2) or 21 (1))		1 (25)	
12-Bit DAC (number of channels)		1 (1)					
Comparators COMP1/COMP2		2					
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator					
CPU frequency		16 MHz					
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power down)					
Operating temperature		-40 to +85 °C/ -40 to +105 °C / -40 to +125 °C					
Packages		UFQFPN28 (4x4; 0.6 mm thickness) WLCSP28		LQFP32(7x7) UFQFPN32 (5x5; 0.6 mm thickness)		LQFP48 UFQFPN48 (4x4; 0.6 mm thickness)	

1. STM8L152xx versions only
2. STM8L151xx versions only
3. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

2.2 Ultra-low-power continuum

The ultra-low-power medium-densitySTM8L151x4/6 and STM8L152x4/6 devices are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101xx and STM8L15xxx. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13 µm ultra-low leakage process.

Note: 1 The STM8L151xx and STM8L152xx are pin-to-pin compatible with STM8L101xx devices.

2 The STM32L family is pin-to-pin compatible with the general purpose STM32F family. Please refer to STM32L15x documentation for more information on these devices.

Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM® Cortex®-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

Shared peripherals

STM8L151xx/152xx and STM8L15xxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC1, DAC, and comparators COMP1/COMP2
- Digital peripherals: RTC and some communication interfaces

Common system strategy

To offer flexibility and optimize performance, the STM8L151xx/152xx and STM8L15xxx devices use a common architecture:

- Same power supply range from 1.8 to 3.6 V, down to 1.65 V at power down
- Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy for both STM8L15x and STM32L15xxx including power-on reset, power-down reset, brownout reset and programmable voltage detector.

Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbyte

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
30	-	-	-	PB6/[*SPI1_MOSI*](4)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out/slave in]*/ LCD segment 16 / ADC1_IN12 / Comparator 1 positive input
-	19	18	F1	PB6/*[SPI1_MOSI]*(4)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP/ DAC_OUT	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out]*/ slave in / LCD segment 16 / ADC1_IN12 / DAC output / Comparator 1 positive input
31	20	19	E1	PB7/*[SPI1_MISO]*(4)/ LCD_SEG17(2)/ ADC1_IN11/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B7**	*[SPI1 master in- slave out]* / LCD segment 17 / ADC1_IN11 / Comparator 1 positive input
37	25	21	B1	PC0(5)/I2C1_SDA	I/O	FT	**X**		X		T(7)		**Port C0**	I2C1 data
38	26	22	A1	PC1(5)/I2C1_SCL	I/O	FT	**X**		X		T(7)		**Port C1**	I2C1 clock
41	27	23	B2	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREFINT	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6 / Comparator 1 positive input / Internal voltage reference output
42	28	24	A2	PC3/USART1_TX/ LCD_SEG23(2)/ ADC1_IN5/COMP1_INP/ COMP2_INM	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5 / Comparator 1 positive input / Comparator 2 negative input
43	29	25	C2	PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24(2)/ ADC1_IN4/COMP2_INM/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C4**	USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
44	30	26	A3	PC5/OSC32_IN /*[SPI1_NSS]*(4)/ *[USART1_TX]*(4)	I/O		**X**	X	X	HS	X	X	**Port C5**	LSE oscillator input / *[SPI1 master/slave select] / [USART1 transmit]*
45	31	27	B3	PC6/OSC32_OUT/ *[SPI1_SCK]*(4)/ *[USART1_RX]*(4)	I/O		**X**	X	X	HS	X	X	**Port C6**	LSE oscillator output / *[SPI1 clock] / [USART1 receive]*
46	-	-	-	PC7/LCD_SEG25(2)/ ADC1_IN3/COMP2_INM/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C7**	LCD segment 25 /ADC1_IN3/ Comparator negative input / Comparator 1 positive input
20	-	8	G3	PD0/TIM3_CH2/ *[ADC1_TRIG]*(4)/ LCD_SEG7(2)/ADC1_IN22/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / LCD segment 7 / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input
-	9	-	-	PD0/TIM3_CH2/ *[ADC1_TRIG]*(4)/ ADC1_IN22/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D0(8)**	Timer 3 - channel 2 / *[ADC1_Trigger]* / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input
21	-	-	-	PD1/TIM3_ETR/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - external trigger / LCD_COM3 / ADC1_IN21 / comparator 2 positive input / Comparator 1 positive input
-	10	-	-	PD1/TIM1_CH3N/[*TIM3_ETR*](4)/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D1**	*[Timer 3 - external trigger]/* TIM1 inverted channel 3 / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 501E to 0x00 5049	Reserved area (28 bytes)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5084	DMA1	Reserved area (1 byte)		
0x00 5085		DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088		Reserved area (2 bytes)		
0x00 5089		DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092		Reserved area (2 bytes)		
0x00 5093		DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		Reserved area (1 byte)		
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509D		Reserved area (3 bytes)		
0x00 509E	SYSCFG	SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_DIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00
0x00 50C2		CLK_ICKR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x80
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0bxxxx0000
0x00 50CA		CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0xxx
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11100x

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52D2	TIM1	TIM1_DCR2	TIM1 DMA1 control register 2	0x00
0x00 52D3		TIM1_DMA1R	TIM1 DMA1 address for burst mode	0x00
0x00 52D4 to 0x00 52DF	Reserved area (12 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 bytes)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5300 to 0x00 533F	Reserved area (64 bytes)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5430	RI	Reserved area (1 byte)		0x00
0x00 5431		RI_ICR1	Timer input capture routing register 1	0x00
0x00 5432		RI_ICR2	Timer input capture routing register 2	0x00
0x00 5433		RI_IOIR1	I/O input register 1	undefined
0x00 5434		RI_IOIR2	I/O input register 2	undefined
0x00 5435		RI_IOIR3	I/O input register 3	undefined
0x00 5436		RI_IOCMR1	I/O control mode register 1	0x00
0x00 5437		RI_IOCMR2	I/O control mode register 2	0x00
0x00 5438		RI_IOCMR3	I/O control mode register 3	0x00
0x00 5439		RI_IOSR1	I/O switch register 1	0x00
0x00 543A		RI_IOSR2	I/O switch register 2	0x00
0x00 543B		RI_IOSR3	I/O switch register 3	0x00
0x00 543C		RI_IOGCR	I/O group control register	0x3F
0x00 543D		RI_ASCR1	Analog switch register 1	0x00
0x00 543E		RI_ASCR2	Analog switch register 2	0x00
0x00 543F		RI_RCR	Resistor control register 1	0x00
0x00 5440	COMP	COMP_CSR1	Comparator control and status register 1	0x00
0x00 5441		COMP_CSR2	Comparator control and status register 2	0x00
0x00 5442		COMP_CSR3	Comparator control and status register 3	0x00
0x00 5443		COMP_CSR4	Comparator control and status register 4	0x00
0x00 5444		COMP_CSR5	Comparator control and status register 5	0x00

1. These registers are not impacted by a system reset. They are reset at power-on.

Table 28. Current consumption under external reset

Symbol	Parameter	Conditions		Typ	Unit
$I_{DD(RST)}$	Supply current under external reset (1)	All pins are externally tied to V_{DD}	V_{DD} = 1.8 V	48	µA
			V_{DD} = 3 V	76	
			V_{DD} = 3.6 V	91	

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset.

9.3.4 Clock and timing characteristics

HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 29. HSE external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency(1)	-	1	-	16	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7 x V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	0.3 x V_{DD}	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	2.6	-	pF
I_{LEAK_HSE}	OSC_IN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-	-	±1	µA

1. Data guaranteed by design.

LSE external clock (LSEBYP=1 in CLK_ECKCR)

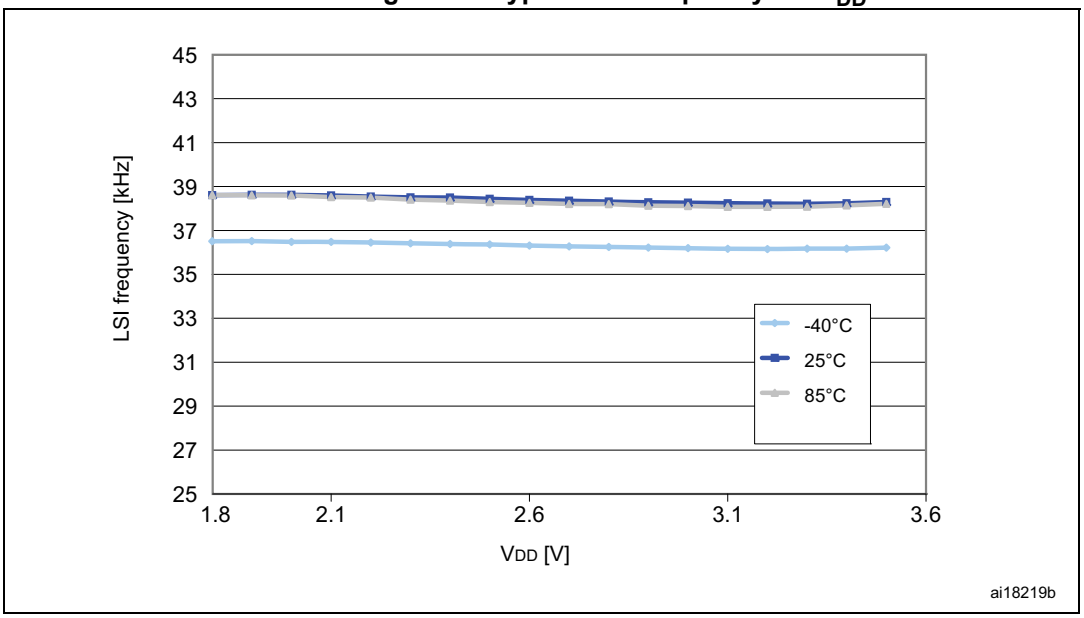
Subject to general operating conditions for V_{DD} and T_A.

Table 30. LSE external clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency(1)	-	32.768	-	kHz
V_{LSEH}(2)	OSC32_IN input pin high level voltage	0.7 x V_{DD}	-	V_{DD}	V
V_{LSEL}(2)	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 x V_{DD}	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	0.6	-	pF
I_{LEAK_LSE}	OSC32_IN input leakage current	-	-	±1	µA

1. Data guaranteed by design.
2. Data based on characterization results.

Figure 20. Typical LSI frequency vs. V_{DD}



9.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 35. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory

Table 36. Flash program and data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1 or 64 bytes (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 64 bytes (block) write cycles (on erased byte)	-	-	3	-	ms
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-	0.7	-	
t_{RET} (2)	Data retention (program memory) after 10000 erase/write cycles at T_A= –40 to +85 °C (6 suffix)	T_{RET} = +85 °C	30(1)	-	-	years
	Data retention (program memory) after 10000 erase/write cycles at T_A= –40 to +125 °C (3 suffix)	T_{RET} = +125 °C	5(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A= –40 to +85 °C (6 suffix)	T_{RET} = +85 °C	30(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A= –40 to +125 °C (3 suffix)	T_{RET} = +125 °C	5(1)	-	-	
N_{RW} (3)	Erase/write cycles (program memory)	T_A = –40 to +85 °C (6 suffix), T_A = –40 to +125 °C (3 suffix)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)		300(1) (4)	-	-	

1. Data based on characterization results.
2. Conforming to JEDEC JESD22a117
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.
4. Data based on characterization performed on the whole data memory.

Table 38. I/O static characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
V_{IL}	Input low level voltage(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS}-0.3	-	0.3 x V_{DD}	V
		Input voltage on five-volt tolerant (FT) pins (PA7 and PE0)	V_{SS}-0.3	-	0.3 x V_{DD}	
		Input voltage on 3.6 V tolerant (TT) pins	V_{SS}-0.3	-	0.3 x V_{DD}	
		Input voltage on any other pin	V_{SS}-0.3	-	0.3 x V_{DD}	
V_{IH}	Input high level voltage (2)	Input voltage on true open-drain pins (PC0 and PC1) with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	V
		Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD} \geq 2$ V		-	5.5	
		Input voltage on five-volt tolerant (FT) pins (PA7 and PE0) with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	
		Input voltage on five-volt tolerant (FT) pins (PA7 and PE0) with $V_{DD} \geq 2$ V		-	5.5	
		Input voltage on 3.6 V tolerant (TT) pins		-	3.6	
		Input voltage on any other pin	0.70 x V_{DD}	-	V_{DD}+0.3	
V_{hys}	Schmitt trigger voltage hysteresis (3)	I/Os	-	200	-	mV
		True open drain I/Os	-	200	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ High sink I/Os	-	-	50 (5)	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200(5)	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200(5)	
R_{PU}	Weak pull-up equivalent resistor(2)(6)	$V_{IN}=V_{SS}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Data based on characterization results.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.

Figure 23. Typical pull-up resistance R_{PU} vs V_{DD} with $V_{IN}=V_{SS}$

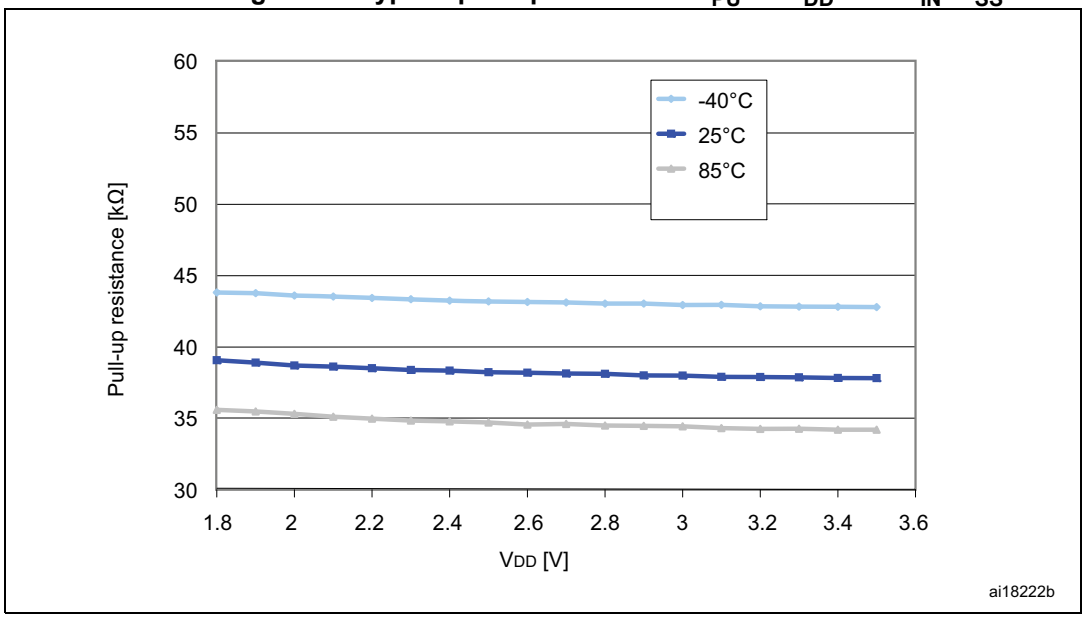
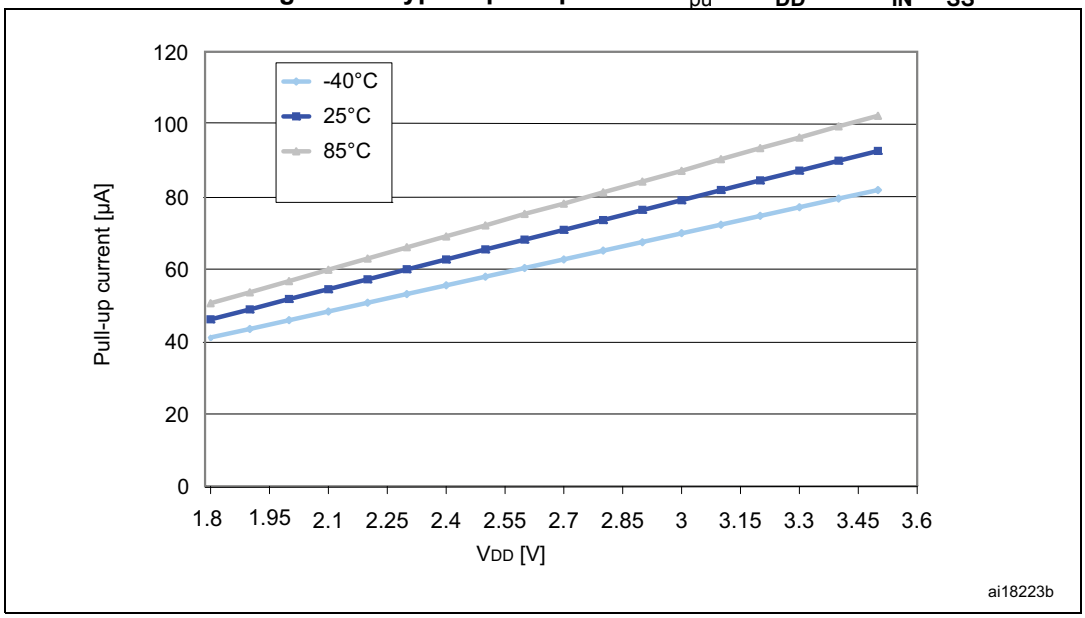


Figure 24. Typical pull-up current I_{pu} vs V_{DD} with $V_{IN}=V_{SS}$



9.3.10 Embedded reference voltage

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 46. Reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	µA
$T_{S\_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(2)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202(3)	1.224	1.242(3)	V
I_{LPBUF}(2)	Internal reference voltage low power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(2)	Buffer output current(4)	-	-	-	1	µA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(2)	Internal reference voltage buffer startup time once enabled (1)	-	-	-	10	µs
$ACC_{VREFINT}$	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte(5)	-	-	-	± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	-40 °C ≤T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤T_A ≤ 50 °C	-	-	20	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours	-	-	-	TBD	ppm

1. Defined when ADC output reaches its final value ±1/2LSB
2. Data guaranteed by design.
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guaranty less than 1% V_{REFOUT} deviation.
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

Figure 40. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

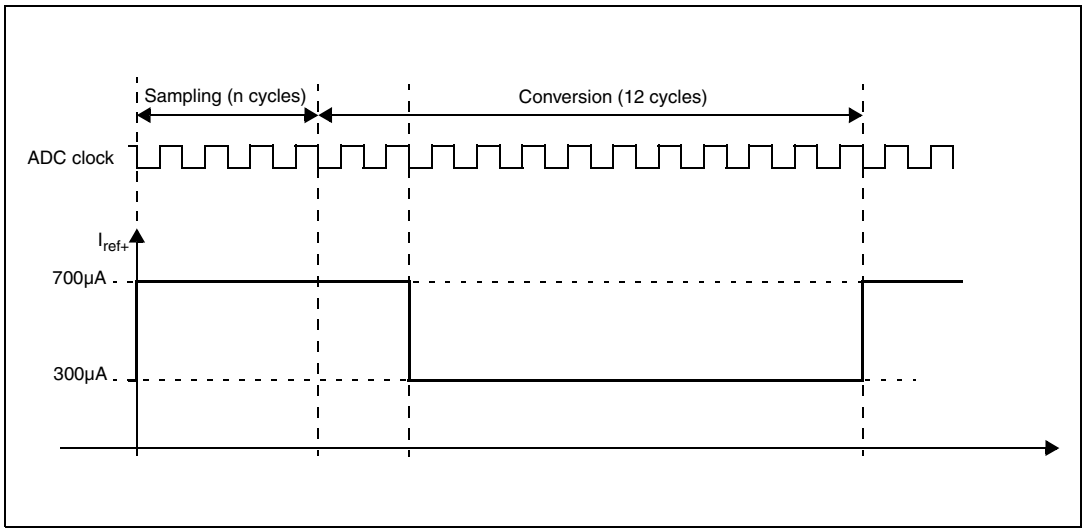


Table 57. R_{AIN} max for f_{ADC} = 16 MHz(1)

Ts (cycles)	Ts (µs)	R_{AIN} max (kohm)			
		Slow channels		Fast channels	
		2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA} < 3.3 V	1.8 V < V_{DDA} < 2.4 V
4	0.25	Not allowed	Not allowed	0.7	Not allowed
9	0.5625	0.8	Not allowed	2.0	1.0
16	1	2.0	0.8	4.0	3.0
24	1.5	3.0	1.8	6.0	4.5
48	3	6.8	4.0	15.0	10.0
96	6	15.0	10.0	30.0	20.0
192	12	32.0	25.0	50.0	40.0
384	24	50.0	50.0	50.0	50.0

1. Guaranteed by design.

General PCB design guidelines

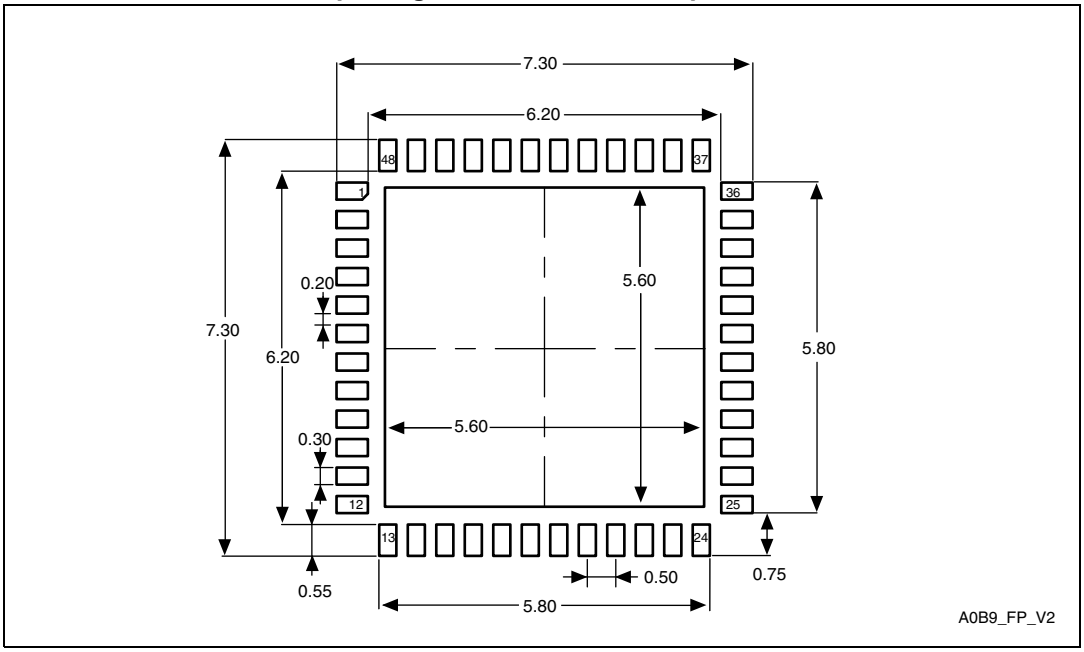
Power supply decoupling should be performed as shown in *Figure 41* or *Figure 42*, depending on whether V_{REF+} is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

Table 63. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 69. Document revision history (continued)

Date	Revision	Changes
21-Apr-2015	14	Added: – *Figure 45: LQFP48 marking example (package top view)*, – *Figure 48: UFQFPN48 marking example (package top view)*, – *Figure 51: LQFP32 marking example (package top view)*, – *Figure 54: UFQFPN32 marking example (package top view)*, – *Figure 57: UFQFPN28 marking example (package top view)*, – *Figure 59: WLCSP28 marking example (package top view)*.
07-Apr-2017	15	Changed symbol V_{125} to V_{90} in *Table 47: TS characteristics* and updated related Min/Typ/Max values. Updated *Section 9.2: Absolute maximum ratings*. Updated table notes for *Table 30*, *Table 31*, *Table 32*, *Table 33*, *Table 34*, *Table 36*, *Table 38*, *Table 42*, *Table 43*, *Table 46*, *Table 47*, *Table 48*, *Table 49*, *Table 53*, *Table 57*, and *Table 60*. Updated device marking paragraphs in *Section 10.2*, *Section 10.3*, *Section 10.4*, *Section 10.5*, *Section 10.6*, and *Section 10.7*.