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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFBGA, WLCSP
Supplier Device Package	28-WLCSP (1.7x2.84)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151g4y3tr

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2 Description

The medium-density STM8L151x4/6 and STM8L152x4/6 devices are members of the STM8L ultra-low-power 8-bit family. The medium-density STM8L15x family operates from 1.8 V to 3.6 V (down to 1.65 V at power down) and is available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

The medium-density STM8L15x ultra-low-power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive In-Application debugging and ultra-fast Flash programming.

All medium-density STM8L15x microcontrollers feature embedded data EEPROM and low-power, low-voltage, single-supply program Flash memory.

They incorporate an extensive range of enhanced I/Os and peripherals.

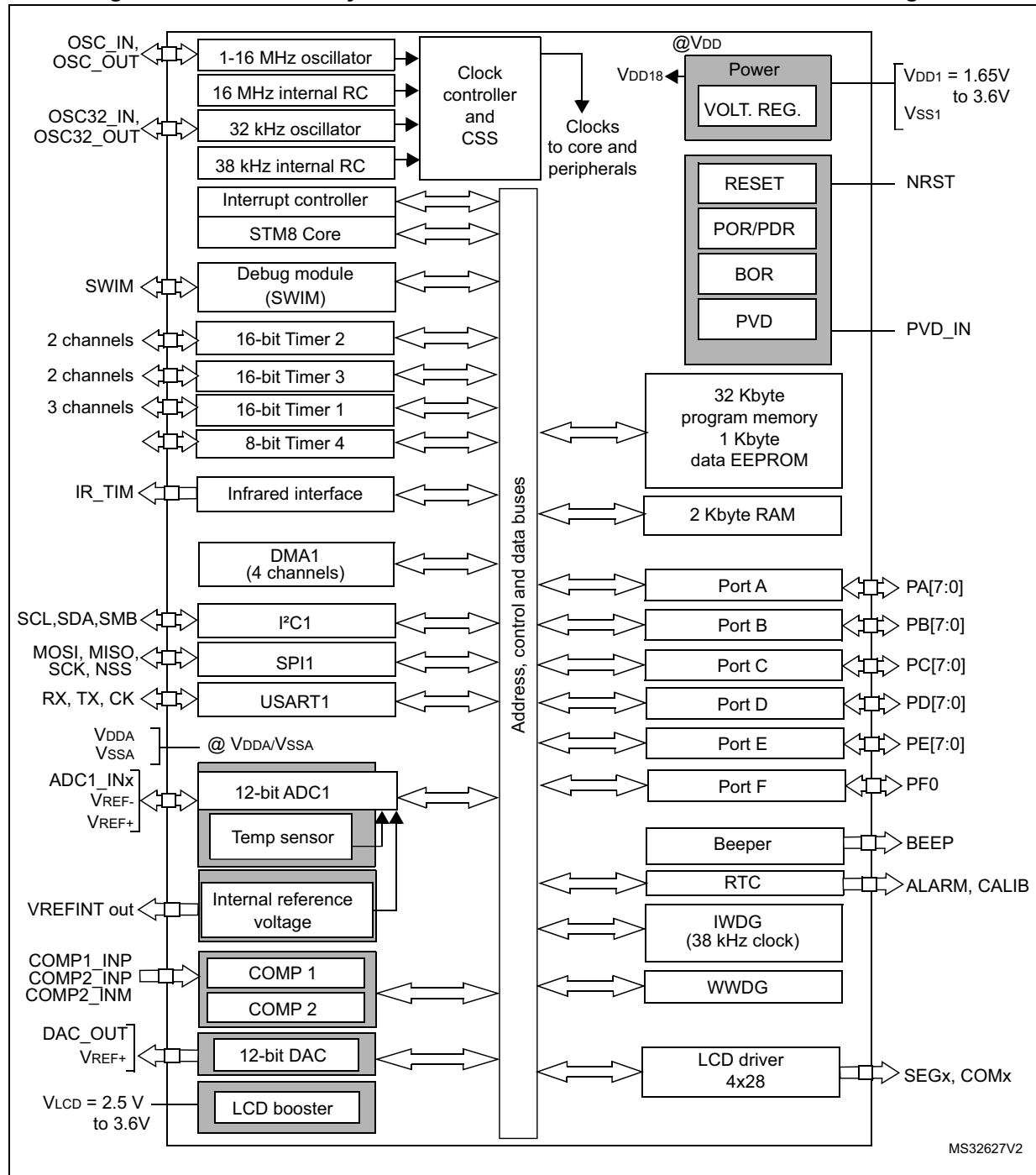
The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

Six different packages are proposed from 28 to 48 pins. Depending on the device chosen, different sets of peripherals are included.

All STM8L ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

3 Functional overview

Figure 1. Medium-density STM8L151x4/6 and STM8L152x4/6 device block diagram



1. **Legend:**
 ADC: Analog-to-digital converter
 BOR: Brownout reset
 DMA: Direct memory access
 DAC: Digital-to-analog converter
 I²C: Inter-integrated circuit multi master interface

3.6 LCD (Liquid crystal display)

The liquid crystal display drives up to 4 common terminals and up to 28 segment terminals to drive up to 112 pixels.

- Internal step-up converter to guarantee contrast control whatever V_{DD} .
- Static 1/2, 1/3, 1/4 duty supported.
- Static 1/2, 1/3 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 4 pixels which can be programmed to blink.
- The LCD controller can operate in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The medium-density STM8L151x4/6 and STM8L152x4/6 devices have the following main features:

- Up to 2 Kbyte of RAM
- The non-volatile memory is divided into three arrays:
 - Up to 32 Kbyte of medium-density embedded Flash program memory
 - 1 Kbyte of data EEPROM
 - Option bytes.

The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC, I2C1, SPI1, USART1, the four Timers.

3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 25 channels (including 1 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 μ s with f_{SYSCLK} = 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

and STM8L152x4/6 devices, the acquisition sequence is managed by software and it involves analog I/O groups and the routing interface.

Reliable touch sensing solutions can be quickly and easily implemented using the free STM8 Touch Sensing Library.

3.14 Timers

Medium-density STM8L151x4/6 and STM8L152x4/6 devices contain one advanced control timer (TIM1), two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

[Table 3](#) compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	up/down	Any integer from 1 to 65536	Yes	3 + 1	3
TIM2			Any power of 2 from 1 to 128		2	None
TIM3						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

3.14.1 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 3 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- 1 additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52B0	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 52B1		TIM1_CR2	TIM1 control register 2	0x00
0x00 52B2		TIM1_SMCR	TIM1 Slave mode control register	0x00
0x00 52B3		TIM1_ETR	TIM1 external trigger register	0x00
0x00 52B4		TIM1_DER	TIM1 DMA1 request enable register	0x00
0x00 52B5		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 52B6		TIM1_SR1	TIM1 status register 1	0x00
0x00 52B7		TIM1_SR2	TIM1 status register 2	0x00
0x00 52B8		TIM1_EGR	TIM1 event generation register	0x00
0x00 52B9		TIM1_CCMR1	TIM1 Capture/Compare mode register 1	0x00
0x00 52BA		TIM1_CCMR2	TIM1 Capture/Compare mode register 2	0x00
0x00 52BB		TIM1_CCMR3	TIM1 Capture/Compare mode register 3	0x00
0x00 52BC		TIM1_CCMR4	TIM1 Capture/Compare mode register 4	0x00
0x00 52BD		TIM1_CCER1	TIM1 Capture/Compare enable register 1	0x00
0x00 52BE		TIM1_CCER2	TIM1 Capture/Compare enable register 2	0x00
0x00 52BF		TIM1_CNTRH	TIM1 counter high	0x00
0x00 52C0		TIM1_CNTRL	TIM1 counter low	0x00
0x00 52C1		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 52C2		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 52C3		TIM1_ARRH	TIM1 Auto-reload register high	0xFF
0x00 52C4		TIM1_ARRL	TIM1 Auto-reload register low	0xFF
0x00 52C5		TIM1_RCR	TIM1 Repetition counter register	0x00
0x00 52C6		TIM1_CCR1H	TIM1 Capture/Compare register 1 high	0x00
0x00 52C7		TIM1_CCR1L	TIM1 Capture/Compare register 1 low	0x00
0x00 52C8		TIM1_CCR2H	TIM1 Capture/Compare register 2 high	0x00
0x00 52C9		TIM1_CCR2L	TIM1 Capture/Compare register 2 low	0x00
0x00 52CA		TIM1_CCR3H	TIM1 Capture/Compare register 3 high	0x00
0x00 52CB		TIM1_CCR3L	TIM1 Capture/Compare register 3 low	0x00
0x00 52CC		TIM1_CCR4H	TIM1 Capture/Compare register 4 high	0x00
0x00 52CD		TIM1_CCR4L	TIM1 Capture/Compare register 4 low	0x00
0x00 52CE		TIM1_BKR	TIM1 break register	0x00
0x00 52CF		TIM1_DTR	TIM1 dead-time register	0x00
0x00 52D0		TIM1_OISR	TIM1 output idle state register	0x00
0x00 52D1		TIM1_DCR1	DMA1 control register 1	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52D2	TIM1	TIM1_DCR2	TIM1 DMA1 control register 2	0x00
0x00 52D3		TIM1_DMA1R	TIM1 DMA1 address for burst mode	0x00
0x00 52D4 to 0x00 52DF	Reserved area (12 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 bytes)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5300 to 0x00 533F	Reserved area (64 bytes)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00

6 Interrupt vector mapping

Table 11. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode) ⁽¹⁾	Vector address
-	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	Reserved						0x00 8008
1	FLASH	FLASH end of programing/ write attempted to protected page interrupt	-	-	Yes	Yes	0x00 800C
2	DMA1 0/1	DMA1 channels 0/1 half transaction/transaction complete interrupt	-	-	Yes	Yes	0x00 8010
3	DMA1 2/3	DMA1 channels 2/3 half transaction/transaction complete interrupt	-	-	Yes	Yes	0x00 8014
4	RTC	RTC alarm A/ wakeup	Yes	Yes	Yes	Yes	0x00 8018
5	EXTI E/F/ PVD ⁽²⁾	External interrupt port E/F PVD interrupt	Yes	Yes	Yes	Yes	0x00 801C
6	EXTIB/G	External interrupt port B/G	Yes	Yes	Yes	Yes	0x00 8020
7	EXTID/H	External interrupt port D/H	Yes	Yes	Yes	Yes	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes	0x00 8044
16	LCD	LCD interrupt	-	-	Yes	Yes	0x00 8048
17	CLK/TIM1/ DAC	CLK system clock switch/ CSS interrupt/ TIM 1 break/DAC	-	-	Yes	Yes	0x00 804C
18	COMP1/ COMP2/ ADC1	COMP1 interrupt COMP2 interrupt ACD1 end of conversion/ analog watchdog/ overrun interrupt	Yes	Yes	Yes	Yes	0x00 8050

Table 11. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode) ⁽¹⁾	Vector address
19	TIM2	TIM2 update/overflow/trigger/break interrupt	-	-	Yes	Yes	0x00 8054
20	TIM2	TIM2 capture/compare interrupt	-	-	Yes	Yes	0x00 8058
21	TIM3	TIM3 update/overflow/trigger/break interrupt	-	-	Yes	Yes	0x00 805C
22	TIM3	TIM3 capture/compare interrupt	-	-	Yes	Yes	0x00 8060
23	TIM1	Update /overflow/trigger/COM	-	-	-	Yes	0x00 8064
24	TIM1	Capture/compare	-	-	-	Yes	0x00 8068
25	TIM4	TIM4 update/overflow/trigger interrupt	-	-	Yes	Yes	0x00 806C
26	SPI1	SPI1 TX buffer empty/ RX buffer not empty/ error/wakeup interrupt	Yes	Yes	Yes	Yes	0x00 8070
27	USART1	USART1 transmit data register empty/ transmission complete interrupt	-	-	Yes	Yes	0x00 8074
28	USART1	USART1 received data ready/overrun error/ idle line detected/parity error/global error interrupt	-	-	Yes	Yes	0x00 8078
29	I ² C1	I ² C1 interrupt ⁽³⁾	Yes	Yes	Yes	Yes	0x00 807C

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode. In WFE mode, the interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When the interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
2. The interrupt from PVD is logically OR-ed with Port E and F interrupts. Register EXTI_CONF allows to select between Port E and Port F interrupt (see [External interrupt port select register \(EXTI_CONF\)](#) in the RM0031).
3. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See [Table 12](#) for details on option byte addresses.

The option bytes can also be modified 'on the fly' by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 12. Option byte addresses

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved									0x00	
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG _HALT	WWDG _HW	IWDG _HALT	IWDG _HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x00
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

8 Unique ID

STM8 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4926	X co-ordinate on the wafer	U_ID[7:0]							
0x4927		U_ID[15:8]							
0x4928	Y co-ordinate on the wafer	U_ID[23:16]							
0x4929		U_ID[31:24]							
0x492A	Wafer number	U_ID[39:32]							
0x492B	Lot number	U_ID[47:40]							
0x492C		U_ID[55:48]							
0x492D		U_ID[63:56]							
0x492E		U_ID[71:64]							
0x492F		U_ID[79:72]							
0x4930		U_ID[87:80]							
0x4931		U_ID[95:88]							

In the following table, data is based on characterization results, unless otherwise specified.

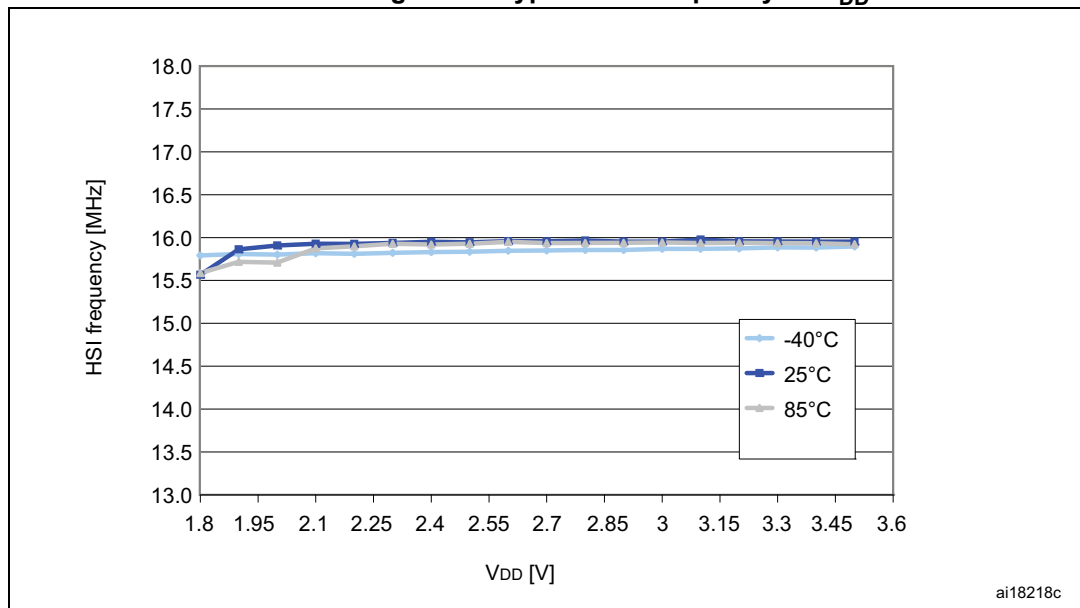
**Table 22. Total current consumption and timing in Low power run mode
at $V_{DD} = 1.65\text{ V}$ to 3.6 V**

Symbol	Parameter	Conditions ⁽¹⁾			Typ	Max	Unit
$I_{DD(LPR)}$	Supply current in Low power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	5.1	5.4	μA
				$T_A = 55\text{ }^{\circ}\text{C}$	5.7	6	
				$T_A = 85\text{ }^{\circ}\text{C}$	6.8	7.5	
				$T_A = 105\text{ }^{\circ}\text{C}$	9.2	10.4	
				$T_A = 125\text{ }^{\circ}\text{C}$	13.4	16.6	
			with TIM2 active ⁽²⁾	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	5.4	5.7	
				$T_A = 55\text{ }^{\circ}\text{C}$	6.0	6.3	
				$T_A = 85\text{ }^{\circ}\text{C}$	7.2	7.8	
				$T_A = 105\text{ }^{\circ}\text{C}$	9.4	10.7	
				$T_A = 125\text{ }^{\circ}\text{C}$	13.8	17	
		LSE ⁽³⁾ external clock (32.768 kHz)	all peripherals OFF	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	5.25	5.6	
				$T_A = 55\text{ }^{\circ}\text{C}$	5.67	6.1	
				$T_A = 85\text{ }^{\circ}\text{C}$	5.85	6.3	
				$T_A = 105\text{ }^{\circ}\text{C}$	7.11	7.6	
				$T_A = 125\text{ }^{\circ}\text{C}$	9.84	12	
			with TIM2 active ⁽²⁾	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	5.59	6	
				$T_A = 55\text{ }^{\circ}\text{C}$	6.10	6.4	
				$T_A = 85\text{ }^{\circ}\text{C}$	6.30	7	
				$T_A = 105\text{ }^{\circ}\text{C}$	7.55	8.4	
				$T_A = 125\text{ }^{\circ}\text{C}$	10.1	15	

1. No floating I/Os

2. Timer 2 clock enabled and counter running

3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\text{ LSE}}$) must be added. Refer to [Table 32](#)

Figure 19. Typical HSI frequency vs V_{DD} 

ai18218c

Low speed internal RC oscillator (LSI)

In the following table, data is based on characterization results, not tested in production.

Table 34. LSI oscillator characteristics

Symbol	Parameter ⁽¹⁾	Conditions ⁽¹⁾	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	200 ⁽²⁾	μ s
$I_{DD(LSI)}$	LSI oscillator frequency drift ⁽³⁾	$0\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$	-12	-	11	%

1. $V_{DD} = 1.65\text{ V to }3.6\text{ V}$, $T_A = -40\text{ to }125\text{ }^{\circ}\text{C}$ unless otherwise specified.

2. Guaranteed by design.

3. This is a deviation for an individual part, once the initial frequency has been measured.

6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in [Figure 24](#)).

Figure 21. Typical V_{IL} and V_{IH} vs V_{DD} (high sink I/Os)

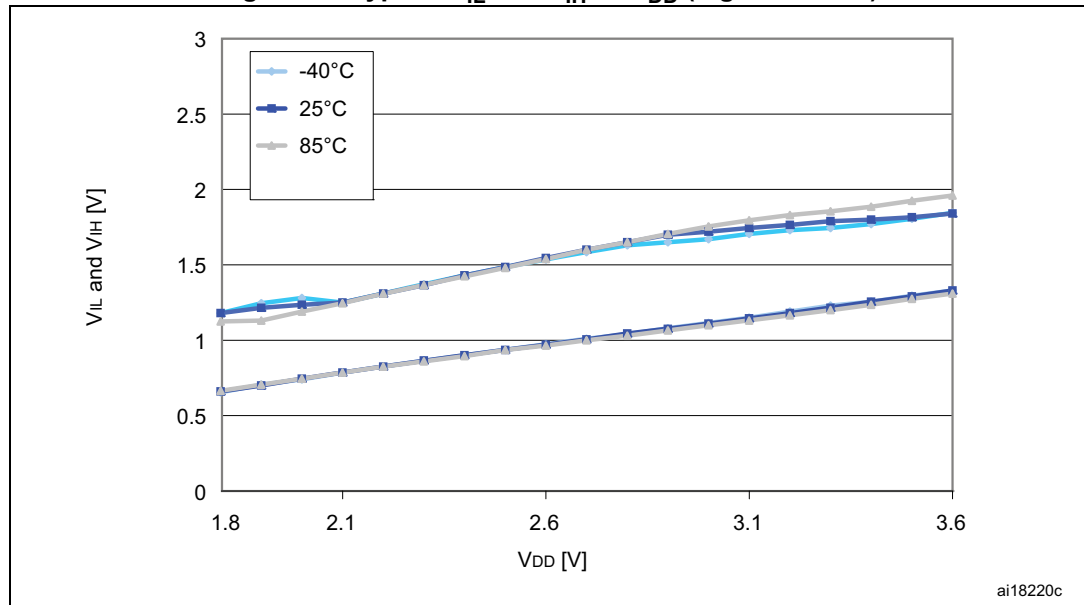
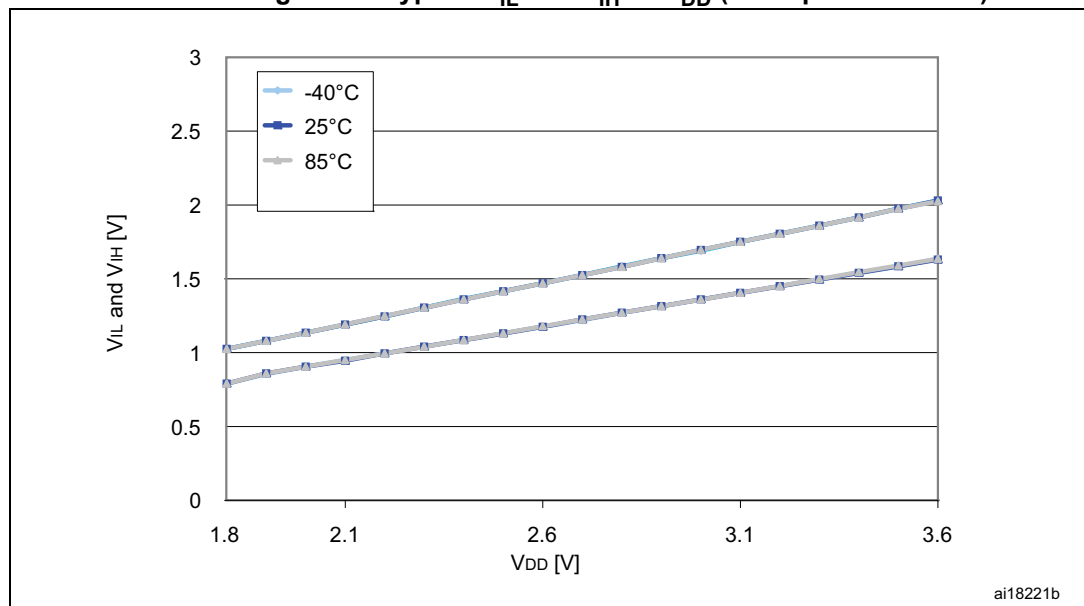


Figure 22. Typical V_{IL} and V_{IH} vs V_{DD} (true open drain I/Os)



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
High sink	$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +2 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$	-	0.45	V
			$I_{IO} = +2 \text{ mA}$, $V_{DD} = 1.8 \text{ V}$	-	0.45	V
			$I_{IO} = +10 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$	-	0.7	V
	$V_{OH}^{(2)}$	Output high level voltage for an I/O pin	$I_{IO} = -2 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$	$V_{DD}-0.45$	-	V
			$I_{IO} = -1 \text{ mA}$, $V_{DD} = 1.8 \text{ V}$	$V_{DD}-0.45$	-	V
			$I_{IO} = -10 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$	$V_{DD}-0.7$	-	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Table 16](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in [Table 16](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .

Table 40. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +3 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$	-	0.45	V
			$I_{IO} = +1 \text{ mA}$, $V_{DD} = 1.8 \text{ V}$	-	0.45	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Table 16](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .

Table 41. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
$\overline{R}$	$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +20 \text{ mA}$, $V_{DD} = 2.0 \text{ V}$	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Table 16](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .

9.3.14 12-bit ADC1 characteristics

In the following table, data is guaranteed by design, not tested in production.

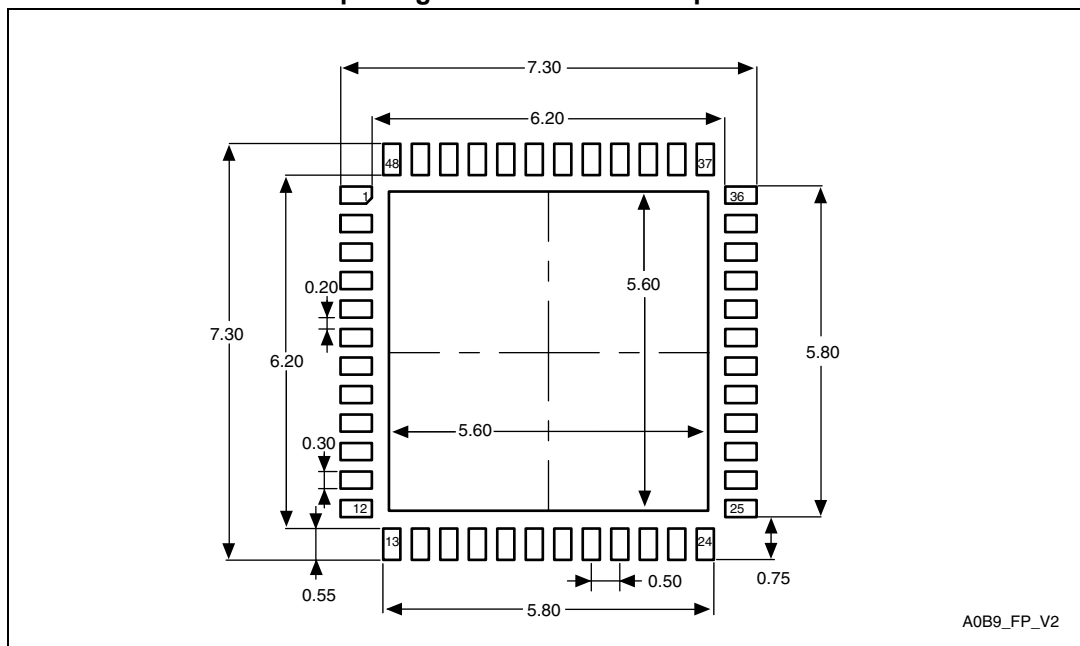
Table 53. ADC1 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	$2.4\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$	2.4	-	V_{DDA}	V
		$1.8\text{ V} \leq V_{DDA} \leq 2.4\text{ V}$	V_{DDA}			V
V_{REF-}	Lower reference voltage	-	V_{SSA}			V
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	μA
I_{VREF+}	Current on the V_{REF+} input pin	-	-	400	700 (peak) ⁽¹⁾	μA
		-	-		450 (average) ⁽¹⁾	μA
V_{AIN}	Conversion voltage range	-	0 ⁽²⁾	-	V_{REF+}	V
T_A	Temperature range	-	-40	-	125	$^{\circ}\text{C}$
R_{AIN}	External resistance on V_{AIN}	on PF0 fast channel	-	-	50 ⁽³⁾	$\text{k}\Omega$
		on all other channels	-	-		
C_{ADC}	Internal sample and hold capacitor	on PF0 fast channel	-	16	-	pF
		on all other channels	-		-	
f_{ADC}	ADC sampling clock frequency	$2.4\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$ without zooming	0.320	-	16	MHz
		$1.8\text{ V} \leq V_{DDA} \leq 2.4\text{ V}$ with zooming	0.320	-	8	MHz
f_{CONV}	12-bit conversion rate	V_{AIN} on PF0 fast channel	-	-	1 ⁽⁴⁾⁽⁵⁾	MHz
		V_{AIN} on all other channels	-	-	760 ⁽⁴⁾⁽⁵⁾	kHz
f_{TRIG}	External trigger frequency	-	-	-	t_{conv}	$1/f_{ADC}$
t_{LAT}	External trigger latency	-	-	-	3.5	$1/f_{SYSCLK}$

Table 63. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

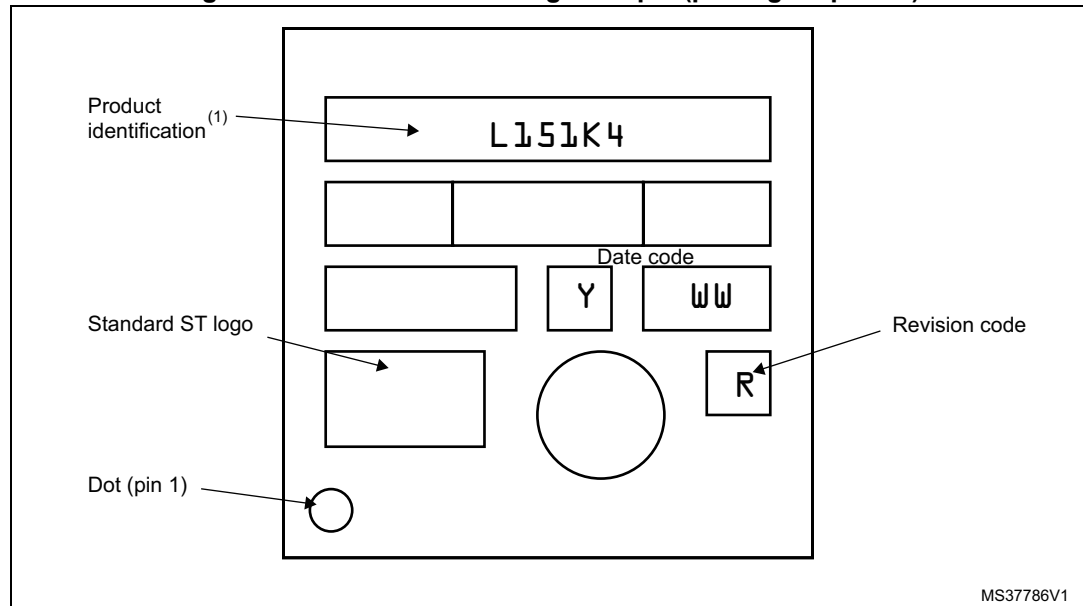
Figure 47. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 54. UFQFPN32 marking example (package top view)

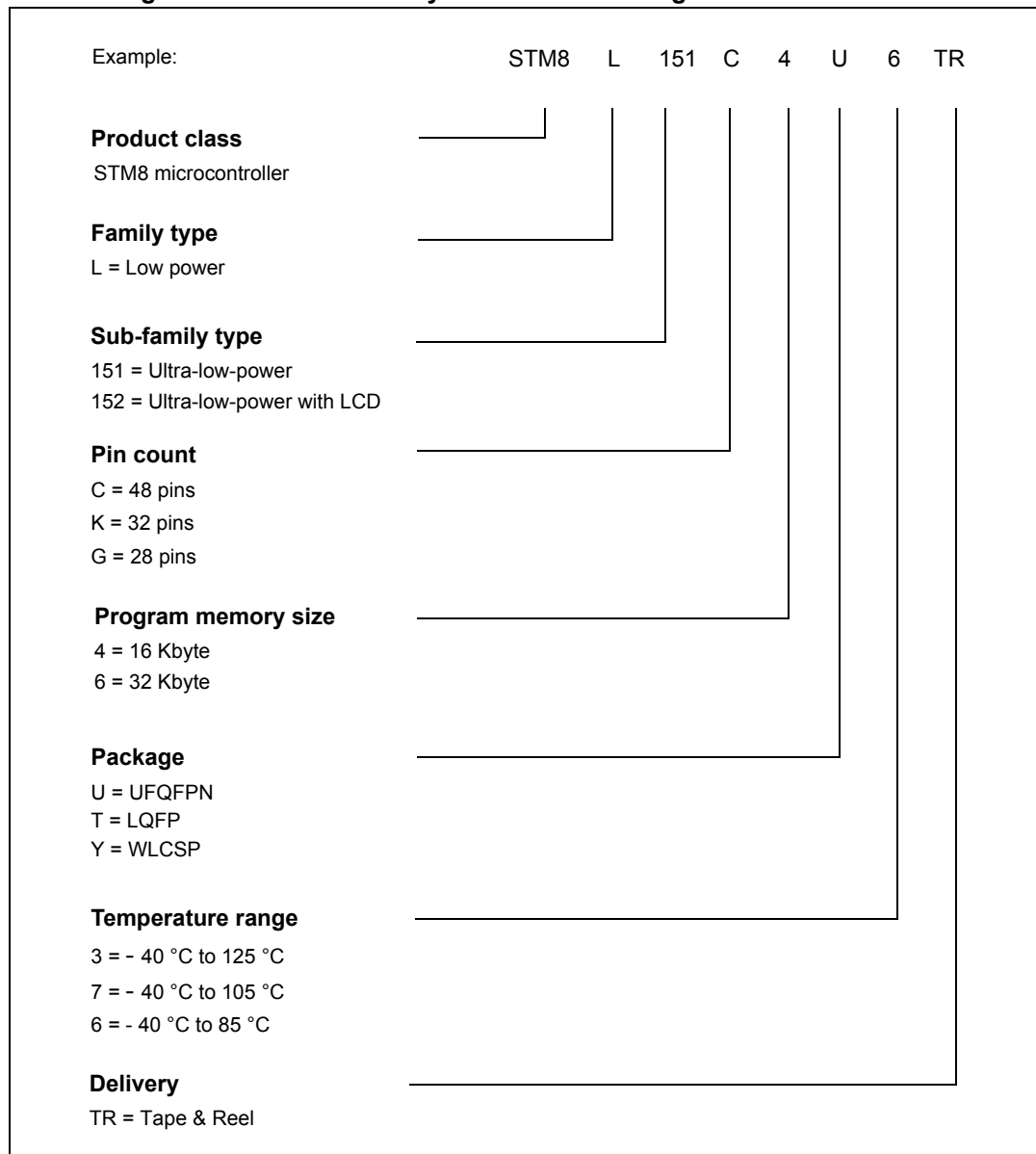


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

11 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Figure 60. Medium-density STM8L15x ordering information scheme



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please contact the ST sales office nearest to you.