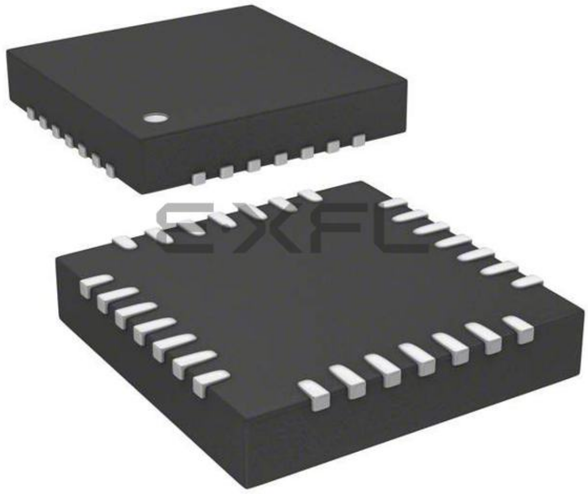


## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | STM8 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 18x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-UFQFN |
| Supplier Device Package | 28-UFQFPN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151g6u3tr |

# 2 Description

The medium-density STM8L151x4/6 and STM8L152x4/6 devices are members of the STM8L ultra-low-power 8-bit family. The medium-density STM8L15x family operates from 1.8 V to 3.6 V (down to 1.65 V at power down) and is available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

The medium-density STM8L15x ultra-low-power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive In-Application debugging and ultra-fast Flash programming.

All medium-density STM8L15x microcontrollers feature embedded data EEPROM and low-power, low-voltage, single-supply program Flash memory.

They incorporate an extensive range of enhanced I/Os and peripherals.

The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

Six different packages are proposed from 28 to 48 pins. Depending on the device chosen, different sets of peripherals are included.

All STM8L ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

## 2.2 Ultra-low-power continuum

The ultra-low-power medium-densitySTM8L151x4/6 and STM8L152x4/6 devices are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101xx and STM8L15xxx. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13 µm ultra-low leakage process.

*Note:* 1 *The STM8L151xx and STM8L152xx are pin-to-pin compatible with STM8L101xx devices.*

2 *The STM32L family is pin-to-pin compatible with the general purpose STM32F family. Please refer to STM32L15x documentation for more information on these devices.*

### Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM® Cortex®-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

### Shared peripherals

STM8L151xx/152xx and STM8L15xxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC1, DAC, and comparators COMP1/COMP2
- Digital peripherals: RTC and some communication interfaces

### Common system strategy

To offer flexibility and optimize performance, the STM8L151xx/152xx and STM8L15xxx devices use a common architecture:

- Same power supply range from 1.8 to 3.6 V, down to 1.65 V at power down
- Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy for both STM8L15x and STM32L15xxx including power-on reset, power-down reset, brownout reset and programmable voltage detector.

### Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbyte

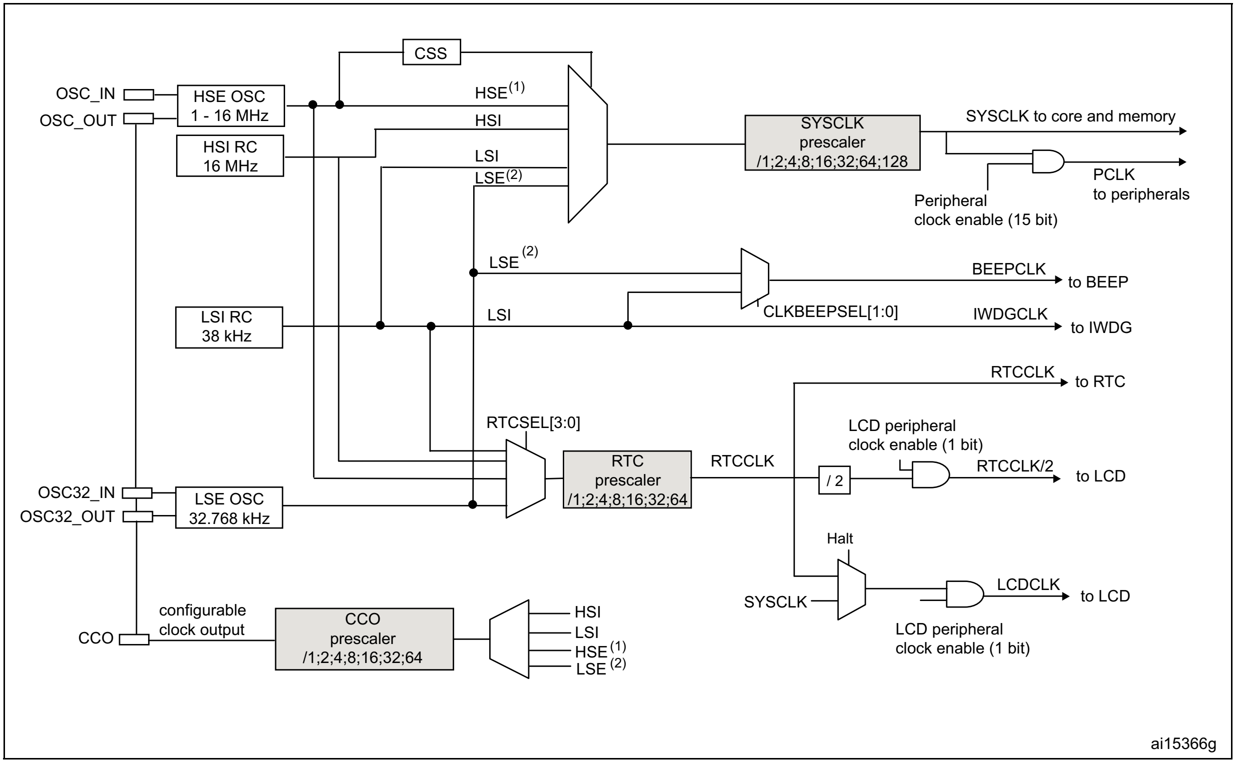
IWDG: Independent watchdog
LCD: Liquid crystal display
POR/PDR: Power on reset / power down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

## 3.1 Low-power modes

The medium-density STM8L151x4/6 and STM8L152x4/6 devices support five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: The CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt, event or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode). Wait consumption: refer to *Table 21*.
- **Low power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power run mode consumption: refer to *Table 22*.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power wait mode consumption: refer to *Table 23*.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset. Active-halt consumption: refer to *Table 24* and *Table 25*.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs. Halt consumption: refer to *Table 26*.

Figure 2. Medium-density STM8L151x4/6 and STM8L152x4/6 clock tree diagram



1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to *Section HSE clock* in the STM8L15x and STM8L16x reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to *Section LSE clock* in the STM8L15x and STM8L16x reference manual (RM0031).

## 3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from every second to every year

### Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48/UFQFPN48 | LQFP32/UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| - | 5 | 5 | D4 | PA5/TIM3_BKIN/ *[TIM3_ETR]*(4)/ LCD_COM1(2)/ADC1_IN1/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port A5** | Timer 3 - break input / *[Timer 3 - external trigger]* / LCD_COM 1 / ADC1 input 1 / Comparator 1 positive input |
| 7 | 6 | - | - | PA6/*[ADC1_TRIG]*(4)/ LCD_COM2(2)/ADC1_IN0/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port A6** | *[ADC1 - trigger]* / LCD_COM2 / ADC1 input 0 / Comparator 1 positive input |
| 8 | - | - | - | PA7/LCD_SEG0(2)(5) | I/O | FT | **X** | X | X | HS | X | X | **Port A7** | LCD segment 0 |
| 24 | 13 | 12 | E3 | PB0(6)/TIM2_CH1/ LCD_SEG10(2)/ ADC1_IN18/COMP1_INP | I/O | TT (3) | **X**(6) | X(6) | X | HS | X | X | **Port B0** | Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18 / Comparator 1 positive input |
| 25 | 14 | 13 | G1 | PB1/TIM3_CH1/ LCD_SEG11(2)/ ADC1_IN17/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port B1** | Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17 / Comparator 1 positive input |
| 26 | 15 | 14 | F2 | PB2/ TIM2_CH2/ LCD_SEG12(2)/ ADC1_IN16/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port B2** | Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16/ Comparator 1 positive input |
| 27 | - | - | - | PB3/TIM2_ETR/ LCD_SEG13(2)/ ADC1_IN15/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port B3** | Timer 2 - external trigger / LCD segment 13 /ADC1_IN15 / Comparator 1 positive input |

### Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48/UFQFPN48 | LQFP32/UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| - | 8 | 7 | G4 | $V_{DD1}$/$V_{DDA}$/$V_{REF+}$ | S | - | **-** | - | - | - | - | - | Digital power supply / Analog supply voltage / ADC1 positive voltage reference | |
| 9 | 7 | 6 | F4 | $V_{SS1}$/$V_{SSA}$/$V_{REF-}$ | S | - | **-** | - | - | - | - | - | I/O ground / Analog ground voltage /<br>ADC1 negative voltage reference | |
| 39 | - | - | - | $V_{DD2}$ | S | - | **-** | - | - | - | - | - | IOs supply voltage | |
| 40 | - | - | - | $V_{SS2}$ | S | - | **-** | - | - | - | - | - | IOs ground voltage | |
| 1 | 32 | 28 | A4 | PA0(9)/*[USART1_CK]*(4)/ SWIM/BEEP/IR_TIM (10) | I/O | | X | **X**(9) | X | HS<br>(10) | X | X | **Port A0** | *[USART1 synchronous clock]*(4) / SWIM input and output /<br>Beep output / Infrared Timer output |

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15x and STM8L16x reference manual (RM0031).
2. Available on STM8L152xx devices only.
3. In the 3.6 V tolerant I/Os, protection diode to $V_{DD}$ is not implemented.
4. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
5. In the 5 V tolerant I/Os, protection diode to $V_{DD}$ is not implemented.
6. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
7. In the open-drain output column, ‘T’ defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to $V_{DD}$ are not implemented).
8. Available on STM8L151xx devices only.
9. The PA0 pin is in input pull-up during the reset phase and after reset release.
10. High Sink LED driver capability available on PA0.

*Note: The slope control of all GPIO pins, except true open drain pins, can be programmed. By default, the slope control is limited to 2 MHz.*

Table 9. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5200 | SPI1 | SPI1_CR1 | SPI1 control register 1 | 0x00 |
| 0x00 5201 | | SPI1_CR2 | SPI1 control register 2 | 0x00 |
| 0x00 5202 | | SPI1_ICR | SPI1 interrupt control register | 0x00 |
| 0x00 5203 | | SPI1_SR | SPI1 status register | 0x02 |
| 0x00 5204 | | SPI1_DR | SPI1 data register | 0x00 |
| 0x00 5205 | | SPI1_CRCPR | SPI1 CRC polynomial register | 0x07 |
| 0x00 5206 | | SPI1_RXCRCR | SPI1 Rx CRC register | 0x00 |
| 0x00 5207 | | SPI1_TXCRCR | SPI1 Tx CRC register | 0x00 |
| 0x00 5208<br>to<br>0x00 520F | Reserved area (8 bytes) | | | |
| 0x00 5210 | I2C1 | I2C1_CR1 | I2C1 control register 1 | 0x00 |
| 0x00 5211 | | I2C1_CR2 | I2C1 control register 2 | 0x00 |
| 0x00 5212 | | I2C1_FREQR | I2C1 frequency register | 0x00 |
| 0x00 5213 | | I2C1_OARL | I2C1 own address register low | 0x00 |
| 0x00 5214 | | I2C1_OARH | I2C1 own address register high | 0x00 |
| 0x00 5215 | | Reserved (1 byte) | | |
| 0x00 5216 | | I2C1_DR | I2C1 data register | 0x00 |
| 0x00 5217 | | I2C1_SR1 | I2C1 status register 1 | 0x00 |
| 0x00 5218 | | I2C1_SR2 | I2C1 status register 2 | 0x00 |
| 0x00 5219 | | I2C1_SR3 | I2C1 status register 3 | 0x0x |
| 0x00 521A | | I2C1_ITR | I2C1 interrupt control register | 0x00 |
| 0x00 521B | | I2C1_CCRL | I2C1 clock control register low | 0x00 |
| 0x00 521C | | I2C1_CCRH | I2C1 clock control register high | 0x00 |
| 0x00 521D | | I2C1_TRISER | I2C1 TRISE register | 0x02 |
| 0x00 521E | | I2C1_PECR | I2C1 packet error checking register | 0x00 |
| 0x00 521F<br>to<br>0x00 522F | Reserved area (17 bytes) | | | |

Table 11. Interrupt mapping (continued)

| IRQ No. | Source block | Description | Wakeup from Halt mode | Wakeup from Active-halt mode | Wakeup from Wait (WFI mode) | Wakeup from Wait (WFE mode)[1] | Vector address |
|---|---|---|---|---|---|---|---|
| 19 | TIM2 | TIM2 update/overflow/ trigger/break interrupt | - | - | Yes | Yes | 0x00 8054 |
| 20 | TIM2 | TIM2 capture/ compare interrupt | - | - | Yes | Yes | 0x00 8058 |
| 21 | TIM3 | TIM3 update/overflow/ trigger/break interrupt | - | - | Yes | Yes | 0x00 805C |
| 22 | TIM3 | TIM3 capture/ compare interrupt | - | - | Yes | Yes | 0x00 8060 |
| 23 | TIM1 | Update /overflow/trigger/ COM | - | - | - | Yes | 0x00 8064 |
| 24 | TIM1 | Capture/compare | - | - | - | Yes | 0x00 8068 |
| 25 | TIM4 | TIM4 update/overflow/ trigger interrupt | - | - | Yes | Yes | 0x00 806C |
| 26 | SPI1 | SPI1 TX buffer empty/ RX buffer not empty/ error/wakeup interrupt | Yes | Yes | Yes | Yes | 0x00 8070 |
| 27 | USART1 | USART1 transmit data register empty/ transmission complete interrupt | - | - | Yes | Yes | 0x00 8074 |
| 28 | USART1 | USART1 received data ready/overrun error/ idle line detected/parity error/global error interrupt | - | - | Yes | Yes | 0x00 8078 |
| 29 | I$^2$C1 | I$^2$C1 interrupt[3] | Yes | Yes | Yes | Yes | 0x00 807C |

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode. In WFE mode, the interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When the interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
2. The interrupt from PVD is logically OR-ed with Port E and F interrupts. Register EXTI_CONF allows to select between Port E and Port F interrupt (see *External interrupt port select register (EXTI_CONF)* in the RM0031).
3. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

# 7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option bytes can also be modified ‘on the fly’ by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

**Table 12. Option byte addresses**

| **Addr.** | **Option name** | **Option byte No.** | **Option bits** | | | | | | | | **Factory default setting** |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0x00 4800 | Read-out protection (ROP) | OPT0 | ROP[7:0] | | | | | | | | 0xAA |
| 0x00 4802 | UBC (User Boot code size) | OPT1 | UBC[7:0] | | | | | | | | 0x00 |
| 0x00 4807 | Reserved | | | | | | | | | | 0x00 |
| 0x00 4808 | Independent watchdog option | OPT3 [3:0] | Reserved | | | | WWDG _HALT | WWDG _HW | IWDG _HALT | IWDG _HW | 0x00 |
| 0x00 4809 | Number of stabilization clock cycles for HSE and LSE oscillators | OPT4 | Reserved | | | | LSECNT[1:0] | | HSECNT[1:0] | | 0x00 |
| 0x00 480A | Brownout reset (BOR) | OPT5 [3:0] | Reserved | | | | BOR_TH | | | BOR_ ON | 0x00 |
| 0x00 480B | Bootloader option bytes (OPTBL) | OPTBL [15:0] | OPTBL[15:0] | | | | | | | | 0x00 |
| 0x00 480C | | | | | | | | | | | 0x00 |

## 9.3 Operating conditions

Subject to general operating conditions for $V_{DD}$ and $T_A$.

### 9.3.1 General operating conditions

Table 18. General operating conditions

| Symbol | Parameter | Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{SYSCLK}$(1) | System clock frequency | 1.65 V ≤ $V_{DD}$ < 3.6 V | | 0 | 16 | MHz |
| $V_{DD}$ | Standard operating voltage | - | | 1.65(2) | 3.6 | V |
| $V_{DDA}$ | Analog operating voltage | ADC and DAC not used | Must be at the same potential as $V_{DD}$ | 1.65(2) | 3.6 | V |
| | | ADC or DAC used | | 1.8 | 3.6 | V |
| $P_D$(3) | Power dissipation at $T_A$= 85 °C for suffix 6 devices | LQFP48 | | - | 288 | mW |
| | | UFQFPN48 | | - | 169 | |
| | | LQFP32 | | - | 288 | |
| | | UFQFPN32 | | - | 169 | |
| | | UFQFPN28 | | - | 169 | |
| | | WLCSP28 | | - | 286 | |
| | Power dissipation at $T_A$= 125 °C for suffix 3 devices and at $T_A$= 105 °C for suffix 7 devices | LQFP48 | | - | 77 | |
| | | UFQFPN48 | | - | 156 | |
| | | LQFP32 | | - | 85 | |
| | | UFQFPN32 | | - | 131 | |
| | | UFQFPN28 | | - | 42 | |
| | | WLCSP28 | | - | 71 | |
| $T_A$ | Temperature range | 1.65 V ≤ $V_{DD}$ < 3.6 V (6 suffix version) | | -40 | 85 | °C |
| | | 1.65 V ≤ $V_{DD}$ < 3.6 V (7 suffix version) | | -40 | 105 | |
| | | 1.65 V ≤ $V_{DD}$ < 3.6 V (3 suffix version) | | -40 | 125 | |
| $T_J$ | Junction temperature range | -40 °C ≤ $T_A$ < 85 °C (6 suffix version) | | -40 | 105(4) | °C |
| | | -40 °C ≤ $T_A$ < 105 °C (7 suffix version) | | -40 | 110(4) | |
| | | -40 °C ≤ $T_A$ < 125 °C (3 suffix version) | | -40 | 130 | |

1. $f_{SYSCLK} = f_{CPU}$
2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with $T_{Jmax}$ in this table and $\Theta_{JA}$ in “Thermal characteristics” table.
4. $T_{Jmax}$ is given by the test limit. Above this value the product behavior is not guaranteed.

In the following table, data is based on characterization results, unless otherwise specified.

**Table 24. Total current consumption and timing in Active-halt mode at $V_{DD}$ = 1.65 V to 3.6 V**

| Symbol | Parameter | Conditions (1) | | | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(AH)}$ | Supply current in Active-halt mode | LSI RC (at 38 kHz) | LCD OFF(2) | $T_A$ = -40 °C to 25 °C | 0.9 | 2.1 | µA |
| | | | | $T_A$ = 55 °C | 1.2 | 3 | |
| | | | | $T_A$ = 85 °C | 1.5 | 3.4 | |
| | | | | $T_A$ = 105 °C | 2.6 | 6.6 | |
| | | | | $T_A$ = 125 °C | 5.1 | 12 | |
| | | | LCD ON (static duty/ external $V_{LCD}$) (3) | $T_A$ = -40 °C to 25 °C | 1.4 | 3.1 | |
| | | | | $T_A$ = 55 °C | 1.5 | 3.3 | |
| | | | | $T_A$ = 85 °C | 1.9 | 4.3 | |
| | | | | $T_A$ = 105 °C | 2.9 | 6.8 | |
| | | | | $T_A$ = 125 °C | 5.5 | 13 | |
| | | | LCD ON (1/4 duty/ external $V_{LCD}$) (4) | $T_A$ = -40 °C to 25 °C | 1.9 | 4.3 | |
| | | | | $T_A$ = 55 °C | 1.95 | 4.4 | |
| | | | | $T_A$ = 85 °C | 2.4 | 5.4 | |
| | | | | $T_A$ = 105 °C | 3.4 | 7.6 | |
| | | | | $T_A$ = 125 °C | 6.0 | 15 | |
| | | | LCD ON (1/4 duty/ internal $V_{LCD}$) (5) | $T_A$ = -40 °C to 25 °C | 3.9 | 8.75 | |
| | | | | $T_A$ = 55 °C | 4.15 | 9.3 | |
| | | | | $T_A$ = 85 °C | 4.5 | 10.2 | |
| | | | | $T_A$ = 105 °C | 5.6 | 13.5 | |
| | | | | $T_A$ = 125 °C | 6.8 | 16.3 | |

### Table 24. Total current consumption and timing in Active-halt mode at $V_{DD}$ = 1.65 V to 3.6 V

| Symbol | Parameter | Conditions [1] | | | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(AH)}$ | Supply current in Active-halt mode | LSE external clock (32.768 kHz) [6] | LCD OFF[7] | $T_A$ = -40 °C to 25 °C | 0.5 | 1.2 | µA |
| | | | | $T_A$ = 55 °C | 0.62 | 1.4 | |
| | | | | $T_A$ = 85 °C | 0.88 | 2.1 | |
| | | | | $T_A$ = 105 °C | 2.1 | 4.85 | |
| | | | | $T_A$ = 125 °C | 4.8 | 11 | |
| | | | LCD ON (static duty/ external $V_{LCD}$) [3] | $T_A$ = -40 °C to 25 °C | 0.85 | 1.9 | |
| | | | | $T_A$ = 55 °C | 0.95 | 2.2 | |
| | | | | $T_A$ = 85 °C | 1.3 | 3.2 | |
| | | | | $T_A$ = 105 °C | 2.3 | 5.3 | |
| | | | | $T_A$ = 125 °C | 5.0 | 12 | |
| | | | LCD ON (1/4 duty/ external $V_{LCD}$) [4] | $T_A$ = -40 °C to 25 °C | 1.5 | 2.5 | |
| | | | | $T_A$ = 55 °C | 1.6 | 3.8 | |
| | | | | $T_A$ = 85 °C | 1.8 | 4.2 | |
| | | | | $T_A$ = 105 °C | 2.9 | 7.0 | |
| | | | | $T_A$ = 125 °C | 5.7 | 14 | |
| | | | LCD ON (1/4 duty/ internal $V_{LCD}$) [5] | $T_A$ = -40 °C to 25 °C | 3.4 | 7.6 | |
| | | | | $T_A$ = 55 °C | 3.7 | 8.3 | |
| | | | | $T_A$ = 85 °C | 3.9 | 9.2 | |
| | | | | $T_A$ = 105 °C | 5.0 | 14.5 | |
| | | | | $T_A$ = 125 °C | 6.3 | 15.2 | |
| $I_{DD(WUFAH)}$ | Supply current during wakeup time from Active-halt mode (using HSI) | - | | - | 2.4 | - | mA |
| $t_{WU\_HSI(AH)}$[8][9] | Wakeup time from Active-halt mode to Run mode (using HSI) | - | | - | 4.7 | 7 | µs |
| $t_{WU\_LSI(AH)}$[8][9] | Wakeup time from Active-halt mode to Run mode (using LSI) | - | | - | 150 | - | µs |

1. No floating I/O, unless otherwise specified.
2. RTC enabled. Clock source = LSI
3. RTC enabled, LCD enabled with external $V_{LCD}$ = 3 V, static duty, division ratio = 256, all pixels active, no LCD connected.
4. RTC enabled, LCD enabled with external $V_{LCD}$, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. LCD enabled with internal LCD booster $V_{LCD}$ = 3 V, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
6. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*.
7. RTC enabled. Clock source = LSE.
8. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after $t_{WU}$.
9. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

### Output driving current

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 39. Output driving current (high sink ports)**

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| High sink | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +2 mA, $V_{DD}$ = 3.0 V | - | 0.45 | V |
| | | | $I_{IO}$ = +2 mA, $V_{DD}$ = 1.8 V | - | 0.45 | V |
| | | | $I_{IO}$ = +10 mA, $V_{DD}$ = 3.0 V | - | 0.7 | V |
| | $V_{OH}$ (2) | Output high level voltage for an I/O pin | $I_{IO}$ = -2 mA, $V_{DD}$ = 3.0 V | $V_{DD}$-0.45 | - | V |
| | | | $I_{IO}$ = -1 mA, $V_{DD}$ = 1.8 V | $V_{DD}$-0.45 | - | V |
| | | | $I_{IO}$ = -10 mA, $V_{DD}$ = 3.0 V | $V_{DD}$-0.7 | - | V |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. The $I_{IO}$ current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.

**Table 40. Output driving current (true open drain ports)**

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Open drain | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +3 mA, $V_{DD}$ = 3.0 V | - | 0.45 | V |
| | | | $I_{IO}$ = +1 mA, $V_{DD}$ = 1.8 V | - | 0.45 | |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

**Table 41. Output driving current (PA0 with high sink LED driver capability)**

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| IR | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +20 mA, $V_{DD}$ = 2.0 V | - | 0.45 | V |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

## 9.3.8 Communication interfaces

### SPI1 - Serial peripheral interface

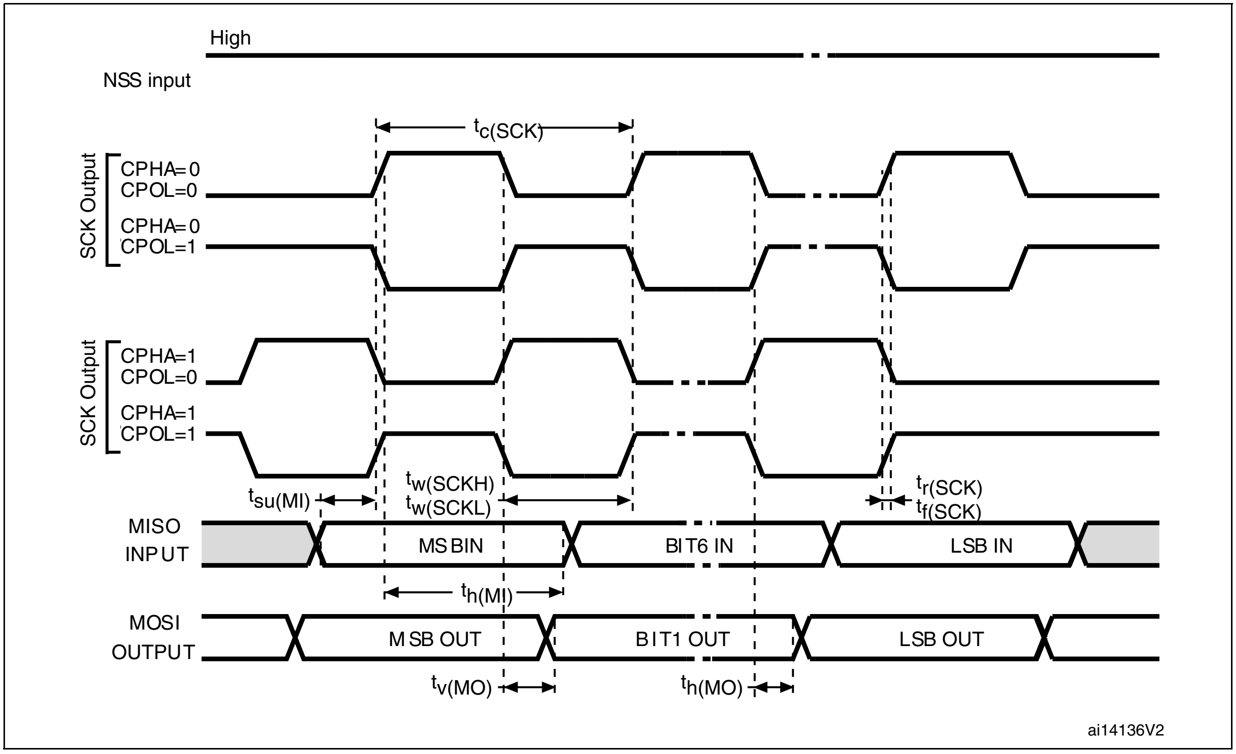
Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, $f_{SYSCLK}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 43. SPI1 characteristics**

| Symbol | Parameter | Conditions(1) | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI1 clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 8 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI1 clock rise and fall time | Capacitive load: C = 30 pF | - | 30 | ns |
| $t_{su(NSS)}$(2) | NSS setup time | Slave mode | 4 x 1/$f_{SYSCLK}$ | - | |
| $t_{h(NSS)}$(2) | NSS hold time | Slave mode | 80 | - | |
| $t_{w(SCKH)}$(2)<br>$t_{w(SCKL)}$(2) | SCK high and low time | Master mode, $f_{MASTER}$ = 8 MHz, $f_{SCK}$= 4 MHz | 105 | 145 | |
| $t_{su(MI)}$(2)<br>$t_{su(SI)}$(2) | Data input setup time | Master mode | 30 | - | |
| | | Slave mode | 3 | - | |
| $t_{h(MI)}$(2)<br>$t_{h(SI)}$(2) | Data input hold time | Master mode | 15 | - | |
| | | Slave mode | 0 | - | |
| $t_{a(SO)}$(2)(3) | Data output access time | Slave mode | - | 3x 1/$f_{SYSCLK}$ | |
| $t_{dis(SO)}$(2)(4) | Data output disable time | Slave mode | 30 | - | |
| $t_{v(SO)}$ (2) | Data output valid time | Slave mode (after enable edge) | - | 60 | |
| $t_{v(MO)}$(2) | Data output valid time | Master mode (after enable edge) | - | 20 | |
| $t_{h(SO)}$(2) | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| $t_{h(MO)}$(2) | | Master mode (after enable edge) | 1 | - | |

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

Figure 36. SPI1 timing diagram - master mode[1]



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

### 9.3.10 Embedded reference voltage

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

**Table 46. Reference voltage characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{REFINT}$ | Internal reference voltage consumption | - | - | 1.4 | - | µA |
| $T_{S\_VREFINT}$(1)(2) | ADC sampling time when reading the internal reference voltage | - | - | 5 | 10 | µs |
| $I_{BUF}$(2) | Internal reference voltage buffer consumption (used for ADC) | - | - | 13.5 | 25 | µA |
| $V_{REFINT\ out}$ | Reference voltage output | - | 1.202(3) | 1.224 | 1.242(3) | V |
| $I_{LPBUF}$(2) | Internal reference voltage low power buffer consumption (used for comparators or output) | - | - | 730 | 1200 | nA |
| $I_{REFOUT}$(2) | Buffer output current(4) | - | - | - | 1 | µA |
| $C_{REFOUT}$ | Reference voltage output load | - | - | - | 50 | pF |
| $t_{VREFINT}$ | Internal reference voltage startup time | - | - | 2 | 3 | ms |
| $t_{BUFEN}$(2) | Internal reference voltage buffer startup time once enabled (1) | - | - | - | 10 | µs |
| $ACC_{VREFINT}$ | Accuracy of $V_{REFINT}$ stored in the VREFINT_Factory_CONV byte(5) | - | - | - | ± 5 | mV |
| $STAB_{VREFINT}$ | Stability of $V_{REFINT}$ over temperature | $-40\ °C \leq T_A \leq 125\ °C$ | - | 20 | 50 | ppm/°C |
| | Stability of $V_{REFINT}$ over temperature | $0\ °C \leq T_A \leq 50\ °C$ | - | - | 20 | ppm/°C |
| $STAB_{VREFINT}$ | Stability of $V_{REFINT}$ after 1000 hours | - | - | - | TBD | ppm |

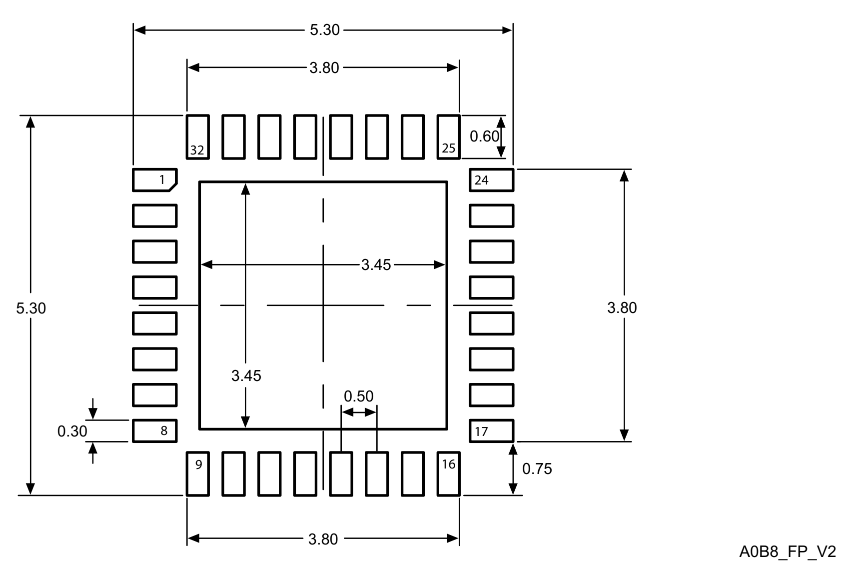
1. Defined when ADC output reaches its final value ±1/2LSB
2. Data guaranteed by design.
3. Tested in production at $V_{DD}$ = 3 V ±10 mV.
4. To guaranty less than 1% $V_{REFOUT}$ deviation.
5. Measured at $V_{DD}$ = 3 V ±10 mV. This value takes into account $V_{DD}$ accuracy and ADC conversion accuracy.

### Table 65. UFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| A3 | - | 0.152 | - | - | 0.0060 | - |
| b | 0.180 | 0.230 | 0.280 | 0.0071 | 0.0091 | 0.0110 |
| D | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| D1 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| D2 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| E | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| E1 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| E2 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

### Figure 53. UFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

**Table 69. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 23-Jul-2010 | 5 | Modified *Introduction* and *Description.*<br>Modified *Table: Legend/abbreviation for table 5* and *Table: Medium density STM8L15x pin description* (for PA0, PA1, PB0 and PB4 and for reset states in the floating input column)<br>Modified *Figure: Low density STM8L151xx device block diagram, Figure: Low density STM8L15x clock tree diagram*, *Figure: Low power modes* and *Figure : Low power real-time clock.*<br>Modified CLK_PCKENR2 and CLK_HSICALR reset values in *Table: General hardware register map.*<br>Modified notes below *Figure: Memory map.*<br>Modified PA_CR1 reset value.<br>Modified reset values for Px_IDR registers.<br>Modified *Table: Voltage characteristics* and *Table: Current characteristics.*<br>Modified $V_{IH}$ in *Table: I/O static characteristics.*<br>Modified *Table: Total current consumption in Wait mode.*<br>Modified *Figure Typical application with I2C bus and timing diagram 1).*<br>Modified $I_L$ value in *Figure: Typical connection diagram using the ADC1.*<br>Modified $R_H$ and $R_L$ in *Table: LCD characteristics.*<br>Added graphs in *Section: Electrical parameters.*<br>Modified note 3 below *Table: Reference voltage characteristics.*<br>Modified note 1 below *Table: TS characteristics.*<br>Changed $V_{ESD(CDM)}$ value in *Table: ESD absolute maximum ratings.*<br>Updated notes for UFQFPN32 and UFQFPN48 packages. |
| 11-Mar-2011 | 6 | Modified note on true open drain I/Os and I/O level columns in *Table: Medium density STM8L15x pin description.*<br>Remapping option removed for USART1_TX, USART1_RX, and USART1_CK on PC2, PC3 and PC4 in *Table: Medium density STM8L15x pin description.*<br>Modified IDWDG_KR reset value in *Table: General hardware register map.*<br>Replaced VREF_OUT with VREFINT and TIMx_TRIG with TIMx_ETR.<br>Added *Table: Factory conversion registers.* Modified reset values for TIM1_DCR1, IWDG_KR, RTC_DR1, RTC_DR2, RTC_SPRERH, RTC_SPRERL, RTC_APRER, RTC_WUTRH, and RTC_WUTRL in *Table: General hardware register map.*<br>Added notes to certain values in *Section: Embedded reference voltage* and *Section: Temperature sensor.* |