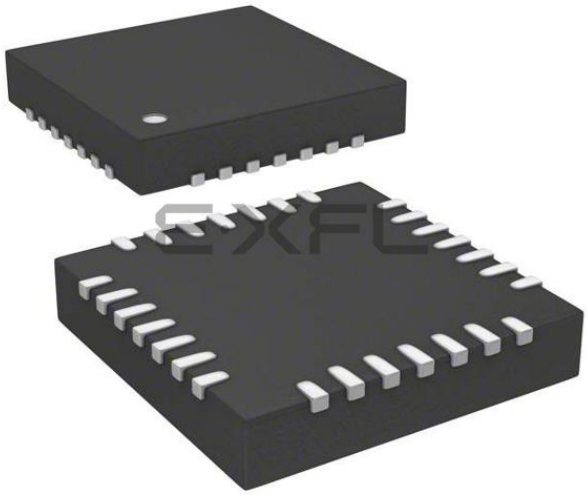

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | STM8 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 18x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-UFQFN |
| Supplier Device Package | 28-UFQFPN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151g6u6 |

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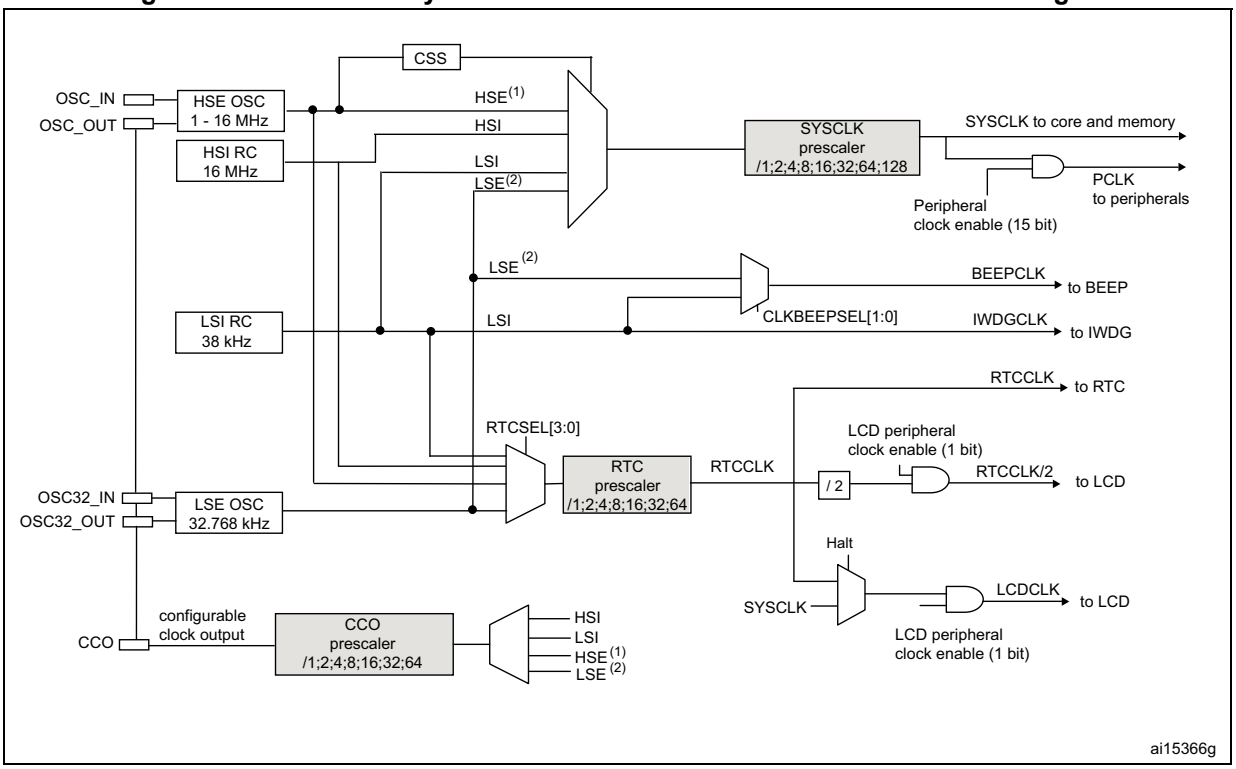
## 2.1 Device overview

**Table 2. Medium-density STM8L151x4/6 and STM8L152x4/6 low-power device features and peripheral counts**

| Features | | STM8L151Gx | | STM8L15xKx | | STM8L15xCx | |
|---|---|---|---|---|---|---|---|
| Flash (Kbyte) | | 16 | 32 | 16 | 32 | 16 | 32 |
| Data EEPROM (Kbyte) | | 1 | | | | | |
| RAM (Kbyte) | | 2 | | | | | |
| LCD | | No | | 4x17 (1) | | 4x28 (1) | |
| Timers | Basic | 1 (8-bit) | | | | | |
| | General purpose | 2 (16-bit) | | | | | |
| | Advanced control | 1 (16-bit) | | | | | |
| Communication interfaces | SPI | 1 | | | | | |
| | I2C | 1 | | | | | |
| | USART | 1 | | | | | |
| GPIOs | | 26(3) | | 30 (2)(3) or 29 (1)(3) | | 41(3) | |
| 12-bit synchronized ADC (number of channels) | | 1 (18) | | 1 (22 (2) or 21 (1)) | | 1 (25) | |
| 12-Bit DAC (number of channels) | | 1 (1) | | | | | |
| Comparators COMP1/COMP2 | | 2 | | | | | |
| Others | | RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator | | | | | |
| CPU frequency | | 16 MHz | | | | | |
| Operating voltage | | 1.8 V to 3.6 V (down to 1.65 V at power down) | | | | | |
| Operating temperature | | -40 to +85 °C/ -40 to +105 °C / -40 to +125 °C | | | | | |
| Packages | | UFQFPN28 (4x4; 0.6 mm thickness) WLCSP28 | | LQFP32(7x7) UFQFPN32 (5x5; 0.6 mm thickness) | | LQFP48 UFQFPN48 (4x4; 0.6 mm thickness) | |

1. STM8L152xx versions only
2. STM8L151xx versions only
3. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

**Figure 2. Medium-density STM8L151x4/6 and STM8L152x4/6 clock tree diagram**




1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to *Section HSE clock* in the STM8L15x and STM8L16x reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to *Section LSE clock* in the STM8L15x and STM8L16x reference manual (RM0031).

## 3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from every second to every year

## 3.6 LCD (Liquid crystal display)

The liquid crystal display drives up to 4 common terminals and up to 28 segment terminals to drive up to 112 pixels.

- Internal step-up converter to guarantee contrast control whatever $V_{DD}$.
- Static 1/2, 1/3, 1/4 duty supported.
- Static 1/2, 1/3 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 4 pixels which can programmed to blink.
- The LCD controller can operate in Halt mode.

*Note: Unnecessary segments and common pins can be used as general I/O pins.*

## 3.7 Memories

The medium-density STM8L151x4/6 and STM8L152x4/6 devices have the following main features:

- Up to 2 Kbyte of RAM
- The non-volatile memory is divided into three arrays:
  - Up to 32 Kbyte of medium-density embedded Flash program memory
  - 1 Kbyte of data EEPROM
  - Option bytes.

The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

## 3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC, I2C1, SPI1, USART1, the four Timers.

## 3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 25 channels (including 1 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 µs with $f_{SYSCLK}$= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

**Figure 6. STM8L151G4, STM8L151G6 WLCSP28 package pinout**

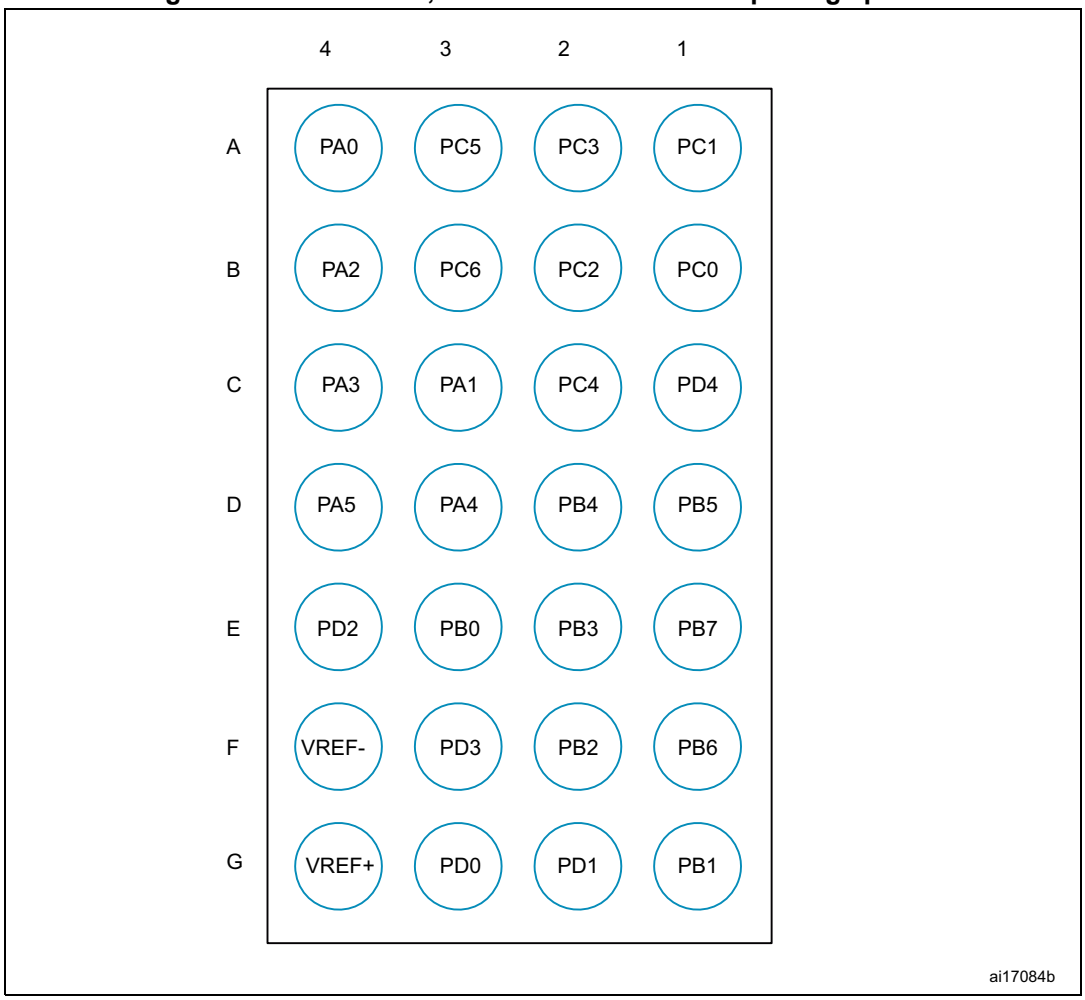



**Figure 7. STM8L152C4, STM8L152C6 48-pin pinout (with LCD)**

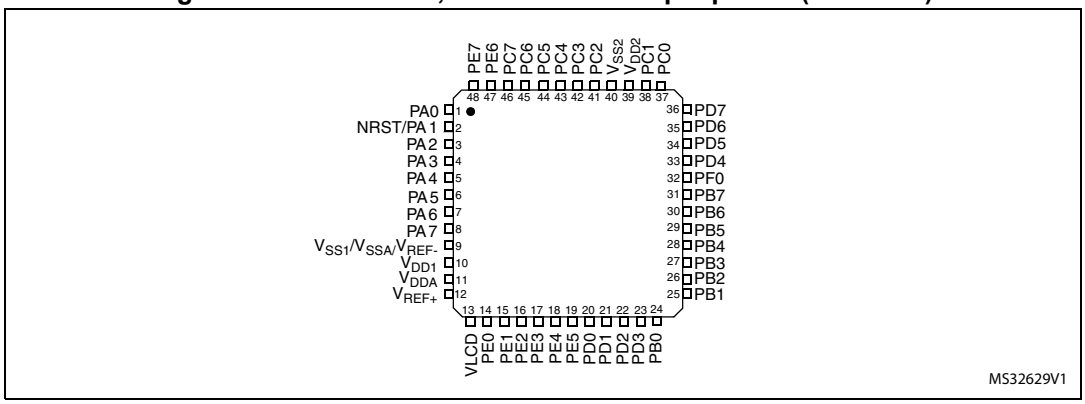


**Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48/UFQFPN48 | LQFP32/UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| - | 16 | - | - | PB3/*[TIM2_ETR]*(4)/ TIM1_CH2N/LCD_SEG13(2)/ADC1_IN15/ COMP1_INP | I/O | TT(3) | **X** | X | X | HS | X | X | **Port B3** | *[Timer 2 - external trigger]* / Timer 1 inverted channel 2 / LCD segment 13 / ADC1_IN15 / Comparator 1 positive input |
| - | - | 15 | E2 | PB3/*[TIM2_ETR]*(4)/ TIM1_CH1N/ LCD_SEG13(2)/ ADC1_IN15/RTC_ALARM /COMP1_INP | I/O | TT(3) | **X** | X | X | HS | X | X | **Port B3** | *[Timer 2 - external trigger]* / Timer 1 inverted channel 1/ LCD segment 13 / ADC1_IN15 / RTC alarm/ Comparator 1 positive input |
| 28 | - | - | - | PB4(6)/*[SPI1_NSS]*(4)/ LCD_SEG14(2)/ ADC1_IN14/COMP1_INP | I/O | TT(3) | **X**(6) | X(6) | X | HS | X | X | **Port B4** | *[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14 / Comparator 1 positive input |
| - | 17 | 16 | D2 | PB4(6)/*[SPI1_NSS]*(4)/ LCD_SEG14(2)/ ADC1_IN14/ COMP1_INP/DAC_OUT | I/O | TT(3) | **X**(6) | X(6) | X | HS | X | X | **Port B4** | *[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14 / DAC output / Comparator 1 positive input |
| 29 | - | - | - | PB5/*[SPI1_SCK]*(4)/ LCD_SEG15(2)/ ADC1_IN13/COMP1_INP | I/O | TT(3) | **X** | X | X | HS | X | X | **Port B5** | *[SPI1 clock]* / LCD segment 15 / ADC1_IN13 / Comparator 1 positive input |
| - | 18 | 17 | D1 | PB5/*[SPI1_SCK]*(4)/ LCD_SEG15(2)/ ADC1_IN13/DAC_OUT/ COMP1_INP | I/O | TT(3) | **X** | X | X | HS | X | X | **Port B5** | *[SPI1 clock]* / LCD segment 15 / ADC1_IN13 / DAC output/ Comparator 1 positive input |

**Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48/UFQFPN48 | LQFP32/UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 30 | - | - | - | PB6/[*SPI1_MOSI*](4)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port B6** | *[SPI1 master out/slave in]*/ LCD segment 16 / ADC1_IN12 / Comparator 1 positive input |
| - | 19 | 18 | F1 | PB6/*[SPI1_MOSI]*(4)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP/ DAC_OUT | I/O | TT (3) | **X** | X | X | HS | X | X | **Port B6** | *[SPI1 master out]*/ slave in / LCD segment 16 / ADC1_IN12 / DAC output / Comparator 1 positive input |
| 31 | 20 | 19 | E1 | PB7/*[SPI1_MISO]*(4)/ LCD_SEG17(2)/ ADC1_IN11/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port B7** | *[SPI1 master in- slave out]* / LCD segment 17 / ADC1_IN11 / Comparator 1 positive input |
| 37 | 25 | 21 | B1 | PC0(5)/I2C1_SDA | I/O | FT | **X** | | X | | T(7) | | **Port C0** | I2C1 data |
| 38 | 26 | 22 | A1 | PC1(5)/I2C1_SCL | I/O | FT | **X** | | X | | T(7) | | **Port C1** | I2C1 clock |
| 41 | 27 | 23 | B2 | PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREFINT | I/O | TT (3) | **X** | X | X | HS | X | X | **Port C2** | USART1 receive / LCD segment 22 / ADC1_IN6 / Comparator 1 positive input / Internal voltage reference output |
| 42 | 28 | 24 | A2 | PC3/USART1_TX/ LCD_SEG23(2)/ ADC1_IN5/COMP1_INP/ COMP2_INM | I/O | TT (3) | **X** | X | X | HS | X | X | **Port C3** | USART1 transmit / LCD segment 23 / ADC1_IN5 / Comparator 1 positive input / Comparator 2 negative input |
| 43 | 29 | 25 | C2 | PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24(2)/ ADC1_IN4/COMP2_INM/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port C4** | USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input |

**Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48/UFQFPN48 | LQFP32/UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 44 | 30 | 26 | A3 | PC5/OSC32_IN /*[SPI1_NSS]*(4)/ *[USART1_TX]*(4) | I/O | | **X** | X | X | HS | X | X | **Port C5** | LSE oscillator input / *[SPI1 master/slave select] / [USART1 transmit]* |
| 45 | 31 | 27 | B3 | PC6/OSC32_OUT/ *[SPI1_SCK]*(4)/ *[USART1_RX]*(4) | I/O | | **X** | X | X | HS | X | X | **Port C6** | LSE oscillator output / *[SPI1 clock] / [USART1 receive]* |
| 46 | - | - | - | PC7/LCD_SEG25(2)/ ADC1_IN3/COMP2_INM/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port C7** | LCD segment 25 /ADC1_IN3/ Comparator negative input / Comparator 1 positive input |
| 20 | - | 8 | G3 | PD0/TIM3_CH2/ *[ADC1_TRIG]*(4)/ LCD_SEG7(2)/ADC1_IN22/COMP2_INP/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port D0** | Timer 3 - channel 2 / *[ADC1_Trigger]* / LCD segment 7 / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input |
| - | 9 | - | - | PD0/TIM3_CH2/ *[ADC1_TRIG]*(4)/ ADC1_IN22/COMP2_INP/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port D0(8)** | Timer 3 - channel 2 / *[ADC1_Trigger]* / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input |
| 21 | - | - | - | PD1/TIM3_ETR/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port D1** | Timer 3 - external trigger / LCD_COM3 / ADC1_IN21 / comparator 2 positive input / Comparator 1 positive input |
| - | 10 | - | - | PD1/TIM1_CH3N/[*TIM3_ETR*](4)/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port D1** | *[Timer 3 - external trigger]/* TIM1 inverted channel 3 / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input |

## 4.1 System configuration options

As shown in *Table 5: Medium-density STM8L151x4/6, STM8L152x4/6 pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the “Routing interface (RI) and system configuration controller” section in the STM8L15xxx and STM8L16xxx reference manual (RM0031).

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5055 to 0x00 506F | Reserved area (27 bytes) | | | |
| 0x00 5070 | DMA1 | DMA1_GCSR | DMA1 global configuration & status register | 0xFC |
| 0x00 5071 | | DMA1_GIR1 | DMA1 global interrupt register 1 | 0x00 |
| 0x00 5072 to 0x00 5074 | | Reserved area (3 bytes) | | |
| 0x00 5075 | | DMA1_C0CR | DMA1 channel 0 configuration register | 0x00 |
| 0x00 5076 | | DMA1_C0SPR | DMA1 channel 0 status & priority register | 0x00 |
| 0x00 5077 | | DMA1_C0NDTR | DMA1 number of data to transfer register (channel 0) | 0x00 |
| 0x00 5078 | | DMA1_C0PARH | DMA1 peripheral address high register (channel 0) | 0x52 |
| 0x00 5079 | | DMA1_C0PARL | DMA1 peripheral address low register (channel 0) | 0x00 |
| 0x00 507A | | Reserved area (1 byte) | | |
| 0x00 507B | | DMA1_C0M0ARH | DMA1 memory 0 address high register (channel 0) | 0x00 |
| 0x00 507C | | DMA1_C0M0ARL | DMA1 memory 0 address low register (channel 0) | 0x00 |
| 0x00 507D to 0x00 507E | | Reserved area (2 bytes) | | |
| 0x00 507F | | DMA1_C1CR | DMA1 channel 1 configuration register | 0x00 |
| 0x00 5080 | | DMA1_C1SPR | DMA1 channel 1 status & priority register | 0x00 |
| 0x00 5081 | | DMA1_C1NDTR | DMA1 number of data to transfer register (channel 1) | 0x00 |
| 0x00 5082 | | DMA1_C1PARH | DMA1 peripheral address high register (channel 1) | 0x52 |
| 0x00 5083 | | DMA1_C1PARL | DMA1 peripheral address low register (channel 1) | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5084 | DMA1 | Reserved area (1 byte) | | |
| 0x00 5085 | | DMA1_C1M0ARH | DMA1 memory 0 address high register (channel 1) | 0x00 |
| 0x00 5086 | | DMA1_C1M0ARL | DMA1 memory 0 address low register (channel 1) | 0x00 |
| 0x00 5087<br>0x00 5088 | | Reserved area (2 bytes) | | |
| 0x00 5089 | | DMA1_C2CR | DMA1 channel 2 configuration register | 0x00 |
| 0x00 508A | | DMA1_C2SPR | DMA1 channel 2 status & priority register | 0x00 |
| 0x00 508B | | DMA1_C2NDTR | DMA1 number of data to transfer register (channel 2) | 0x00 |
| 0x00 508C | | DMA1_C2PARH | DMA1 peripheral address high register (channel 2) | 0x52 |
| 0x00 508D | | DMA1_C2PARL | DMA1 peripheral address low register (channel 2) | 0x00 |
| 0x00 508E | | Reserved area (1 byte) | | |
| 0x00 508F | | DMA1_C2M0ARH | DMA1 memory 0 address high register (channel 2) | 0x00 |
| 0x00 5090 | | DMA1_C2M0ARL | DMA1 memory 0 address low register (channel 2) | 0x00 |
| 0x00 5091<br>0x00 5092 | | Reserved area (2 bytes) | | |
| 0x00 5093 | | DMA1_C3CR | DMA1 channel 3 configuration register | 0x00 |
| 0x00 5094 | | DMA1_C3SPR | DMA1 channel 3 status & priority register | 0x00 |
| 0x00 5095 | | DMA1_C3NDTR | DMA1 number of data to transfer register (channel 3) | 0x00 |
| 0x00 5096 | | DMA1_C3PARH_<br>C3M1ARH | DMA1 peripheral address high register (channel 3) | 0x40 |
| 0x00 5097 | | DMA1_C3PARL_<br>C3M1ARL | DMA1 peripheral address low register (channel 3) | 0x00 |
| 0x00 5098 | | Reserved area (1 byte) | | |
| 0x00 5099 | | DMA1_C3M0ARH | DMA1 memory 0 address high register (channel 3) | 0x00 |
| 0x00 509A | | DMA1_C3M0ARL | DMA1 memory 0 address low register (channel 3) | 0x00 |
| 0x00 509B to<br>0x00 509D | | Reserved area (3 bytes) | | |
| 0x00 509E | SYSCFG | SYSCFG_RMPCR1 | Remapping register 1 | 0x00 |
| 0x00 509F | | SYSCFG_RMPCR2 | Remapping register 2 | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5280 | TIM3 | TIM3_CR1 | TIM3 control register 1 | 0x00 |
| 0x00 5281 | | TIM3_CR2 | TIM3 control register 2 | 0x00 |
| 0x00 5282 | | TIM3_SMCR | TIM3 Slave mode control register | 0x00 |
| 0x00 5283 | | TIM3_ETR | TIM3 external trigger register | 0x00 |
| 0x00 5284 | | TIM3_DER | TIM3 DMA1 request enable register | 0x00 |
| 0x00 5285 | | TIM3_IER | TIM3 interrupt enable register | 0x00 |
| 0x00 5286 | | TIM3_SR1 | TIM3 status register 1 | 0x00 |
| 0x00 5287 | | TIM3_SR2 | TIM3 status register 2 | 0x00 |
| 0x00 5288 | | TIM3_EGR | TIM3 event generation register | 0x00 |
| 0x00 5289 | | TIM3_CCMR1 | TIM3 Capture/Compare mode register 1 | 0x00 |
| 0x00 528A | | TIM3_CCMR2 | TIM3 Capture/Compare mode register 2 | 0x00 |
| 0x00 528B | | TIM3_CCER1 | TIM3 Capture/Compare enable register 1 | 0x00 |
| 0x00 528C | | TIM3_CNTRH | TIM3 counter high | 0x00 |
| 0x00 528D | | TIM3_CNTRL | TIM3 counter low | 0x00 |
| 0x00 528E | | TIM3_PSCR | TIM3 prescaler register | 0x00 |
| 0x00 528F | | TIM3_ARRH | TIM3 Auto-reload register high | 0xFF |
| 0x00 5290 | | TIM3_ARRL | TIM3 Auto-reload register low | 0xFF |
| 0x00 5291 | | TIM3_CCR1H | TIM3 Capture/Compare register 1 high | 0x00 |
| 0x00 5292 | | TIM3_CCR1L | TIM3 Capture/Compare register 1 low | 0x00 |
| 0x00 5293 | | TIM3_CCR2H | TIM3 Capture/Compare register 2 high | 0x00 |
| 0x00 5294 | | TIM3_CCR2L | TIM3 Capture/Compare register 2 low | 0x00 |
| 0x00 5295 | | TIM3_BKR | TIM3 break register | 0x00 |
| 0x00 5296 | | TIM3_OISR | TIM3 output idle state register | 0x00 |
| 0x00 5297 to 0x00 52AF | Reserved area (25 bytes) | | | |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 52B0 | TIM1 | TIM1_CR1 | TIM1 control register 1 | 0x00 |
| 0x00 52B1 | | TIM1_CR2 | TIM1 control register 2 | 0x00 |
| 0x00 52B2 | | TIM1_SMCR | TIM1 Slave mode control register | 0x00 |
| 0x00 52B3 | | TIM1_ETR | TIM1 external trigger register | 0x00 |
| 0x00 52B4 | | TIM1_DER | TIM1 DMA1 request enable register | 0x00 |
| 0x00 52B5 | | TIM1_IER | TIM1 Interrupt enable register | 0x00 |
| 0x00 52B6 | | TIM1_SR1 | TIM1 status register 1 | 0x00 |
| 0x00 52B7 | | TIM1_SR2 | TIM1 status register 2 | 0x00 |
| 0x00 52B8 | | TIM1_EGR | TIM1 event generation register | 0x00 |
| 0x00 52B9 | | TIM1_CCMR1 | TIM1 Capture/Compare mode register 1 | 0x00 |
| 0x00 52BA | | TIM1_CCMR2 | TIM1 Capture/Compare mode register 2 | 0x00 |
| 0x00 52BB | | TIM1_CCMR3 | TIM1 Capture/Compare mode register 3 | 0x00 |
| 0x00 52BC | | TIM1_CCMR4 | TIM1 Capture/Compare mode register 4 | 0x00 |
| 0x00 52BD | | TIM1_CCER1 | TIM1 Capture/Compare enable register 1 | 0x00 |
| 0x00 52BE | | TIM1_CCER2 | TIM1 Capture/Compare enable register 2 | 0x00 |
| 0x00 52BF | | TIM1_CNTRH | TIM1 counter high | 0x00 |
| 0x00 52C0 | | TIM1_CNTRL | TIM1 counter low | 0x00 |
| 0x00 52C1 | | TIM1_PSCRH | TIM1 prescaler register high | 0x00 |
| 0x00 52C2 | | TIM1_PSCRL | TIM1 prescaler register low | 0x00 |
| 0x00 52C3 | | TIM1_ARRH | TIM1 Auto-reload register high | 0xFF |
| 0x00 52C4 | | TIM1_ARRL | TIM1 Auto-reload register low | 0xFF |
| 0x00 52C5 | | TIM1_RCR | TIM1 Repetition counter register | 0x00 |
| 0x00 52C6 | | TIM1_CCR1H | TIM1 Capture/Compare register 1 high | 0x00 |
| 0x00 52C7 | | TIM1_CCR1L | TIM1 Capture/Compare register 1 low | 0x00 |
| 0x00 52C8 | | TIM1_CCR2H | TIM1 Capture/Compare register 2 high | 0x00 |
| 0x00 52C9 | | TIM1_CCR2L | TIM1 Capture/Compare register 2 low | 0x00 |
| 0x00 52CA | | TIM1_CCR3H | TIM1 Capture/Compare register 3 high | 0x00 |
| 0x00 52CB | | TIM1_CCR3L | TIM1 Capture/Compare register 3 low | 0x00 |
| 0x00 52CC | | TIM1_CCR4H | TIM1 Capture/Compare register 4 high | 0x00 |
| 0x00 52CD | | TIM1_CCR4L | TIM1 Capture/Compare register 4 low | 0x00 |
| 0x00 52CE | | TIM1_BKR | TIM1 break register | 0x00 |
| 0x00 52CF | | TIM1_DTR | TIM1 dead-time register | 0x00 |
| 0x00 52D0 | | TIM1_OISR | TIM1 output idle state register | 0x00 |
| 0x00 52D1 | | TIM1_DCR1 | DMA1 control register 1 | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 534E | ADC1 | ADC1_TRIGR1 | ADC1 trigger disable 1 | 0x00 |
| 0x00 534F | | ADC1_TRIGR2 | ADC1 trigger disable 2 | 0x00 |
| 0x00 5350 | | ADC1_TRIGR3 | ADC1 trigger disable 3 | 0x00 |
| 0x00 5351 | | ADC1_TRIGR4 | ADC1 trigger disable 4 | 0x00 |
| 0x00 5352 to 0x00 537F | Reserved area (46 bytes) | | | |
| 0x00 5380 | DAC | DAC_CR1 | DAC control register 1 | 0x00 |
| 0x00 5381 | | DAC_CR2 | DAC control register 2 | 0x00 |
| 0x00 5382 to 0x00 5383 | | Reserved area (2 bytes) | | |
| 0x00 5384 | | DAC_SWTRIGR | DAC software trigger register | 0x00 |
| 0x00 5385 | | DAC_SR | DAC status register | 0x00 |
| 0x00 5386 to 0x00 5387 | | Reserved area (2 bytes) | | |
| 0x00 5388 | | DAC_RDHRH | DAC right aligned data holding register high | 0x00 |
| 0x00 5389 | | DAC_RDHRL | DAC right aligned data holding register low | 0x00 |
| 0x00 538A to 0x00 538B | | Reserved area (2 bytes) | | |
| 0x00 538C | | DAC_LDHRH | DAC left aligned data holding register high | 0x00 |
| 0x00 538D | | DAC_LDHRL | DAC left aligned data holding register low | 0x00 |
| 0x00 538E to 0x00 538F | | Reserved area (2 bytes) | | |
| 0x00 5390 | | DAC_DHR8 | DAC 8-bit data holding register | 0x00 |
| 0x00 5391 to 0x00 53AB | | Reserved area (27 bytes) | | |
| 0x00 53AC | | DAC_DORH | DAC data output register high | 0x00 |
| 0x00 53AD | | DAC_DORL | DAC data output register low | 0x00 |
| 0x00 53AE to 0x00 53FF | Reserved area (82 bytes) | | | |

In the following table, data is based on characterization results, unless otherwise specified.

**Table 22. Total current consumption and timing in Low power run mode at $V_{DD}$ = 1.65 V to 3.6 V**

| Symbol | Parameter | Conditions[1] | | | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(LPR)}$ | Supply current in Low power run mode | LSI RC osc. (at 38 kHz) | all peripherals OFF | $T_A$ = -40 °C to 25 °C | 5.1 | 5.4 | µA |
| | | | | $T_A$ = 55 °C | 5.7 | 6 | |
| | | | | $T_A$ = 85 °C | 6.8 | 7.5 | |
| | | | | $T_A$ = 105 °C | 9.2 | 10.4 | |
| | | | | $T_A$ = 125 °C | 13.4 | 16.6 | |
| | | | with TIM2 active[2] | $T_A$ = -40 °C to 25 °C | 5.4 | 5.7 | |
| | | | | $T_A$ = 55 °C | 6.0 | 6.3 | |
| | | | | $T_A$ = 85 °C | 7.2 | 7.8 | |
| | | | | $T_A$ = 105 °C | 9.4 | 10.7 | |
| | | | | $T_A$ = 125 °C | 13.8 | 17 | |
| | | LSE [3] external clock (32.768 kHz) | all peripherals OFF | $T_A$ = -40 °C to 25 °C | 5.25 | 5.6 | |
| | | | | $T_A$ = 55 °C | 5.67 | 6.1 | |
| | | | | $T_A$ = 85 °C | 5.85 | 6.3 | |
| | | | | $T_A$ = 105 °C | 7.11 | 7.6 | |
| | | | | $T_A$ = 125 °C | 9.84 | 12 | |
| | | | with TIM2 active [2] | $T_A$ = -40 °C to 25 °C | 5.59 | 6 | |
| | | | | $T_A$ = 55 °C | 6.10 | 6.4 | |
| | | | | $T_A$ = 85 °C | 6.30 | 7 | |
| | | | | $T_A$ = 105 °C | 7.55 | 8.4 | |
| | | | | $T_A$ = 125 °C | 10.1 | 15 | |

1. No floating I/Os
2. Timer 2 clock enabled and counter running
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*

**Figure 15. Typ. $I_{DD(LPR)}$ vs. $V_{DD}$ (LSI clock source)**

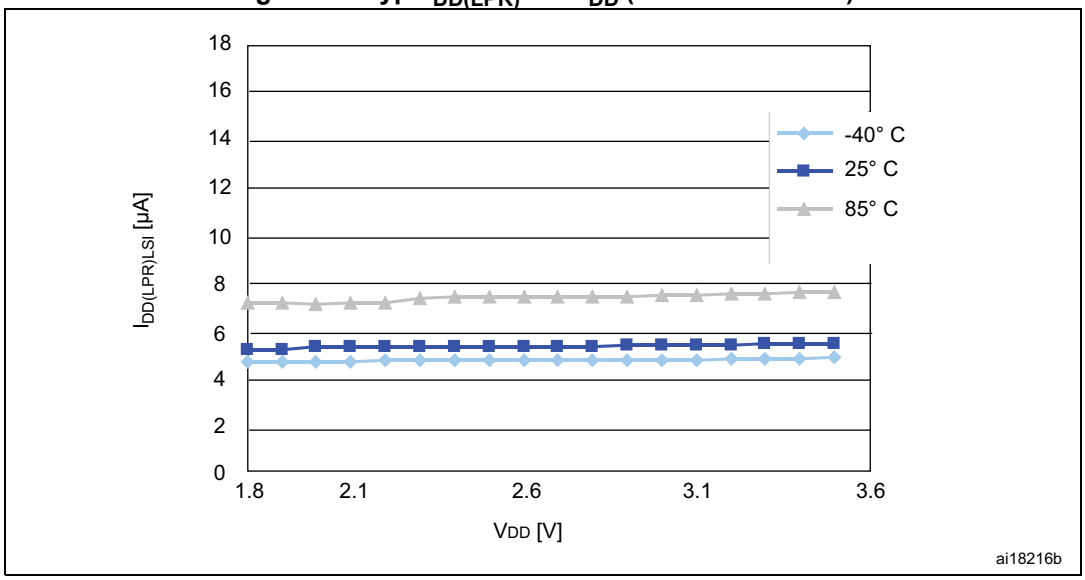
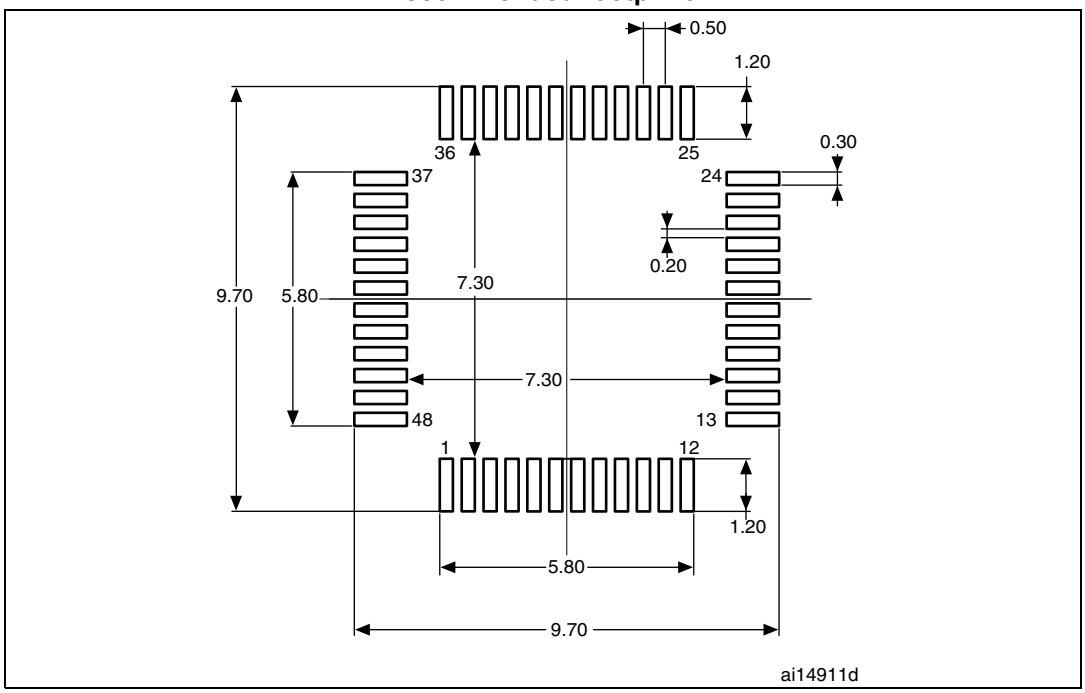


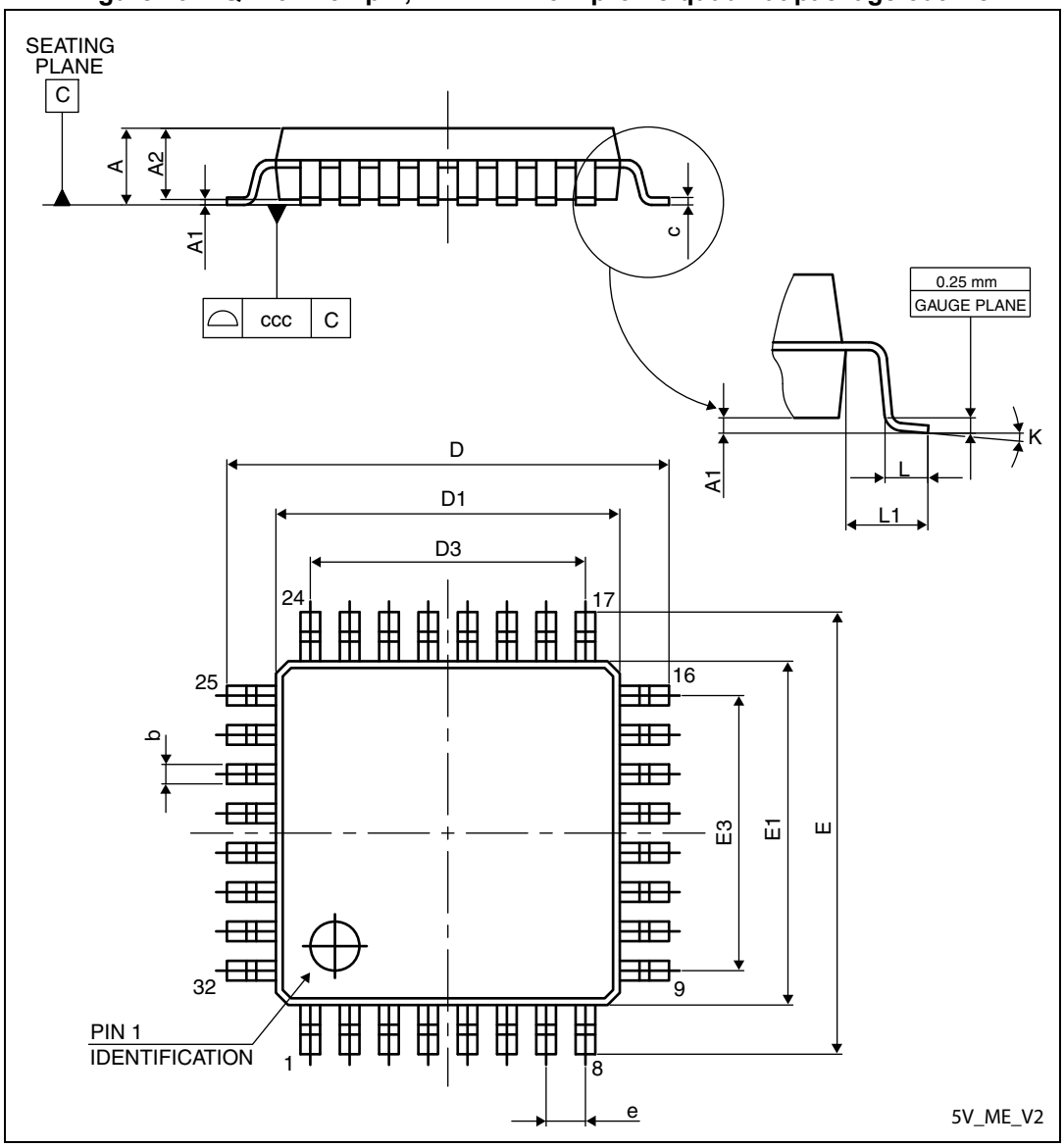
**Figure 44. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

## 10.4 LQFP32 package information

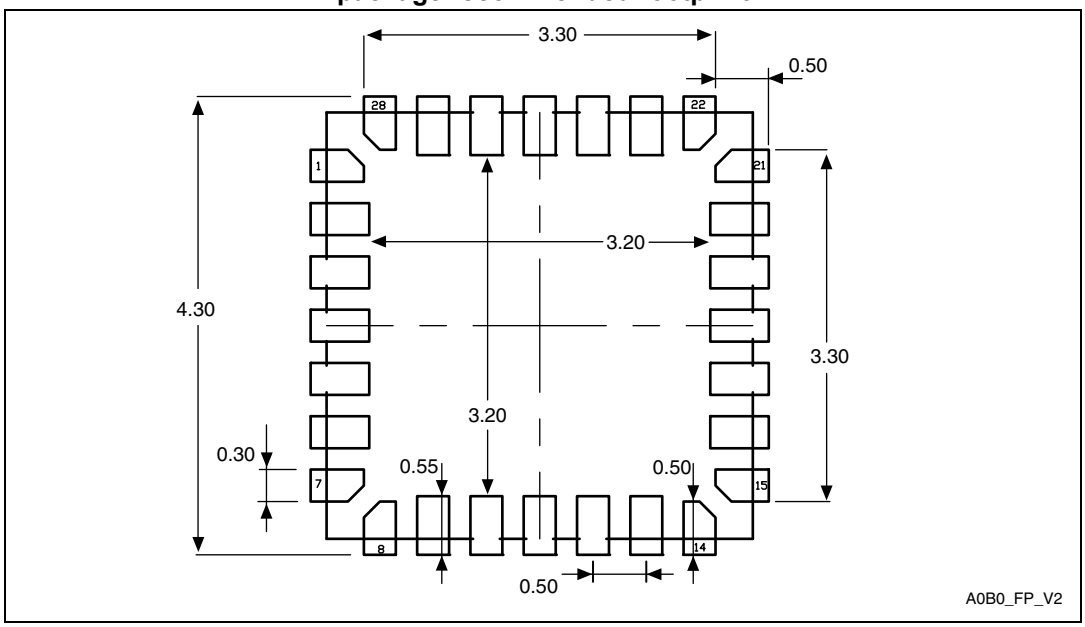
**Figure 49. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline**




1. Drawing is not to scale.

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 56. UFQFPN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

**Table 69. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 23-Jul-2010 | 5 | Modified *Introduction* and *Description.*<br>Modified *Table: Legend/abbreviation for table 5* and *Table: Medium density STM8L15x pin description* (for PA0, PA1, PB0 and PB4 and for reset states in the floating input column)<br>Modified *Figure: Low density STM8L151xx device block diagram, Figure: Low density STM8L15x clock tree diagram*, *Figure: Low power modes* and *Figure : Low power real-time clock.*<br>Modified CLK_PCKENR2 and CLK_HSICALR reset values in *Table: General hardware register map.*<br>Modified notes below *Figure: Memory map.*<br>Modified PA_CR1 reset value.<br>Modified reset values for Px_IDR registers.<br>Modified *Table: Voltage characteristics* and *Table: Current characteristics.*<br>Modified $V_{IH}$ in *Table: I/O static characteristics.*<br>Modified *Table: Total current consumption in Wait mode.*<br>Modified *Figure Typical application with I2C bus and timing diagram 1).*<br>Modified $I_L$ value in *Figure: Typical connection diagram using the ADC1.*<br>Modified $R_H$ and $R_L$ in *Table: LCD characteristics.*<br>Added graphs in *Section: Electrical parameters.*<br>Modified note 3 below *Table: Reference voltage characteristics.*<br>Modified note 1 below *Table: TS characteristics.*<br>Changed $V_{ESD(CDM)}$ value in *Table: ESD absolute maximum ratings.*<br>Updated notes for UFQFPN32 and UFQFPN48 packages. |
| 11-Mar-2011 | 6 | Modified note on true open drain I/Os and I/O level columns in *Table: Medium density STM8L15x pin description.*<br>Remapping option removed for USART1_TX, USART1_RX, and USART1_CK on PC2, PC3 and PC4 in *Table: Medium density STM8L15x pin description.*<br>Modified IDWDG_KR reset value in *Table: General hardware register map.*<br>Replaced VREF_OUT with VREFINT and TIMx_TRIG with TIMx_ETR.<br>Added *Table: Factory conversion registers.* Modified reset values for TIM1_DCR1, IWDG_KR, RTC_DR1, RTC_DR2, RTC_SPRERH, RTC_SPRERL, RTC_APRER, RTC_WUTRH, and RTC_WUTRL in *Table: General hardware register map.*<br>Added notes to certain values in *Section: Embedded reference voltage* and *Section: Temperature sensor.* |