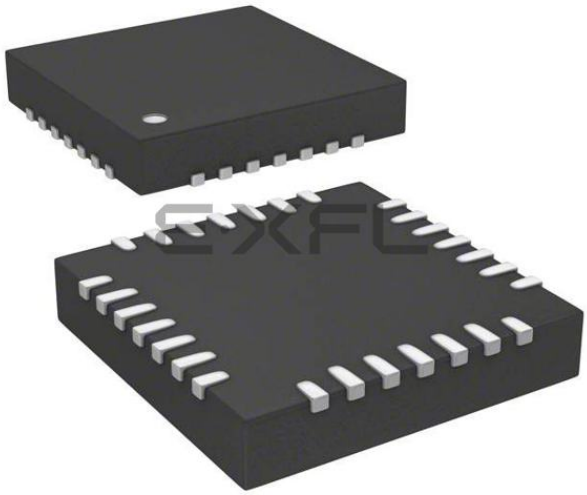

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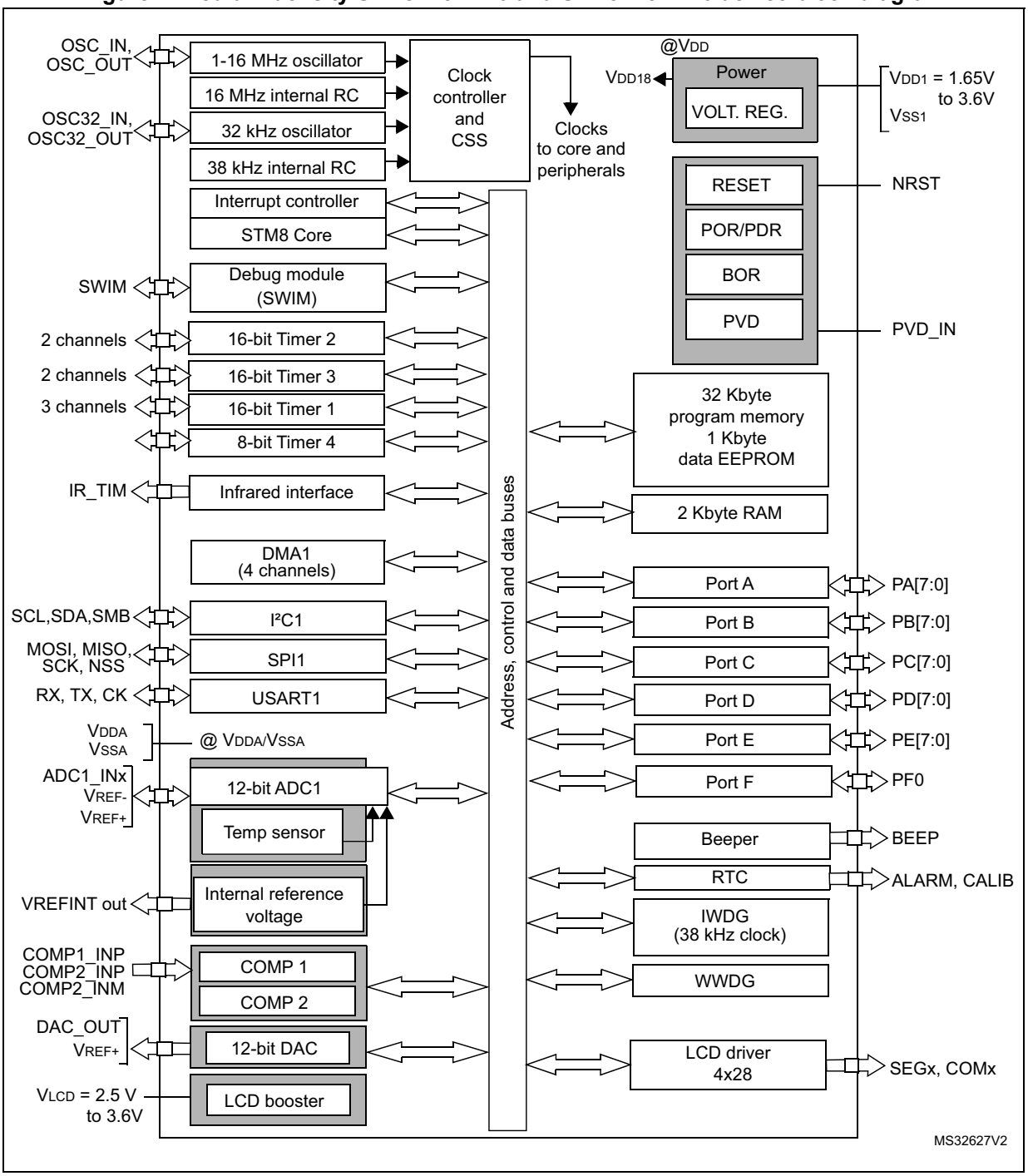
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151g6u6tr

List of tables

3 Functional overview

Figure 1. Medium-density STM8L151x4/6 and STM8L152x4/6 device block diagram



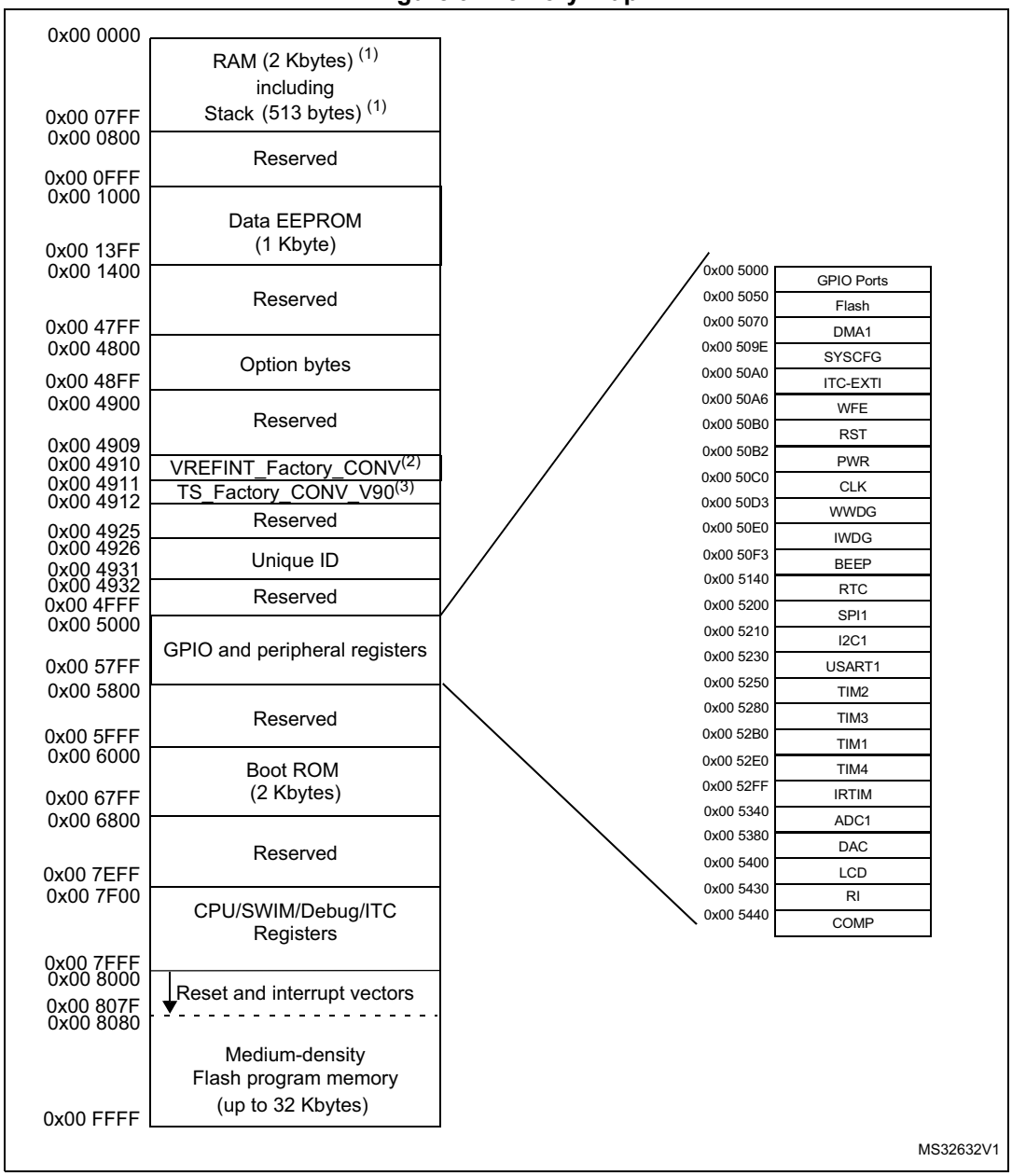
1. **Legend**:
   ADC: Analog-to-digital converter
   BOR: Brownout reset
   DMA: Direct memory access
   DAC: Digital-to-analog converter
   I²C: Inter-integrated circuit multi master interface

5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 9*.

Figure 9. Memory map



1. *Table 6* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. The VREFINT_Factory_CONV byte represents the LSB of the V_{REFINT} 12-bit ADC conversion result. The MSB have a fixed value: 0x6.
3. The TS_Factory_CONV_V90 byte represents the LSB of the V_{90} 12-bit ADC conversion result. The MSB

have a fixed value: 0x3.

4. Refer to *Table 9* for an overview of hardware register mapping, to *Table 8* for details on I/O port hardware registers, and to *Table 10* for information on CPU/SWIM/debug module controller registers.

Table 6. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	2 Kbyte	0x00 0000	0x00 07FF
Flash program memory	16 Kbyte	0x00 8000	0x00 BFFF
	32 Kbyte	0x00 8000	0x00 FFFF

5.2 Register map

Table 7. Factory conversion registers

Address	Block	Register label	Register name	Reset status
0x00 4910	-	VREFINT_Factory_CONV(1)	Internal reference voltage factory conversion	0xXX
0x00 4911	-	TS_Factory_CONV_V90(2)	Temperature sensor output voltage	0xXX

1. The VREFINT_Factory_CONV byte represents the 8 LSB of the result of the VREFINT 12-bit ADC conversion performed in factory. The MSB have a fixed value: 0x6.
2. The TS_Factory_CONV_V90 byte represents the 8 LSB of the result of the V90 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x3.

Table 8. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x01
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50D0 to 0x00 50D2	Reserved area (3 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 bytes)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to 0x00 513F	Reserved area (76 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5140	RTC	RTC_TR1	Time register 1	0x00
0x00 5141		RTC_TR2	Time register 2	0x00
0x00 5142		RTC_TR3	Time register 3	0x00
0x00 5143		Reserved area (1 byte)		
0x00 5144		RTC_DR1	Date register 1	0x01
0x00 5145		RTC_DR2	Date register 2	0x21
0x00 5146		RTC_DR3	Date register 3	0x00
0x00 5147		Reserved area (1 byte)		
0x00 5148		RTC_CR1	Control register 1	0x00
0x00 5149		RTC_CR2	Control register 2	0x00
0x00 514A		RTC_CR3	Control register 3	0x00
0x00 514B		Reserved area (1 byte)		
0x00 514C		RTC_ISR1	Initialization and status register 1	0x00
0x00 514D		RTC_ISR2	Initialization and Status register 2	0x00
0x00 514E 0x00 514F		Reserved area (2 bytes)		
0x00 5150		RTC_SPRERH(1)	Synchronous prescaler register high	0x00(1)
0x00 5151		RTC_SPRERL(1)	Synchronous prescaler register low	0xFF(1)
0x00 5152		RTC_APRER(1)	Asynchronous prescaler register	0x7F(1)
0x00 5153		Reserved area (1 byte)		
0x00 5154		RTC_WUTRH(1)	Wakeup timer register high	0xFF(1)
0x00 5155		RTC_WUTRL(1)	Wakeup timer register low	0xFF(1)
0x00 5156 to 0x00 5158		Reserved area (3 bytes)		
0x00 5159		RTC_WPR	Write protection register	0x00
0x00 515A 0x00 515B		Reserved area (2 bytes)		
0x00 515C		RTC_ALRMAR1	Alarm A register 1	0x00
0x00 515D		RTC_ALRMAR2	Alarm A register 2	0x00
0x00 515E		RTC_ALRMAR3	Alarm A register 3	0x00
0x00 515F		RTC_ALRMAR4	Alarm A register 4	0x00
0x00 5160 to 0x00 51FF	Reserved area (160 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52B0	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 52B1		TIM1_CR2	TIM1 control register 2	0x00
0x00 52B2		TIM1_SMCR	TIM1 Slave mode control register	0x00
0x00 52B3		TIM1_ETR	TIM1 external trigger register	0x00
0x00 52B4		TIM1_DER	TIM1 DMA1 request enable register	0x00
0x00 52B5		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 52B6		TIM1_SR1	TIM1 status register 1	0x00
0x00 52B7		TIM1_SR2	TIM1 status register 2	0x00
0x00 52B8		TIM1_EGR	TIM1 event generation register	0x00
0x00 52B9		TIM1_CCMR1	TIM1 Capture/Compare mode register 1	0x00
0x00 52BA		TIM1_CCMR2	TIM1 Capture/Compare mode register 2	0x00
0x00 52BB		TIM1_CCMR3	TIM1 Capture/Compare mode register 3	0x00
0x00 52BC		TIM1_CCMR4	TIM1 Capture/Compare mode register 4	0x00
0x00 52BD		TIM1_CCER1	TIM1 Capture/Compare enable register 1	0x00
0x00 52BE		TIM1_CCER2	TIM1 Capture/Compare enable register 2	0x00
0x00 52BF		TIM1_CNTRH	TIM1 counter high	0x00
0x00 52C0		TIM1_CNTRL	TIM1 counter low	0x00
0x00 52C1		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 52C2		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 52C3		TIM1_ARRH	TIM1 Auto-reload register high	0xFF
0x00 52C4		TIM1_ARRL	TIM1 Auto-reload register low	0xFF
0x00 52C5		TIM1_RCR	TIM1 Repetition counter register	0x00
0x00 52C6		TIM1_CCR1H	TIM1 Capture/Compare register 1 high	0x00
0x00 52C7		TIM1_CCR1L	TIM1 Capture/Compare register 1 low	0x00
0x00 52C8		TIM1_CCR2H	TIM1 Capture/Compare register 2 high	0x00
0x00 52C9		TIM1_CCR2L	TIM1 Capture/Compare register 2 low	0x00
0x00 52CA		TIM1_CCR3H	TIM1 Capture/Compare register 3 high	0x00
0x00 52CB		TIM1_CCR3L	TIM1 Capture/Compare register 3 low	0x00
0x00 52CC		TIM1_CCR4H	TIM1 Capture/Compare register 4 high	0x00
0x00 52CD		TIM1_CCR4L	TIM1 Capture/Compare register 4 low	0x00
0x00 52CE		TIM1_BKR	TIM1 break register	0x00
0x00 52CF		TIM1_DTR	TIM1 dead-time register	0x00
0x00 52D0		TIM1_OISR	TIM1 output idle state register	0x00
0x00 52D1		TIM1_DCR1	DMA1 control register 1	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5430	RI	Reserved area (1 byte)		0x00
0x00 5431		RI_ICR1	Timer input capture routing register 1	0x00
0x00 5432		RI_ICR2	Timer input capture routing register 2	0x00
0x00 5433		RI_IOIR1	I/O input register 1	undefined
0x00 5434		RI_IOIR2	I/O input register 2	undefined
0x00 5435		RI_IOIR3	I/O input register 3	undefined
0x00 5436		RI_IOCMR1	I/O control mode register 1	0x00
0x00 5437		RI_IOCMR2	I/O control mode register 2	0x00
0x00 5438		RI_IOCMR3	I/O control mode register 3	0x00
0x00 5439		RI_IOSR1	I/O switch register 1	0x00
0x00 543A		RI_IOSR2	I/O switch register 2	0x00
0x00 543B		RI_IOSR3	I/O switch register 3	0x00
0x00 543C		RI_IOGCR	I/O group control register	0x3F
0x00 543D		RI_ASCR1	Analog switch register 1	0x00
0x00 543E		RI_ASCR2	Analog switch register 2	0x00
0x00 543F		RI_RCR	Resistor control register 1	0x00
0x00 5440	COMP	COMP_CSR1	Comparator control and status register 1	0x00
0x00 5441		COMP_CSR2	Comparator control and status register 2	0x00
0x00 5442		COMP_CSR3	Comparator control and status register 3	0x00
0x00 5443		COMP_CSR4	Comparator control and status register 4	0x00
0x00 5444		COMP_CSR5	Comparator control and status register 5	0x00

1. These registers are not impacted by a system reset. They are reset at power-on.

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option bytes can also be modified 'on the fly' by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 12. Option byte addresses

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved										0x00
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x00
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

8 Unique ID

STM8 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4926	X co-ordinate on the wafer	U_ID[7:0]							
0x4927		U_ID[15:8]							
0x4928	Y co-ordinate on the wafer	U_ID[23:16]							
0x4929		U_ID[31:24]							
0x492A	Wafer number	U_ID[39:32]							
0x492B	Lot number	U_ID[47:40]							
0x492C		U_ID[55:48]							
0x492D		U_ID[63:56]							
0x492E		U_ID[71:64]							
0x492F		U_ID[79:72]							
0x4930		U_ID[87:80]							
0x4931		U_ID[95:88]							

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	- 5 / +0	mA
	Injected current on five-volt tolerant (FT) pins (PA7 and PE0) (1)	- 5 / +0	
	Injected current on 3.6 V tolerant (TT) pins (1)	- 5 / +0	
	Injected current on any other pin (2)	- 5 / +5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) (3)	± 25	

1. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15.* for maximum allowed input voltage values.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15.* for maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

9.3.6 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

Table 37. I/O current injection susceptibility

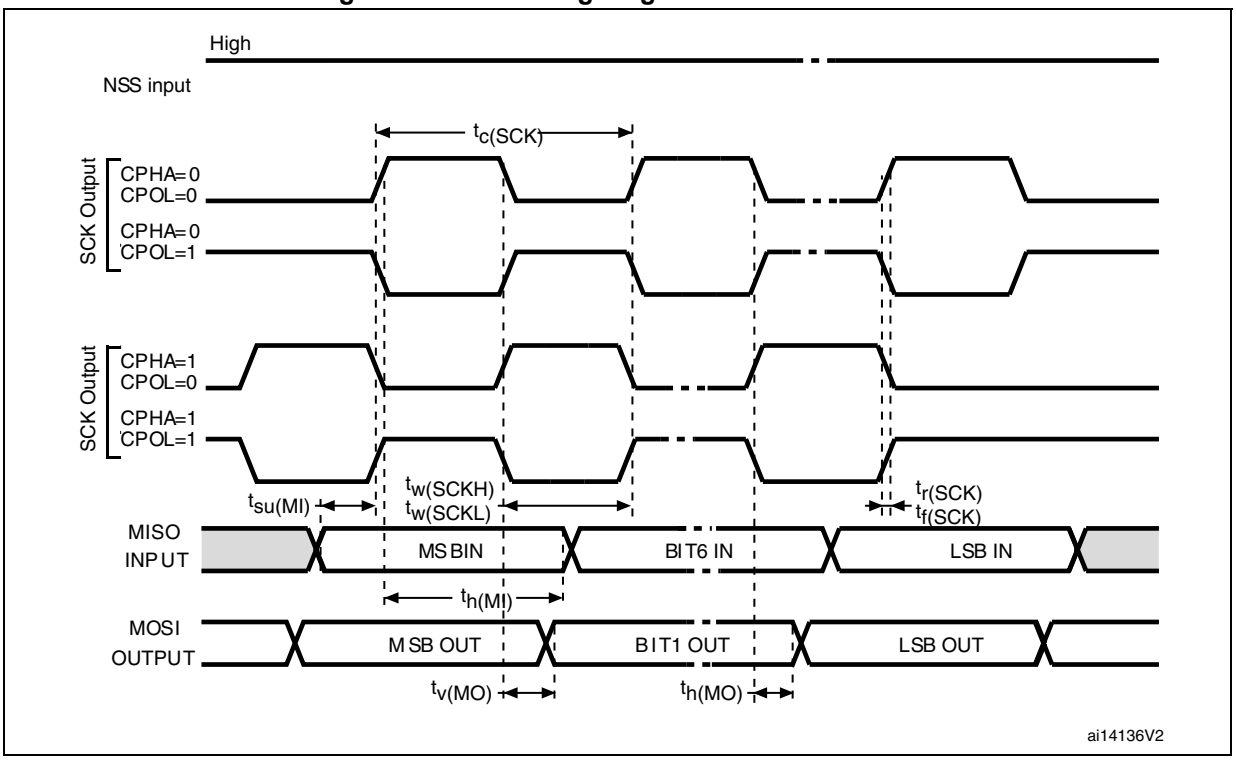
Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on true open-drain pins (PC0 and PC1)	-5	+0	mA
	Injected current on all five-volt tolerant (FT) pins	-5	+0	
	Injected current on all 3.6 V tolerant (TT) pins	-5	+0	
	Injected current on any other pin	-5	+5	

9.3.7 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Figure 36. SPI1 timing diagram - master mode(1)



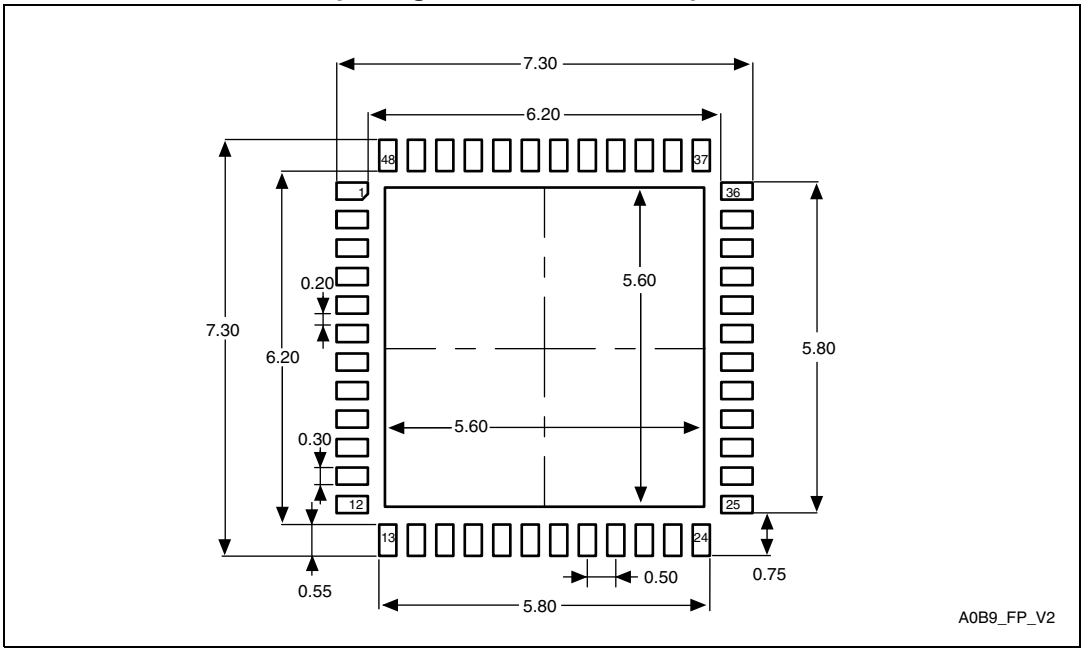
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 63. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

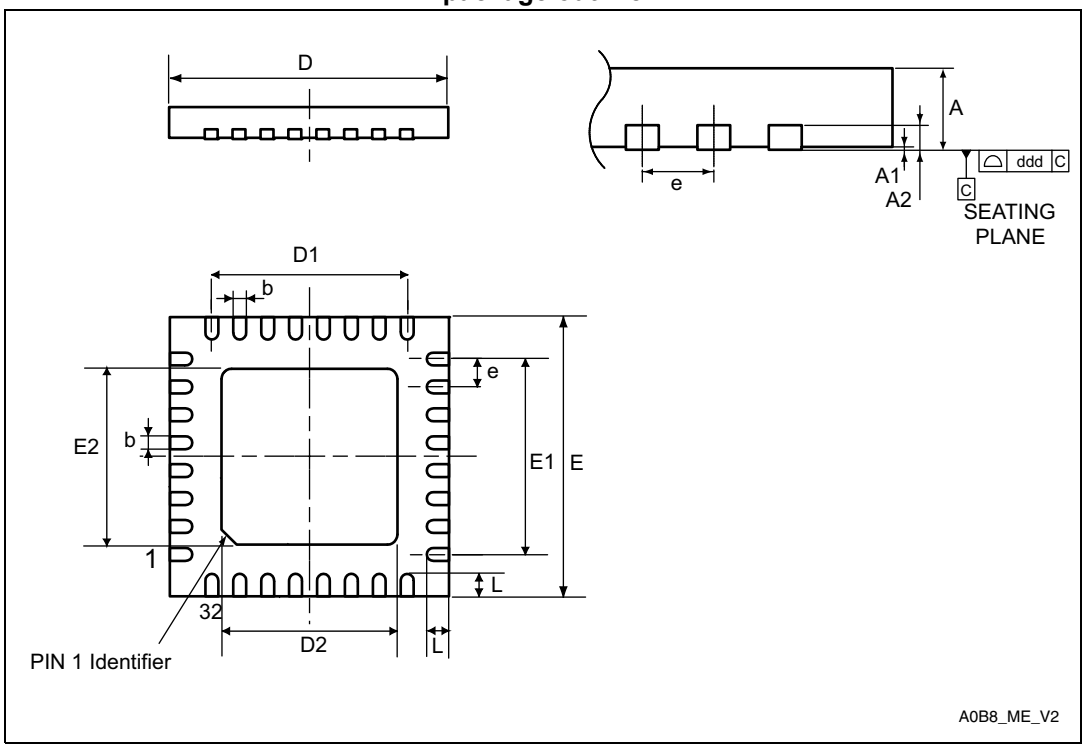


1. Dimensions are expressed in millimeters.

Samples to run qualification activity.

10.5 UFQFPN32 package information

Figure 52. UFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline

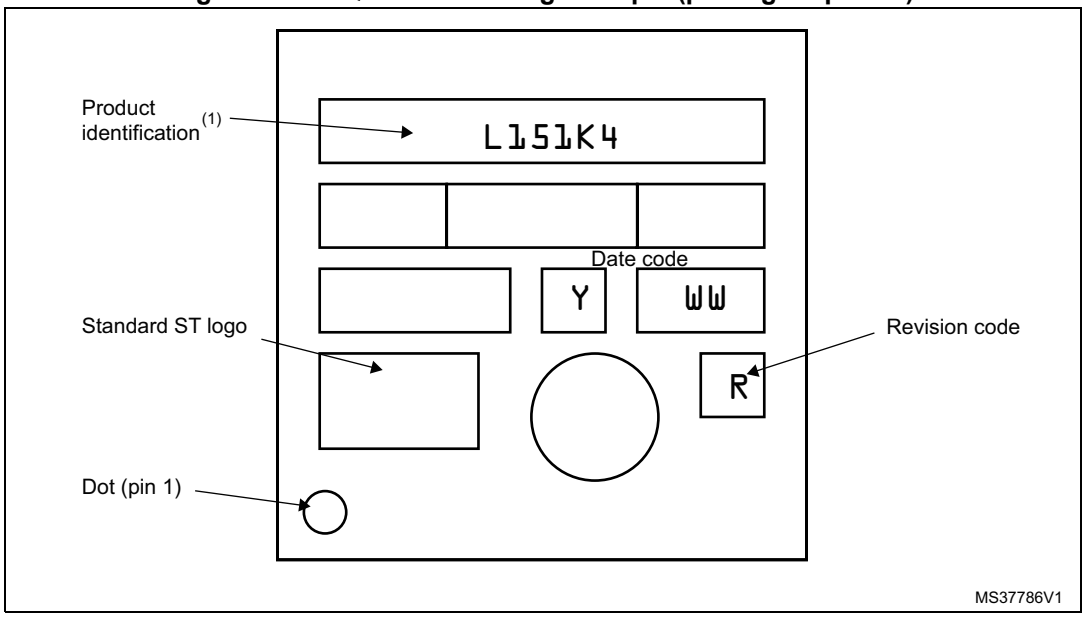


1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

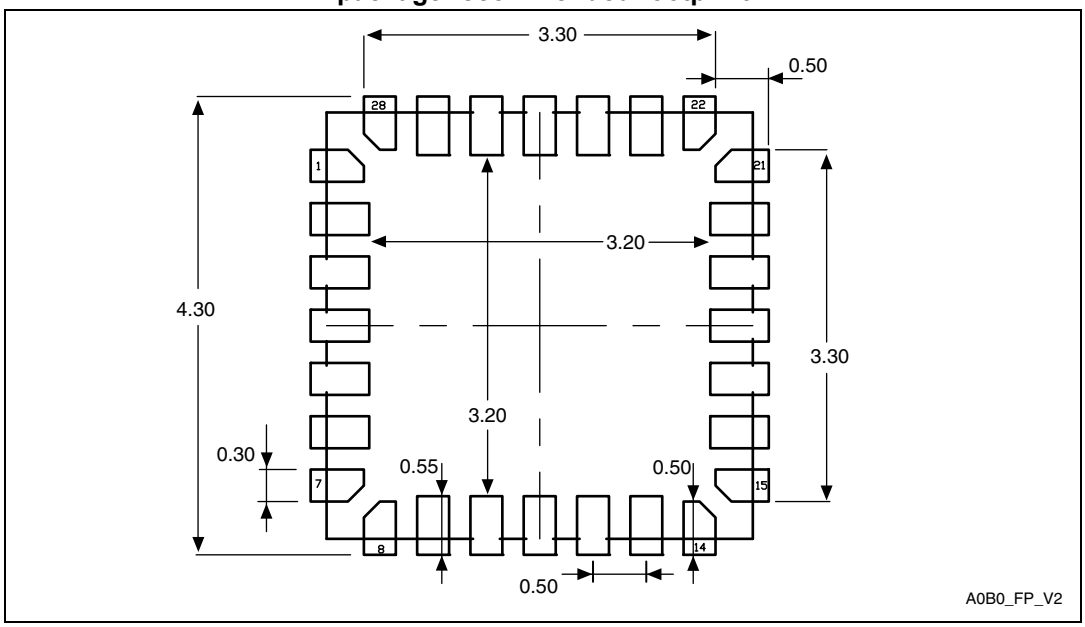
Figure 54. UFQFPN32 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 56. UFQFPN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

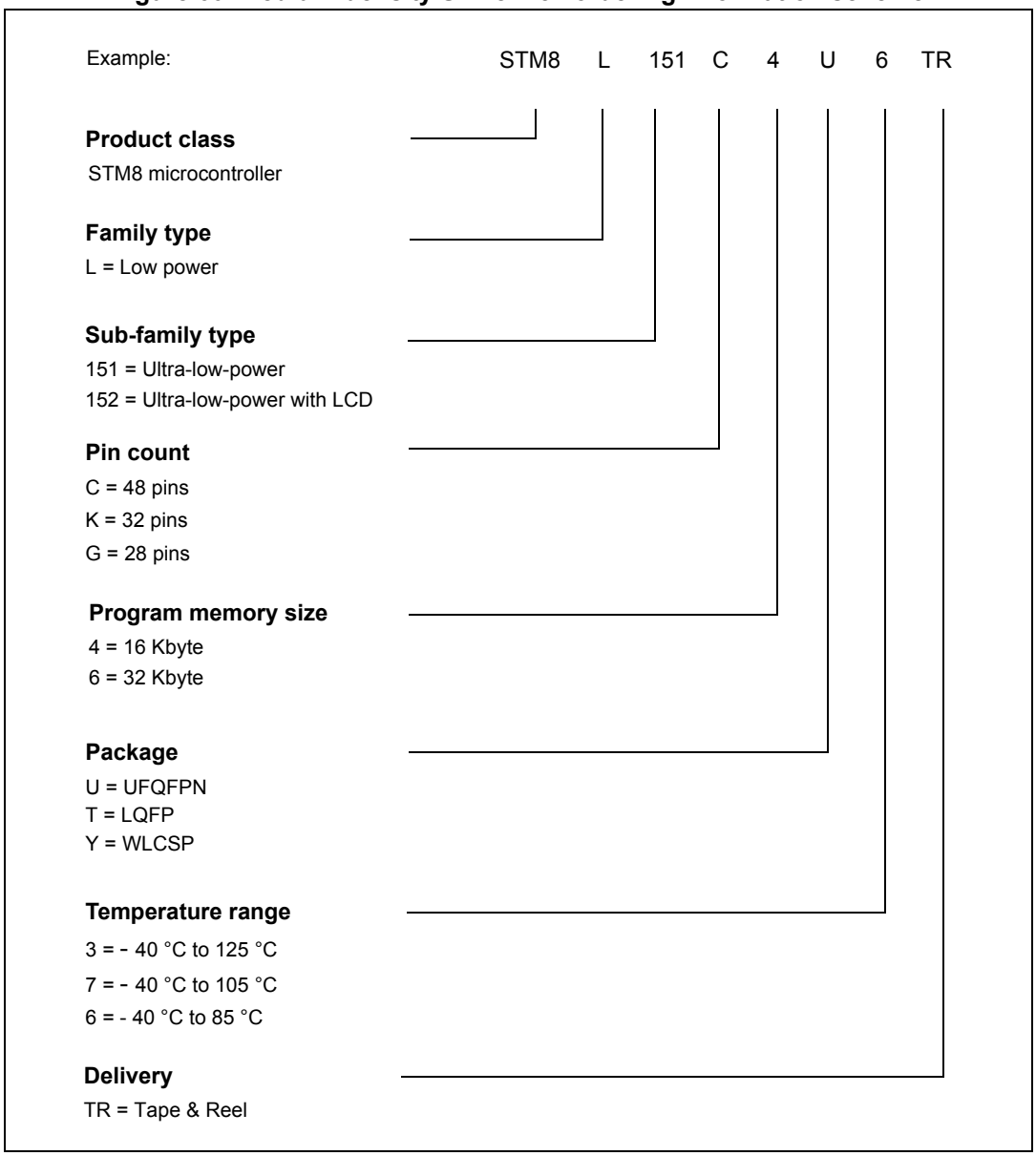


1. Dimensions are expressed in millimeters.

11 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Figure 60. Medium-density STM8L15x ordering information scheme



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please contact the ST sales office nearest to you.

Table 69. Document revision history (continued)

Date	Revision	Changes
10-Feb-2012	8	*Features:* replaced "'Dynamic consumption' with 'Consumption'. *Table: Medium density STM8L15x pin description*: updated OD column of NRST/PA1 pin. *Table: Interrupt mapping:* removed tamper 1, tamper 2 and tamper 3. *Figure: UFQFPN48 package outline:* replaced. *Table: UFQFPN48 package mechanical data:* updated title. *Figure: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5):* removed the line over A1. *Figure: UFQFPN28 package outline:* replaced to improve readability of UFQFPN28 package dimensions A, L, and L1. *Figure: Recommended UFQFPN28 footprint (dimensions in mm)*: updated title. *Figure: WLCSP28 package outline:* updated title. *Table: WLCSP28 package mechanical data:* updated title.
02-Mar-2012	9	Updated *Table: UFQFPN48 package mechanical data.* Updated *Figure: UFQFPN28 package outline, Figure: Recommended UFQFPN28 footprint (dimensions in mm)* and *Table: UFQFPN28 package mechanical data.* *Table: WLCSP28 package mechanical data:* Min and Max values removed for e1, e2, e3, e4, F and G dimensions.
30-Mar-2012	10	*Figure: SPI1 timing diagram - master mode(1):* changed SCK signals to 'output' instead of 'input'. *Figure: Medium density STM8L15x ordering information scheme*: added 'Tape & reel' to package section.
26-Apr-2012	11	Updated *Table: WLCSP28 package mechanical data.*
12-Nov-2013	12	Updated *Table: WLCSP28 package mechanical data.* Updated *Table: Medium-density STM8L15x pin description.* Updated *Table 2: Medium density STM8L15x low power device features and peripheral counts*. Added *Figure: Recommended LQFP48 footprint* and *Figure: Recommended LQFP32 footprint.*
12-Aug-2013	13	Changed the default setting value of OPT5 to 0x00 in *Table: Option byte addresses*. Added tTEMP 'BOR detector enabled' and 'disabled' characteristics in *Table: Embedded reset and power control block characteristics*. Updated E2, D2 and ddd in *Table: UFQFPN48 package mechanical data*