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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFBGA, WLCSP
Supplier Device Package	28-WLCSP (1.7x2.84)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151g6y3tr

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The medium-density STM8L15x microcontroller family is suitable for a wide range of applications:

- Medical and hand-held equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors

Table 4. Legend/abbreviation for table 5

Type	I= input, O = output, S = power supply	
Level	FT	Five-volt tolerant
	TT	3.6 V tolerant
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
2	1	1	C3	NRST/PA1(1)	I/O			**X**		HS		X	**Reset**	PA1
3	2	2	B4	PA2/OSC_IN/ *[USART1_TX]*(4)/ *[SPI1_MISO]* (4)	I/O		**X**	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out] /*
4	3	3	C4	PA3/OSC_OUT/*[USART1_RX]*(4)/*[SPI1_MOSI]*(4)	I/O		**X**	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/*
5	-	-	-	PA4/TIM2_BKIN/ LCD_COM0(2)/ADC1_IN2/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input / LCD COM 0 / ADC1 input 2 / Comparator 1 positive input
-	4	4	D3	PA4/TIM2_BKIN/ *[TIM2_ETR]*(4)/ LCD_COM0(2)/ ADC1_IN2/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input / *[Timer 2 - external trigger]* / LCD_COM 0 / ADC1 input 2 / Comparator 1 positive input
6	-	-	-	PA5/TIM3_BKIN/ LCD_COM1(2)/ADC1_IN1/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input / LCD_COM 1 / ADC1 input 1/ Comparator 1 positive input

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
30	-	-	-	PB6/[*SPI1_MOSI*](4)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out/slave in]*/ LCD segment 16 / ADC1_IN12 / Comparator 1 positive input
-	19	18	F1	PB6/*[SPI1_MOSI]*(4)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP/ DAC_OUT	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out]*/ slave in / LCD segment 16 / ADC1_IN12 / DAC output / Comparator 1 positive input
31	20	19	E1	PB7/*[SPI1_MISO]*(4)/ LCD_SEG17(2)/ ADC1_IN11/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B7**	*[SPI1 master in- slave out]* / LCD segment 17 / ADC1_IN11 / Comparator 1 positive input
37	25	21	B1	PC0(5)/I2C1_SDA	I/O	FT	**X**		X		T(7)		**Port C0**	I2C1 data
38	26	22	A1	PC1(5)/I2C1_SCL	I/O	FT	**X**		X		T(7)		**Port C1**	I2C1 clock
41	27	23	B2	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREFINT	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6 / Comparator 1 positive input / Internal voltage reference output
42	28	24	A2	PC3/USART1_TX/ LCD_SEG23(2)/ ADC1_IN5/COMP1_INP/ COMP2_INM	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5 / Comparator 1 positive input / Comparator 2 negative input
43	29	25	C2	PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24(2)/ ADC1_IN4/COMP2_INM/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C4**	USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
44	30	26	A3	PC5/OSC32_IN /*[SPI1_NSS]*(4)/ *[USART1_TX]*(4)	I/O		**X**	X	X	HS	X	X	**Port C5**	LSE oscillator input / *[SPI1 master/slave select] / [USART1 transmit]*
45	31	27	B3	PC6/OSC32_OUT/ *[SPI1_SCK]*(4)/ *[USART1_RX]*(4)	I/O		**X**	X	X	HS	X	X	**Port C6**	LSE oscillator output / *[SPI1 clock] / [USART1 receive]*
46	-	-	-	PC7/LCD_SEG25(2)/ ADC1_IN3/COMP2_INM/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C7**	LCD segment 25 /ADC1_IN3/ Comparator negative input / Comparator 1 positive input
20	-	8	G3	PD0/TIM3_CH2/ *[ADC1_TRIG]*(4)/ LCD_SEG7(2)/ADC1_IN22/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / LCD segment 7 / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input
-	9	-	-	PD0/TIM3_CH2/ *[ADC1_TRIG]*(4)/ ADC1_IN22/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D0(8)**	Timer 3 - channel 2 / *[ADC1_Trigger]* / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input
21	-	-	-	PD1/TIM3_ETR/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - external trigger / LCD_COM3 / ADC1_IN21 / comparator 2 positive input / Comparator 1 positive input
-	10	-	-	PD1/TIM1_CH3N/[*TIM3_ETR*](4)/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D1**	*[Timer 3 - external trigger]/* TIM1 inverted channel 3 / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

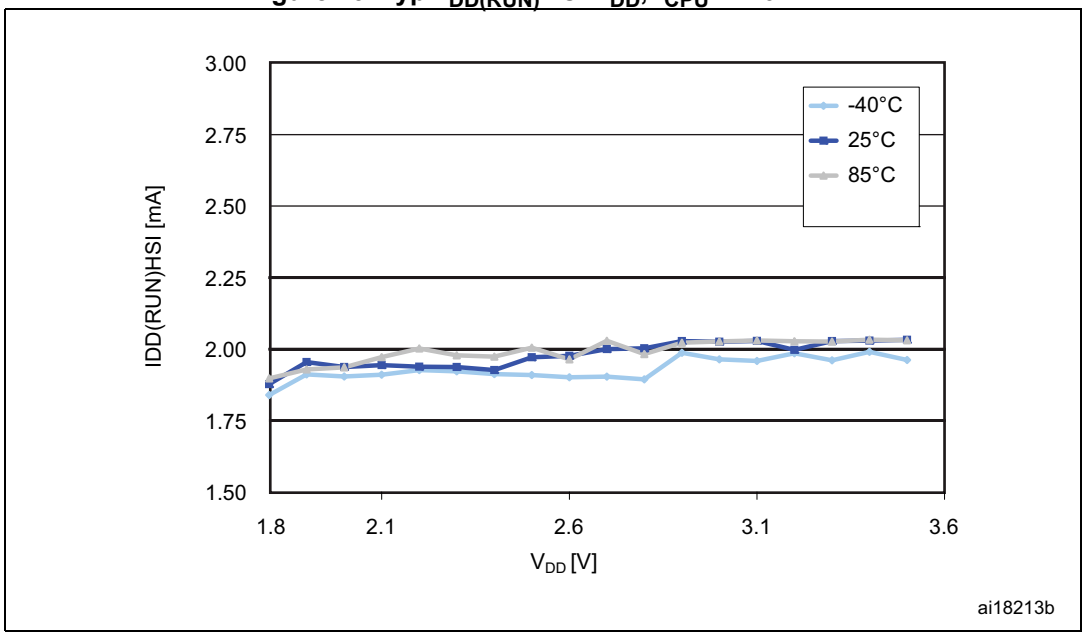
Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	9	G2	PD1/TIM1_CH3/[*TIM3_ETR*](4)/LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D1**	Timer 1 channel 3 / *[Timer 3 - external trigger]* / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input
22	11	10	E4	PD2/TIM1_CH1 /LCD_SEG8(2)/ ADC1_IN20/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D2**	Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20 / Comparator 1 positive input
23	12	-	-	PD3/ TIM1_ETR/ LCD_SEG9(2)/ADC1_IN19/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D3**	Timer 1 - external trigger / LCD segment 9 / ADC1_IN19 / Comparator 1 positive input
-	-	11	F3	PD3/ TIM1_ETR/ LCD_SEG9(2)/ ADC1_IN19/TIM1_BKIN/ COMP1_INP/ RTC_CALIB	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D3**	Timer 1 - external trigger / LCD segment 9 / ADC1_IN19 / Timer 1 break input / RTC calibration / Comparator 1 positive input
33	21	20	C1	PD4/TIM1_CH2 /LCD_SEG18(2)/ ADC1_IN10/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/ Comparator 1 positive input
34	22	-	-	PD5/TIM1_CH3 /LCD_SEG19(2)/ ADC1_IN9/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D5**	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ Comparator 1 positive input
35	23	-	-	PD6/TIM1_BKIN /LCD_SEG20(2)/ ADC1_IN8/RTC_CALIB/ /VREFINT/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D6**	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration / Internal voltage reference output / Comparator 1 positive input

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_DIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00
0x00 50C2		CLK_ICKR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x80
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0bxxxx0000
0x00 50CA		CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0xxx
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11100x

5. CPU executing typical data processing
6. The run from RAM consumption can be approximated with the linear formula:
   I_{DD}(run_from_RAM) = Freq * 90 µA/MHz + 380 µA
7. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 31*.
8. Tested in production.
9. The run from Flash consumption can be approximated with the linear formula:
   I_{DD}(run_from_Flash) = Freq * 195 µA/MHz + 440 µA
10. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*.

Figure 13. Typ. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from RAM

In the following table, data is based on characterization results, unless otherwise specified.

Table 21. Total current consumption in Wait mode

Symbol	Parameter	Conditions(1)			Typ	Max				Unit
						55°C	85 °C(2)	105 °C (3)	125 °C (4)	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from RAM with Flash in I_{DDQ} mode(5), V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.33	0.39	0.41	0.43	0.45	mA
				f_{CPU} = 1 MHz	0.35	0.41	0.44	0.45	0.48	
				f_{CPU} = 4 MHz	0.42	0.51	0.52	0.54	0.58	
				f_{CPU} = 8 MHz	0.52	0.57	0.58	0.59	0.62	
				f_{CPU} = 16 MHz	0.68	0.76	0.79	0.82 (7)	0.85 (7)	
			HSE external clock (f_{CPU}=f_{HSE}) (6)	f_{CPU} = 125 kHz	0.032	0.056	0.068	0.072	0.093	
				f_{CPU} = 1 MHz	0.078	0.121	0.144	0.163	0.197	
				f_{CPU} = 4 MHz	0.218	0.26	0.30	0.36	0.40	
				f_{CPU} = 8 MHz	0.40	0.52	0.57	0.62	0.66	
				f_{CPU} = 16 MHz	0.760	1.01	1.05	1.09 (7)	1.16 (7)	
			LSI	f_{CPU} = f_{LSI}	0.035	0.044	0.046	0.049	0.054	
			LSE(8) external clock (32.768 kHz)	f_{CPU} = f_{LSE}	0.032	0.036	0.038	0.044	0.051	

HSE crystal/ceramic resonator oscillator

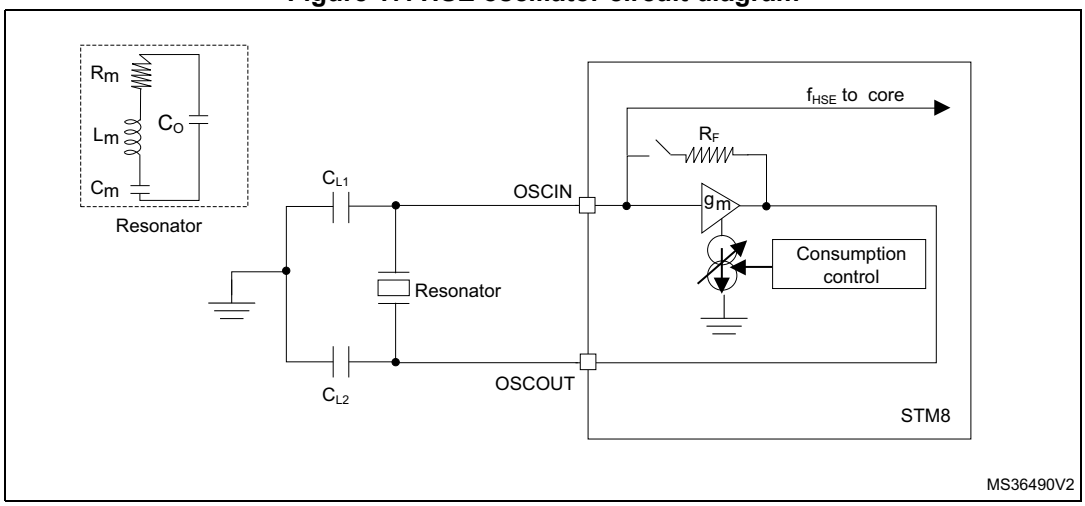
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 31. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High speed external oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$C^{(1)}$	Recommended load capacitance (2)	-	-	20	-	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} =16 MHz	-	-	2.5 (startup) 0.46 (stabilized)(3)	
g_m	Oscillator transconductance	-	3.5(3)	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data guaranteed by design.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 17. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Motional resistance (see crystal specification), L_m: Motional inductance (see crystal specification),
C_m: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification),
C_{L1}=C_{L2}=C: Grounded external capacitance
$g_m >> g_{mcrit}$

LSE crystal/ceramic resonator oscillator

The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 32. LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	ΔV = 200 mV	-	1.2	-	MΩ
C(1)	Recommended load capacitance (2)	-	-	8	-	pF
$I_{DD(LSE)}$	LSE oscillator power consumption	-	-	-	1.4(3)	µA
		V_{DD} = 1.8 V	-	450	-	nA
		V_{DD} = 3 V	-	600	-	
		V_{DD} = 3.6 V	-	750	-	
g_m	Oscillator transconductance	-	3(3)	-	-	µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	s

1. C=C_{L1}=C_{L2} is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details.
3. Data guaranteed by design.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 24*).

Figure 21. Typical V_{IL} and V_{IH} vs V_{DD} (high sink I/Os)

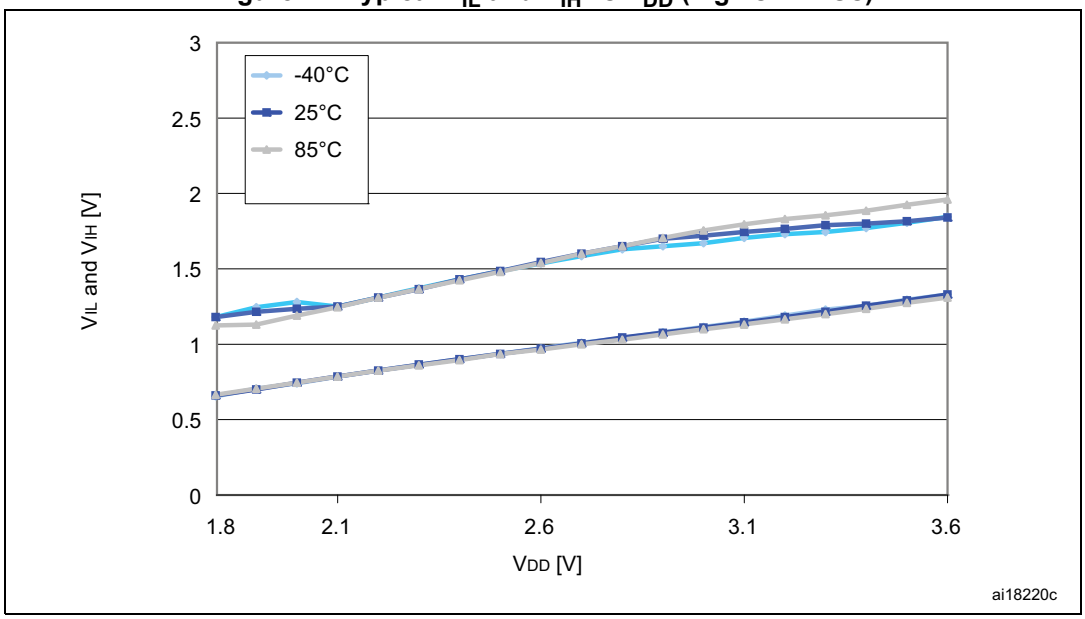
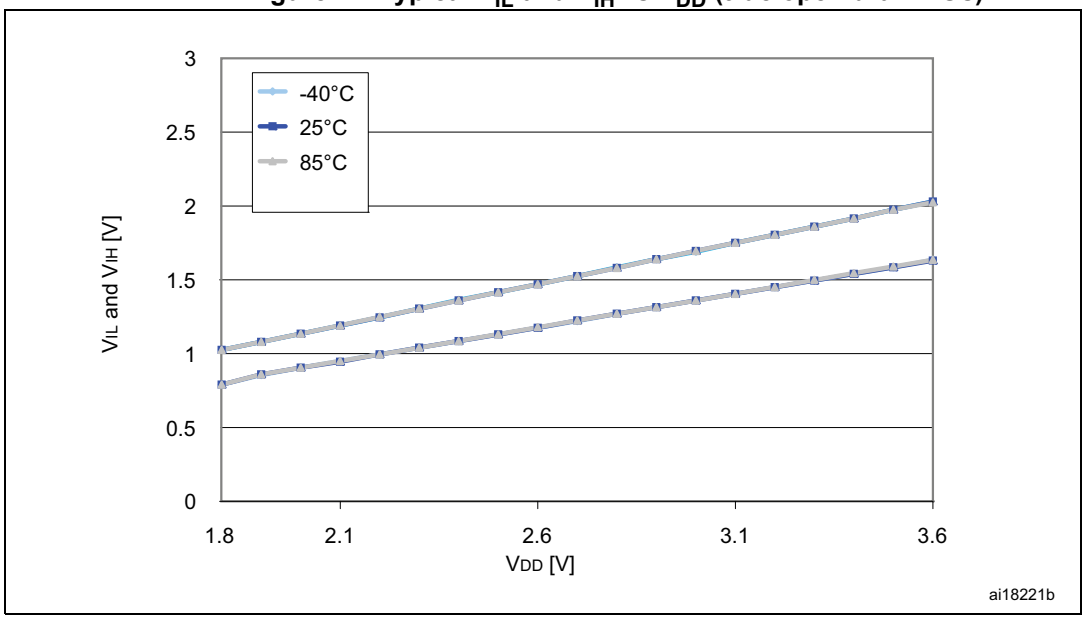


Figure 22. Typical V_{IL} and V_{IH} vs V_{DD} (true open drain I/Os)



9.3.13 12-bit DAC characteristics

In the following table, data is guaranteed by design, not tested in production.

Table 50. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	-	1.8	-	V_{DDA}	
I_{VREF}	Current consumption on V_{REF+} supply	V_{REF+} = 3.3 V, no load, middle code (0x800)	-	130	220	µA
		V_{REF+} = 3.3 V, no load, worst code (0x000)	-	220	350	
I_{VDDA}	Current consumption on V_{DDA} supply	V_{DDA} = 3.3 V, no load, middle code (0x800)	-	210	320	
		V_{DDA} = 3.3 V, no load, worst code (0x000)	-	320	520	
T_A	Temperature range	-	-40	-	125	°C
R_L	Resistive load(1) (2)	DACOUT buffer ON	5	-	-	kΩ
R_O	Output impedance	DACOUT buffer OFF	-	8	10	kΩ
C_L	Capacitive load(3)	-	-	-	50	pF
DAC_OUT	DAC_OUT voltage(4)	DACOUT buffer ON	0.2	-	V_{DDA}-0.2	V
		DACOUT buffer OFF	0	-	V_{REF+} -1 LSB	V
$t_{settling}$	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches the final value ±1LSB)	R_L ≥5 kΩ, C_L≤ 50 pF	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT (@95%) change when small variation of the input code (from code i to i+1LSB).	R_L ≥ 5 kΩ, C_L ≤50 pF	-		1	Msps
t_{WAKEUP}	Wakeup time from OFF state. Input code between lowest and highest possible codes.	R_L ≥5 kΩ, C_L≤50 pF	-	9	15	µs
PSRR+	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	R_L≥ 5 kΩ, C_L≤50 pF	-	-60	-35	dB

1. Resistive load between DACOUT and GNDA.
2. Output on PF0 (48-pin package only).
3. Capacitive load at DACOUT pin.
4. It gives the output excursion of the DAC.

Figure 38. ADC1 accuracy characteristics

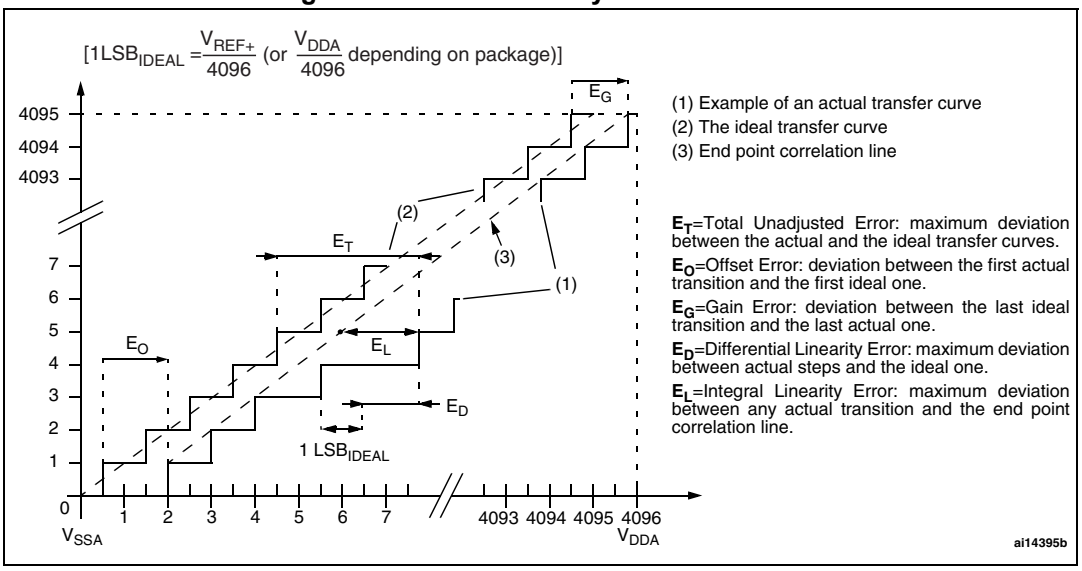
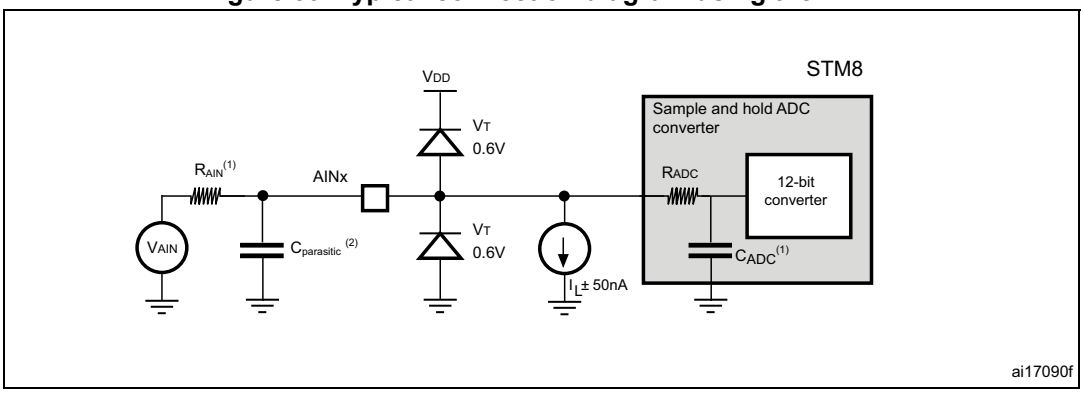


Figure 39. Typical connection diagram using the ADC



1. Refer to *Table 53* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

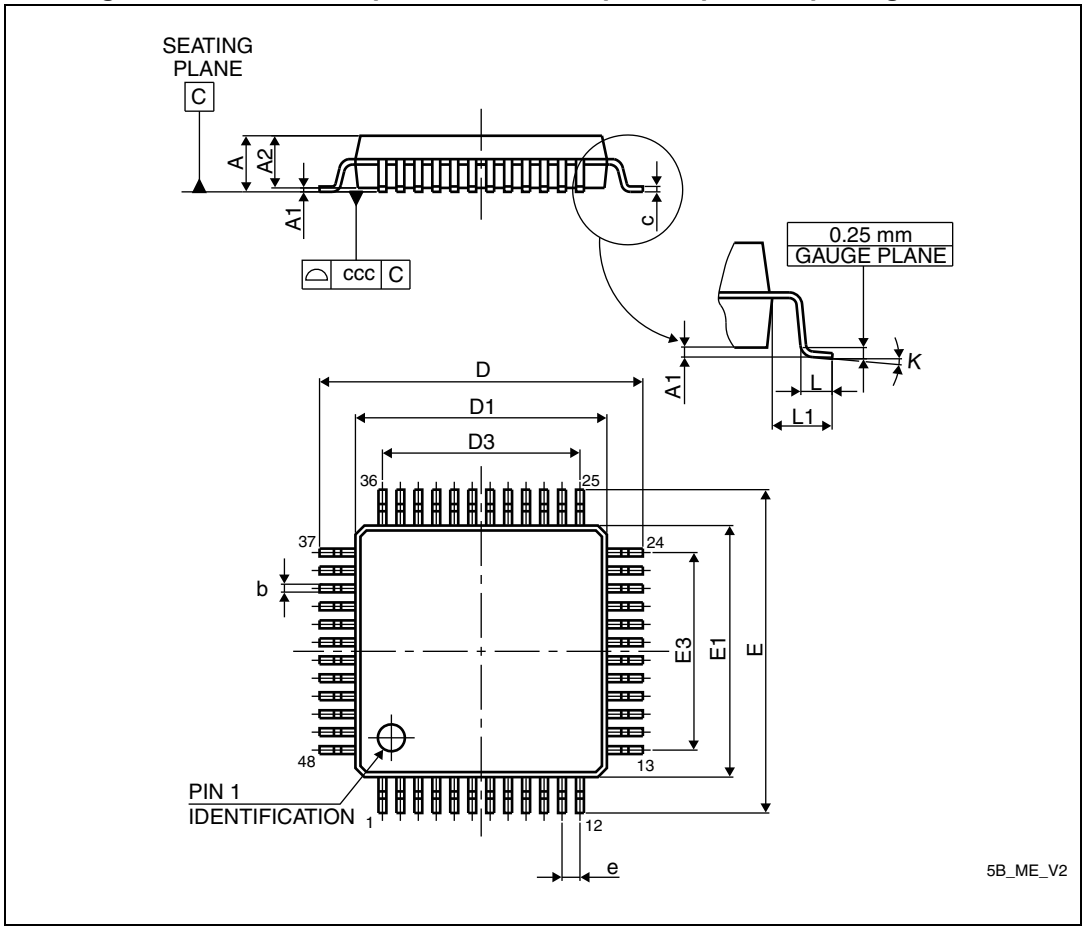
10 Package information

10.1 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

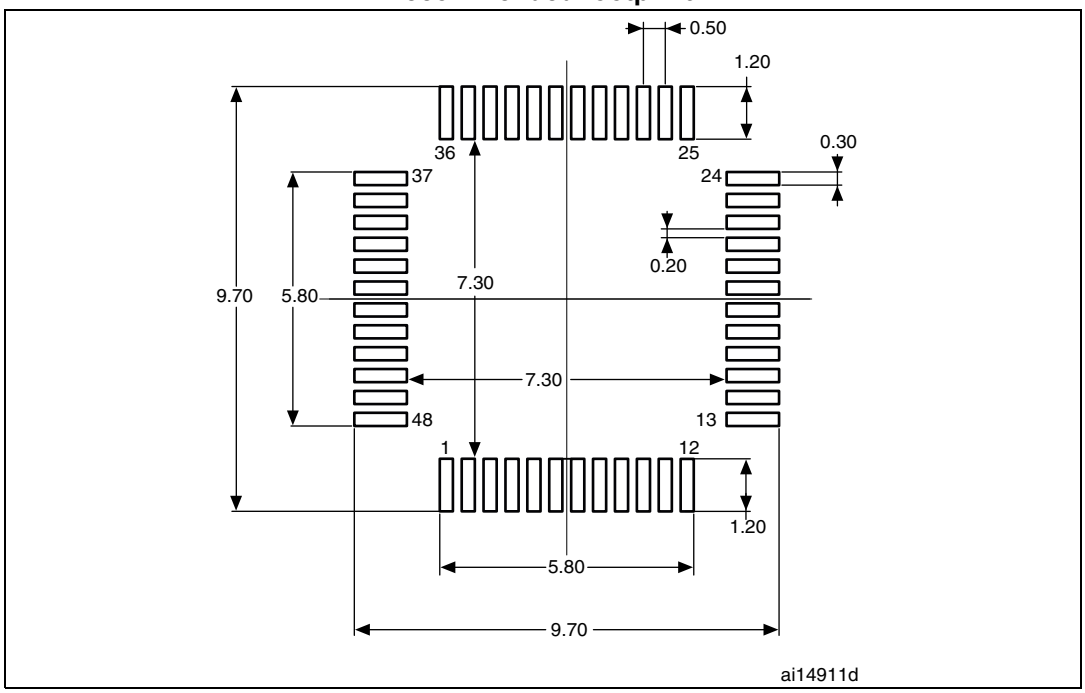
10.2 LQFP48 package information

Figure 43. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Figure 44. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

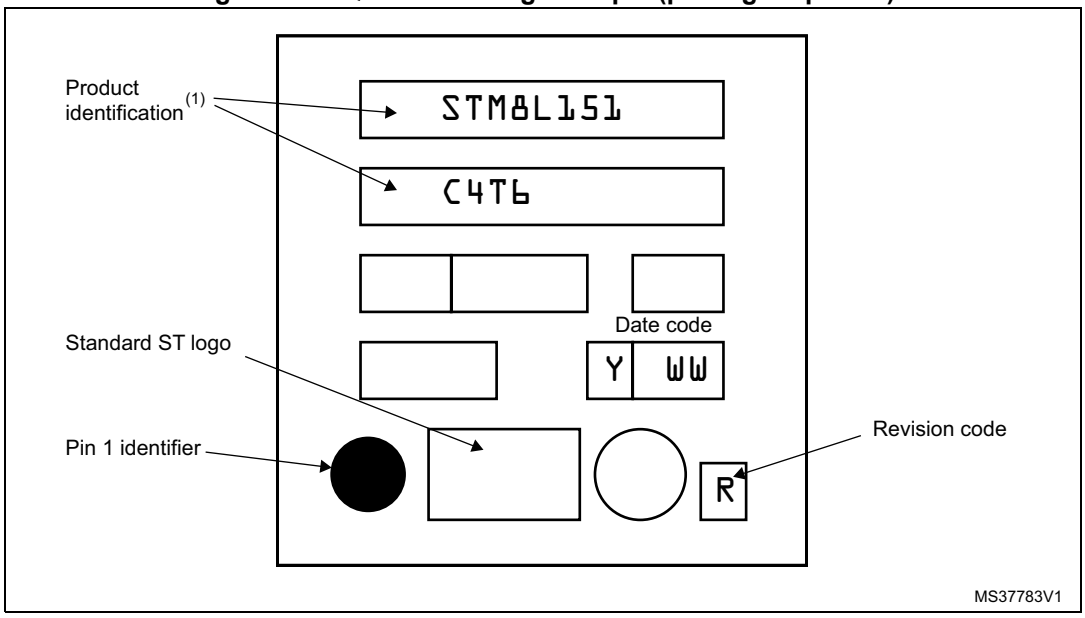


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 45. LQFP48 marking example (package top view)



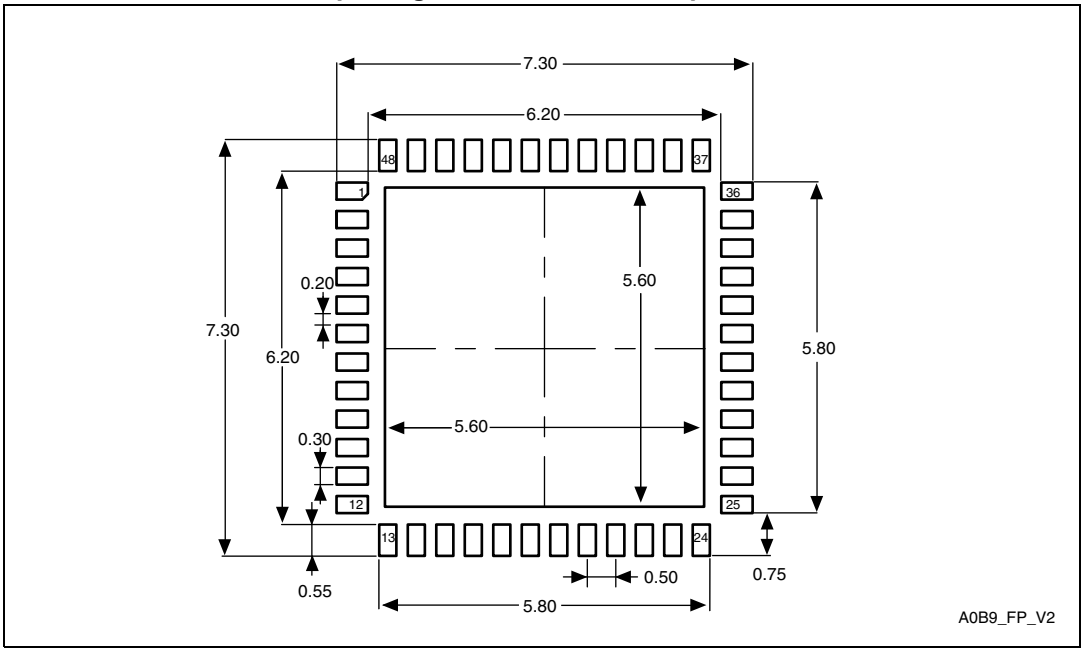
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 63. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

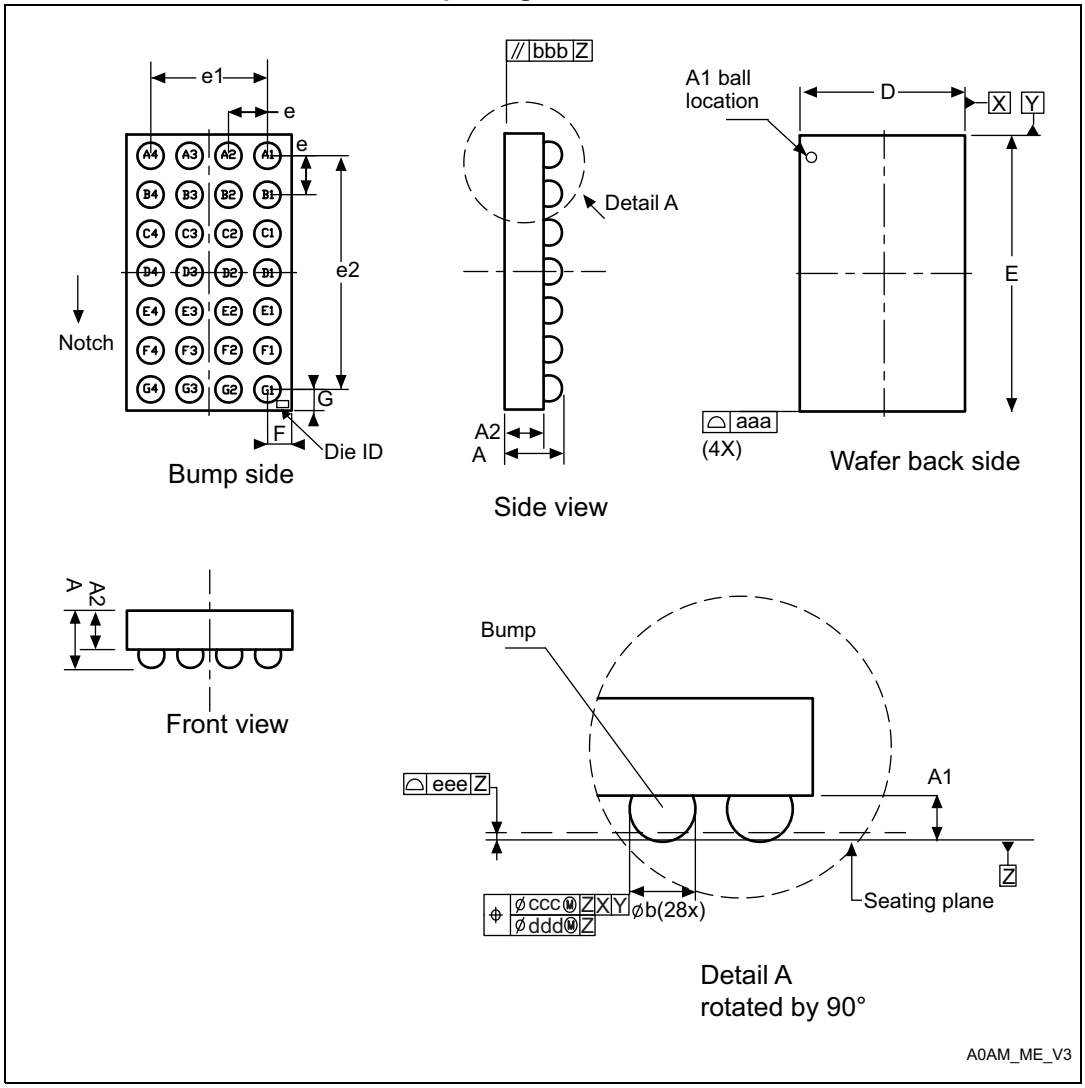
Figure 47. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

10.7 WLCSP28 package information

Figure 58. WLCSP28 - 28-pin, 1.703 x 2.841 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 69. Document revision history (continued)

Date	Revision	Changes
11-Mar-2011	6 cont'd	Modified OPT1 and OPT4 description in *Table: Option byte description.* Updated *Section: Electrical parameters* "standard I/Os" replaced with "high sink I//Os". Updated $R_{HN\ and}$ R_{HN} descriptions in *Table: LCD characteristics.* Added Tape & Reel option to *Figure: Medium density STM8L15x ordering information scheme*.
06-Sep-2011	7	*Features:* updated bullet point concerning capacitive sensing channels. *Section: Low power modes:* updated Wait mode and Halt mode definitions. *Section: Clock management:* added 'kHz' to 32.768 in the 'System clock sources bullet point'. *Section: System configuration controller and routing interface:* replaced last sentence concerning management of charge transfer acquisition sequence. Added *Section: Touchsensing* *Section Development support:* updated the *Bootloader.* *Table: Medium density STM8L15x pin description:* added LQFP32 to second column (same pinout as UFQFPN32); "Timer X - trigger" replaced by "Timer X - external trigger"; added note at the end of this table concerning the slope control of all GPIO pins. *Table: Interrupt mapping:* merged footnotes 1 and 2; updated some of the source blocks and descriptions. *Section: Option bytes*: replaced PM0051 by PM0054 and UM0320 by UM0470. *Table: Option byte description:* replaced the factory default setting (0xAA) for OPT0. *NRST pin:* updated text above the *Figure*; updated *Figure: Recommended NRST pin configuration*. *Table: TS characteristics:* removed typ and max values for the parameter T_{S_TEMP}; added min value for same. *Table: Comparator 1 characteristics:* added typ value for 'Comparator offset error'; added footnote *1.* *Table: Comparator 2 characteristics:* updated t_{START}, t_{dslow}, t_{dfast}, V_{offset}, I_{COMP2}; added footnotes *1.* and *3.* *Table: DAC characteristics:* updated max value for DAC_OUT voltage (DACOUT buffer ON). *Section: 12-bit ADC1 characteristics:* updated. Replaced *Figure: UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline* and *Figure: UFQFPN48 7 x 7 mm recommended footprint (dimensions in mm)*. *Figure: Medium density STM8L15x ordering information scheme*: removed 'TR = Tape & Reel".