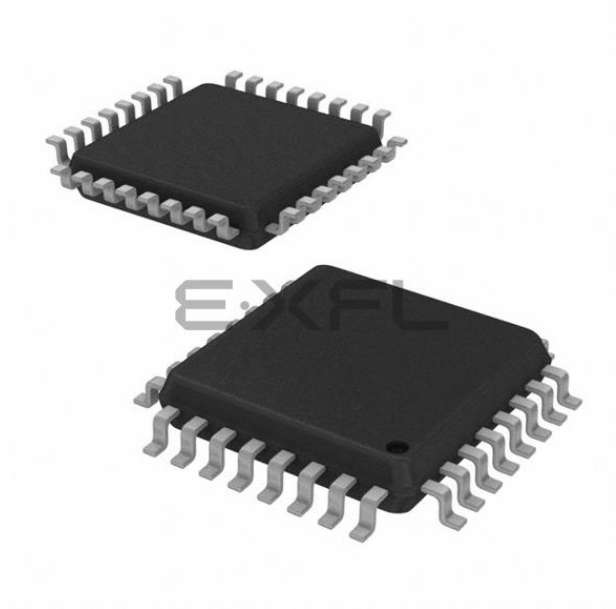

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Applications of "Embedded - Microcontrollers"

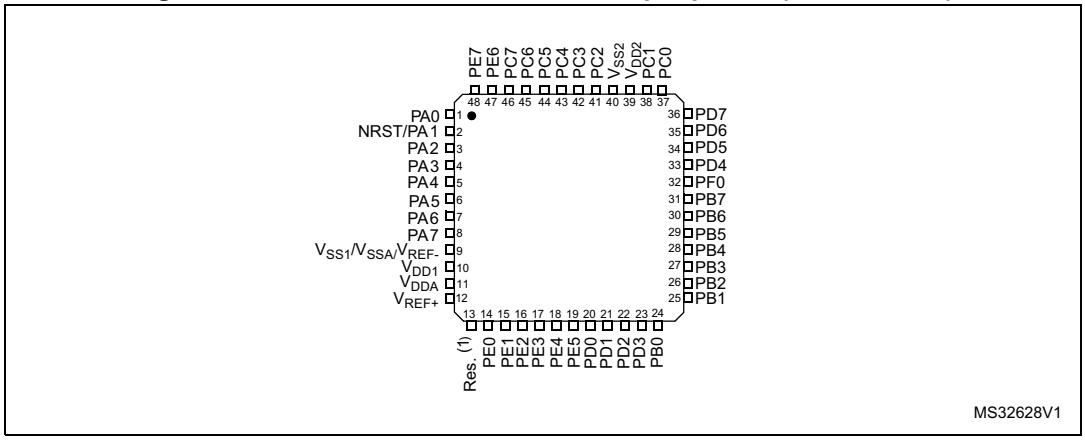
Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	30
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151k4t6tr

Contents

List of tables

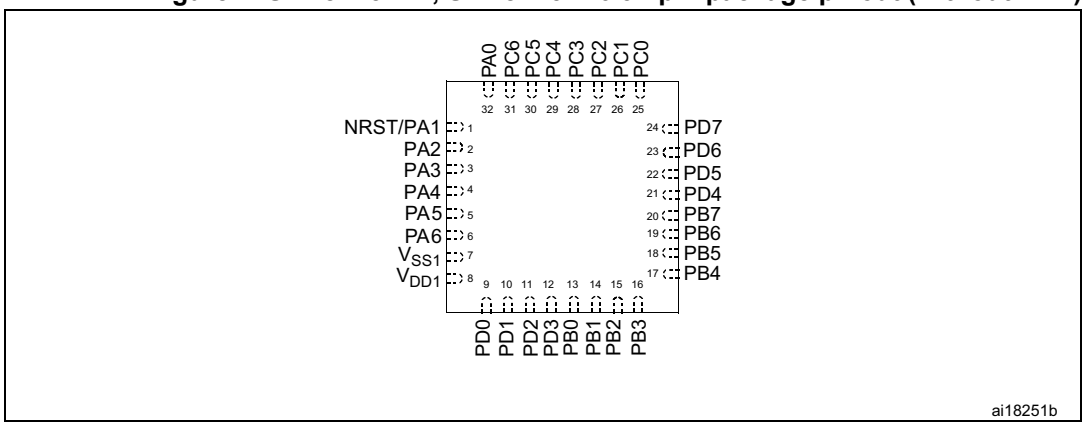
4 Pinout and pin description

Figure 3. STM8L151C4, STM8L151C6 48-pin pinout (without LCD)



1. Reserved. Must be tied to V_{DD}.

Figure 4. STM8L151K4, STM8L151K6 32-pin package pinout (without LCD)



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.

Figure 5. STM8L151Gx UFQFPN28 package pinout

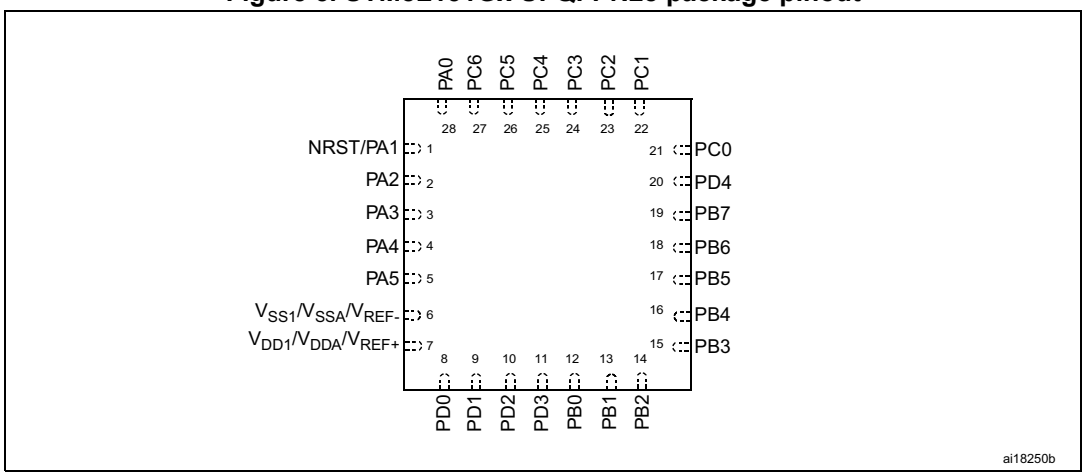


Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	16	-	-	PB3/*[TIM2_ETR]*(4)/ TIM1_CH2N/LCD_SEG13(2)/ADC1_IN15/ COMP1_INP	I/O	TT(3)	**X**	X	X	HS	X	X	**Port B3**	*[Timer 2 - external trigger]* / Timer 1 inverted channel 2 / LCD segment 13 / ADC1_IN15 / Comparator 1 positive input
-	-	15	E2	PB3/*[TIM2_ETR]*(4)/ TIM1_CH1N/ LCD_SEG13(2)/ ADC1_IN15/RTC_ALARM /COMP1_INP	I/O	TT(3)	**X**	X	X	HS	X	X	**Port B3**	*[Timer 2 - external trigger]* / Timer 1 inverted channel 1/ LCD segment 13 / ADC1_IN15 / RTC alarm/ Comparator 1 positive input
28	-	-	-	PB4(6)/*[SPI1_NSS]*(4)/ LCD_SEG14(2)/ ADC1_IN14/COMP1_INP	I/O	TT(3)	**X**(6)	X(6)	X	HS	X	X	**Port B4**	*[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14 / Comparator 1 positive input
-	17	16	D2	PB4(6)/*[SPI1_NSS]*(4)/ LCD_SEG14(2)/ ADC1_IN14/ COMP1_INP/DAC_OUT	I/O	TT(3)	**X**(6)	X(6)	X	HS	X	X	**Port B4**	*[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14 / DAC output / Comparator 1 positive input
29	-	-	-	PB5/*[SPI1_SCK]*(4)/ LCD_SEG15(2)/ ADC1_IN13/COMP1_INP	I/O	TT(3)	**X**	X	X	HS	X	X	**Port B5**	*[SPI1 clock]* / LCD segment 15 / ADC1_IN13 / Comparator 1 positive input
-	18	17	D1	PB5/*[SPI1_SCK]*(4)/ LCD_SEG15(2)/ ADC1_IN13/DAC_OUT/ COMP1_INP	I/O	TT(3)	**X**	X	X	HS	X	X	**Port B5**	*[SPI1 clock]* / LCD segment 15 / ADC1_IN13 / DAC output/ Comparator 1 positive input

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

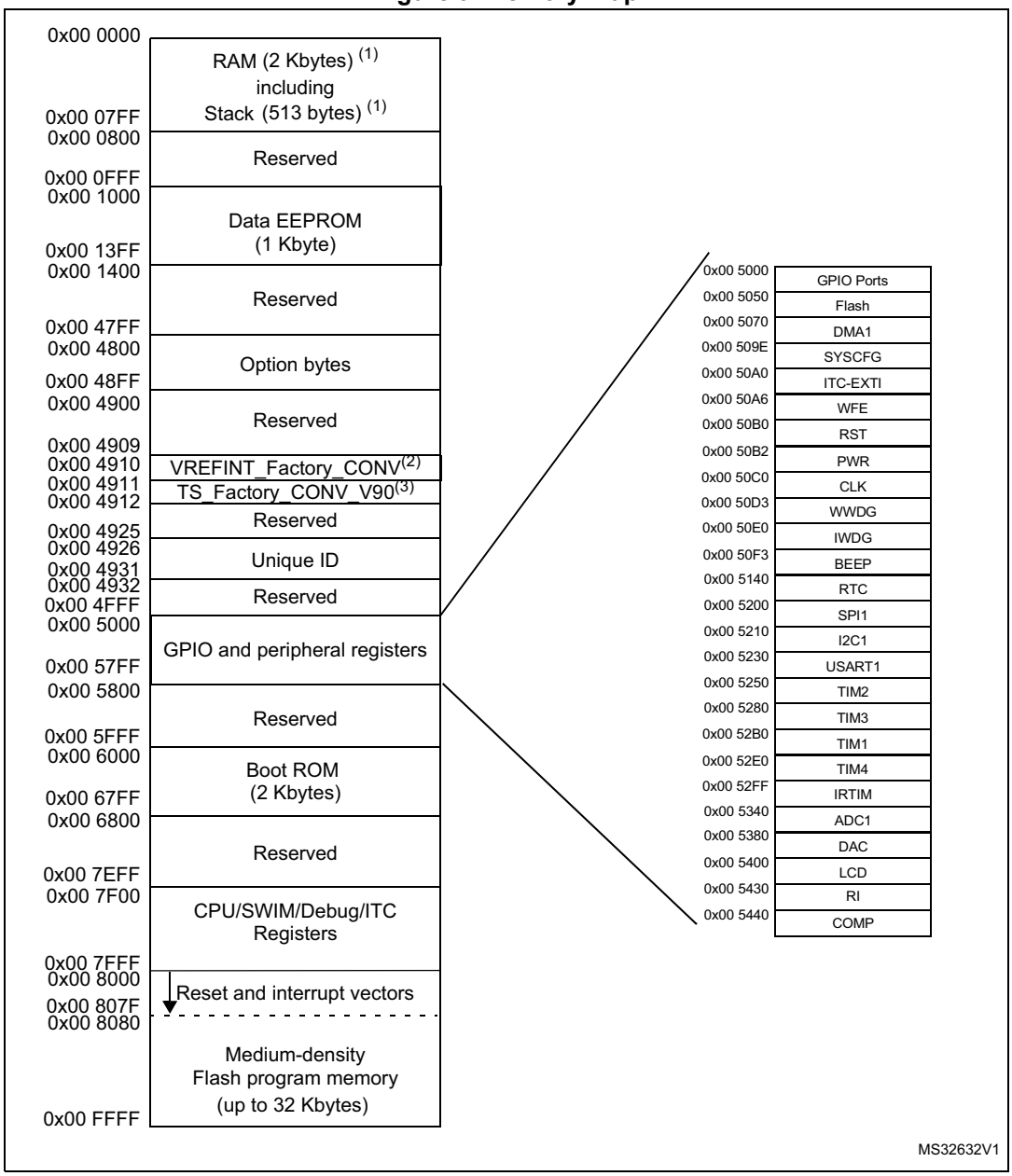
Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	9	G2	PD1/TIM1_CH3/[*TIM3_ETR*](4)/LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D1**	Timer 1 channel 3 / *[Timer 3 - external trigger]* / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input
22	11	10	E4	PD2/TIM1_CH1 /LCD_SEG8(2)/ ADC1_IN20/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D2**	Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20 / Comparator 1 positive input
23	12	-	-	PD3/ TIM1_ETR/ LCD_SEG9(2)/ADC1_IN19/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D3**	Timer 1 - external trigger / LCD segment 9 / ADC1_IN19 / Comparator 1 positive input
-	-	11	F3	PD3/ TIM1_ETR/ LCD_SEG9(2)/ ADC1_IN19/TIM1_BKIN/ COMP1_INP/ RTC_CALIB	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D3**	Timer 1 - external trigger / LCD segment 9 / ADC1_IN19 / Timer 1 break input / RTC calibration / Comparator 1 positive input
33	21	20	C1	PD4/TIM1_CH2 /LCD_SEG18(2)/ ADC1_IN10/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/ Comparator 1 positive input
34	22	-	-	PD5/TIM1_CH3 /LCD_SEG19(2)/ ADC1_IN9/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D5**	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ Comparator 1 positive input
35	23	-	-	PD6/TIM1_BKIN /LCD_SEG20(2)/ ADC1_IN8/RTC_CALIB/ /VREFINT/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D6**	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration / Internal voltage reference output / Comparator 1 positive input

5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 9*.

Figure 9. Memory map



1. *Table 6* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. The VREFINT_Factory_CONV byte represents the LSB of the V_{REFINT} 12-bit ADC conversion result. The MSB have a fixed value: 0x6.
3. The TS_Factory_CONV_V90 byte represents the LSB of the V_{90} 12-bit ADC conversion result. The MSB

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5055 to 0x00 506F	Reserved area (27 bytes)			
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 bytes)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00
0x00 507D to 0x00 507E		Reserved area (2 bytes)		
0x00 507F		DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083		DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50D0 to 0x00 50D2	Reserved area (3 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 bytes)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to 0x00 513F	Reserved area (76 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5430	RI	Reserved area (1 byte)		0x00
0x00 5431		RI_ICR1	Timer input capture routing register 1	0x00
0x00 5432		RI_ICR2	Timer input capture routing register 2	0x00
0x00 5433		RI_IOIR1	I/O input register 1	undefined
0x00 5434		RI_IOIR2	I/O input register 2	undefined
0x00 5435		RI_IOIR3	I/O input register 3	undefined
0x00 5436		RI_IOCMR1	I/O control mode register 1	0x00
0x00 5437		RI_IOCMR2	I/O control mode register 2	0x00
0x00 5438		RI_IOCMR3	I/O control mode register 3	0x00
0x00 5439		RI_IOSR1	I/O switch register 1	0x00
0x00 543A		RI_IOSR2	I/O switch register 2	0x00
0x00 543B		RI_IOSR3	I/O switch register 3	0x00
0x00 543C		RI_IOGCR	I/O group control register	0x3F
0x00 543D		RI_ASCR1	Analog switch register 1	0x00
0x00 543E		RI_ASCR2	Analog switch register 2	0x00
0x00 543F		RI_RCR	Resistor control register 1	0x00
0x00 5440	COMP	COMP_CSR1	Comparator control and status register 1	0x00
0x00 5441		COMP_CSR2	Comparator control and status register 2	0x00
0x00 5442		COMP_CSR3	Comparator control and status register 3	0x00
0x00 5443		COMP_CSR4	Comparator control and status register 4	0x00
0x00 5444		COMP_CSR5	Comparator control and status register 5	0x00

1. These registers are not impacted by a system reset. They are reset at power-on.

Table 13. Option byte description (continued)

Option byte No.	Option description
OPT5	**BOR_ON**: 0: Brownout reset off 1: Brownout reset on
	BOR_TH[3:1]: Brownout reset thresholds. Refer to *Table 23* for details on the thresholds according to the value of BOR_TH bits.
OPTBL	**OPTBL[15:0]**: This option is checked by the boot ROM code after reset. Depending on content of addresses 00 480B, 00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 bootloader user manual for more details.

Table 24. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions (1)			Typ	Max	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSE external clock (32.768 kHz) (6)	LCD OFF(7)	T_A = -40 °C to 25 °C	0.5	1.2	µA
				T_A = 55 °C	0.62	1.4	
				T_A = 85 °C	0.88	2.1	
				T_A = 105 °C	2.1	4.85	
				T_A = 125 °C	4.8	11	
			LCD ON (static duty/ external V_{LCD}) (3)	T_A = -40 °C to 25 °C	0.85	1.9	
				T_A = 55 °C	0.95	2.2	
				T_A = 85 °C	1.3	3.2	
				T_A = 105 °C	2.3	5.3	
				T_A = 125 °C	5.0	12	
			LCD ON (1/4 duty/ external V_{LCD}) (4)	T_A = -40 °C to 25 °C	1.5	2.5	
				T_A = 55 °C	1.6	3.8	
				T_A = 85 °C	1.8	4.2	
				T_A = 105 °C	2.9	7.0	
				T_A = 125 °C	5.7	14	
			LCD ON (1/4 duty/ internal V_{LCD}) (5)	T_A = -40 °C to 25 °C	3.4	7.6	
				T_A = 55 °C	3.7	8.3	
				T_A = 85 °C	3.9	9.2	
				T_A = 105 °C	5.0	14.5	
				T_A = 125 °C	6.3	15.2	
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode (using HSI)	-		-	2.4	-	mA
$t_{WU\_HSI(AH)}$ (8)(9)	Wakeup time from Active-halt mode to Run mode (using HSI)	-		-	4.7	7	µs
$t_{WU\_LSI(AH)}$ (8) (9)	Wakeup time from Active-halt mode to Run mode (using LSI)	-		-	150	-	µs

1. No floating I/O, unless otherwise specified.
2. RTC enabled. Clock source = LSI
3. RTC enabled, LCD enabled with external V_{LCD} = 3 V, static duty, division ratio = 256, all pixels active, no LCD connected.
4. RTC enabled, LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. LCD enabled with internal LCD booster V_{LCD} = 3 V, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
6. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*.
7. RTC enabled. Clock source = LSE.
8. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.
9. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

Table 25. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal

Symbol	Parameter	Condition(1)		Typ	Unit
$I_{DD(AH)}$ (2)	Supply current in Active-halt mode	V_{DD} = 1.8 V	LSE	1.15	µA
			LSE/32(3)	1.05	
		V_{DD} = 3 V	LSE	1.30	
			LSE/32(3)	1.20	
		V_{DD} = 3.6 V	LSE	1.45	
			LSE/32(3)	1.35	

1. No floating I/O, unless otherwise specified.
2. Based on measurements on bench with 32.768 kHz external crystal oscillator.
3. RTC clock is LSE divided by 32.

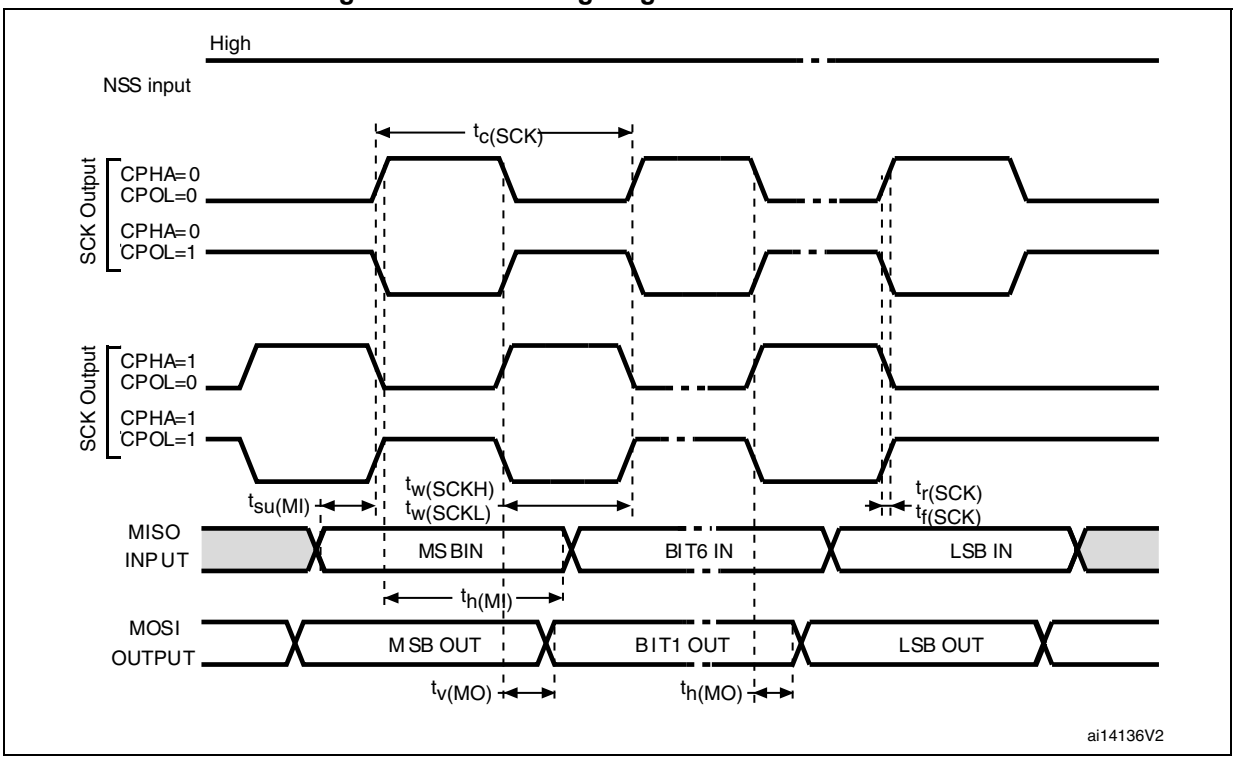
In the following table, data is based on characterization results, unless otherwise specified.

Table 26. Total current consumption and timing in Halt mode at V_{DD} = 1.65 to 3.6 V

Symbol	Parameter	Condition(1)	Typ	Max	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (Ultra-low-power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	350	1400(2)	nA
		T_A = 55 °C	580	2000	
		T_A = 85 °C	1160	2800(2)	
		T_A = 105 °C	2560	6700(2)	
		T_A = 125 °C	4.4	13(2)	µA
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)	-	2.4	-	mA
$t_{WU\_HSI(Halt)}$ (3)(4)	Wakeup time from Halt to Run mode (using HSI)	-	4.7	7	µs
$t_{WU\_LSI(Halt)}$ (3)(4)	Wakeup time from Halt mode to Run mode (using LSI)	-	150	-	µs

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. Tested in production.
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.
4. Wakeup time until start of interrupt vector fetch.
The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.

Figure 36. SPI1 timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

I²C - Inter IC control interface

Subject to general operating conditions for V_{DD}, f_{SYSCLK}, and T_A unless otherwise specified.

The STM8L I²C interface (I2C1) meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 44. I2C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max (2)	Min (2)	Max (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400		400	pF

1. f_{SYSCLK} must be at least equal to 8 MHz to achieve max fast I²C speed (400 kHz).
2. Data based on standard I²C protocol requirement, not tested in production.

Note: For speeds around 200 kHz, the achieved speed can have a± 5% tolerance
For other speed ranges, the achieved speed can have a± 2% tolerance
The above variations depend on the accuracy of the external components used.

Figure 40. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

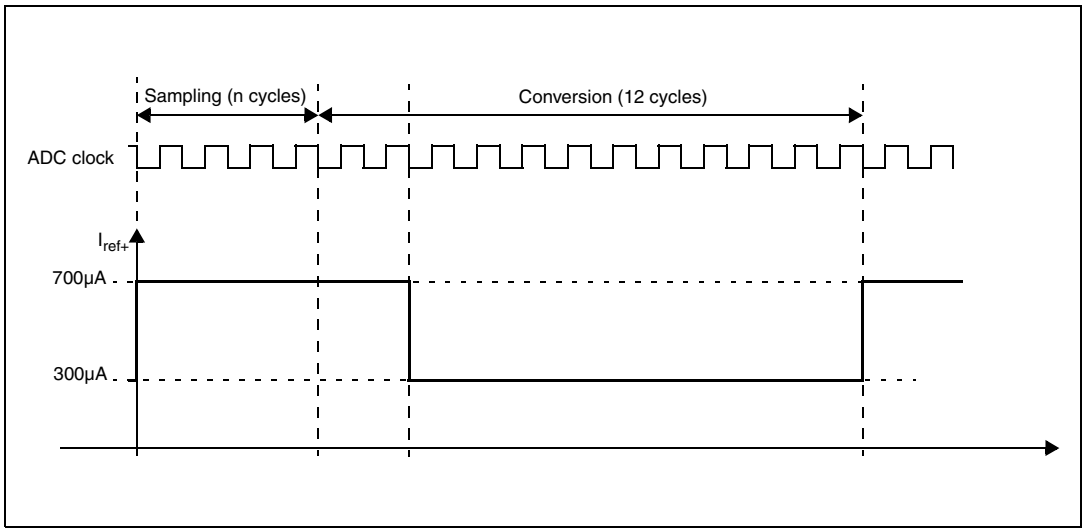


Table 57. R_{AIN} max for f_{ADC} = 16 MHz(1)

Ts (cycles)	Ts (µs)	R_{AIN} max (kohm)			
		Slow channels		Fast channels	
		2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA} < 3.3 V	1.8 V < V_{DDA} < 2.4 V
4	0.25	Not allowed	Not allowed	0.7	Not allowed
9	0.5625	0.8	Not allowed	2.0	1.0
16	1	2.0	0.8	4.0	3.0
24	1.5	3.0	1.8	6.0	4.5
48	3	6.8	4.0	15.0	10.0
96	6	15.0	10.0	30.0	20.0
192	12	32.0	25.0	50.0	40.0
384	24	50.0	50.0	50.0	50.0

1. Guaranteed by design.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 41* or *Figure 42*, depending on whether V_{REF+} is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

Table 59. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. 16 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP32 conforming to IEC61967-2	0.1 MHz to 30 MHz	-3	dBµV
			30 MHz to 130 MHz	9	
			130 MHz to 1 GHz	4	
			SAE EMI Level	2	-

1. Not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and charge device model. This test conforms to the JESD22-A114A/A115A standard.

Table 60. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		500	

1. Data based on characterization results.

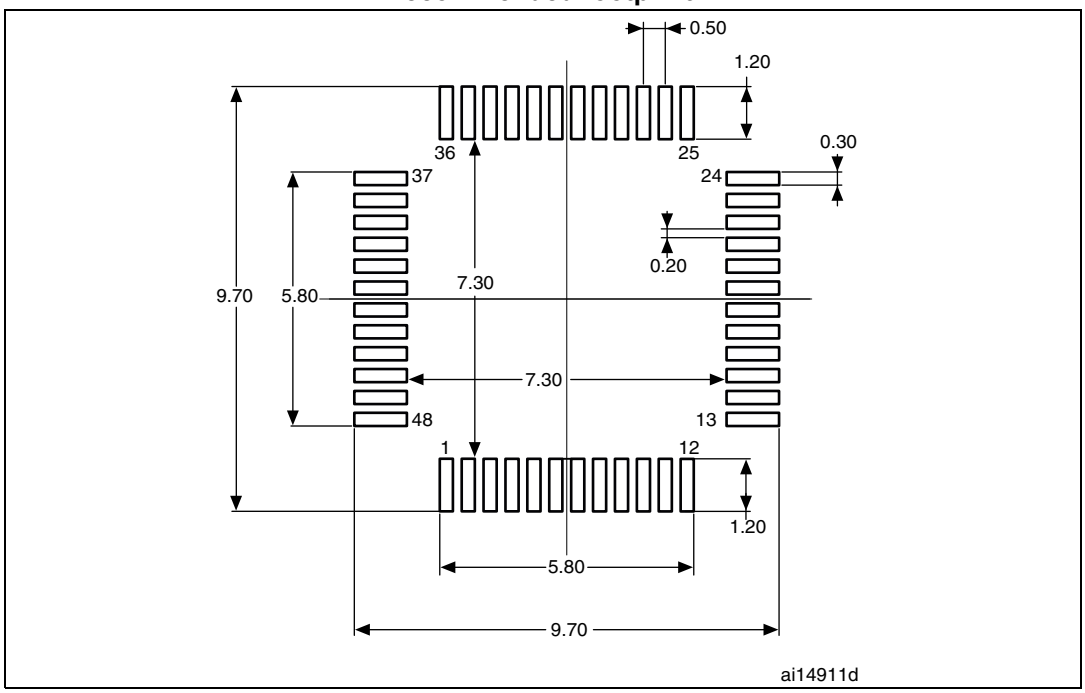
Static latch-up

- **LU**: 3 complementary static tests are required on 6 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 61. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

Figure 44. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

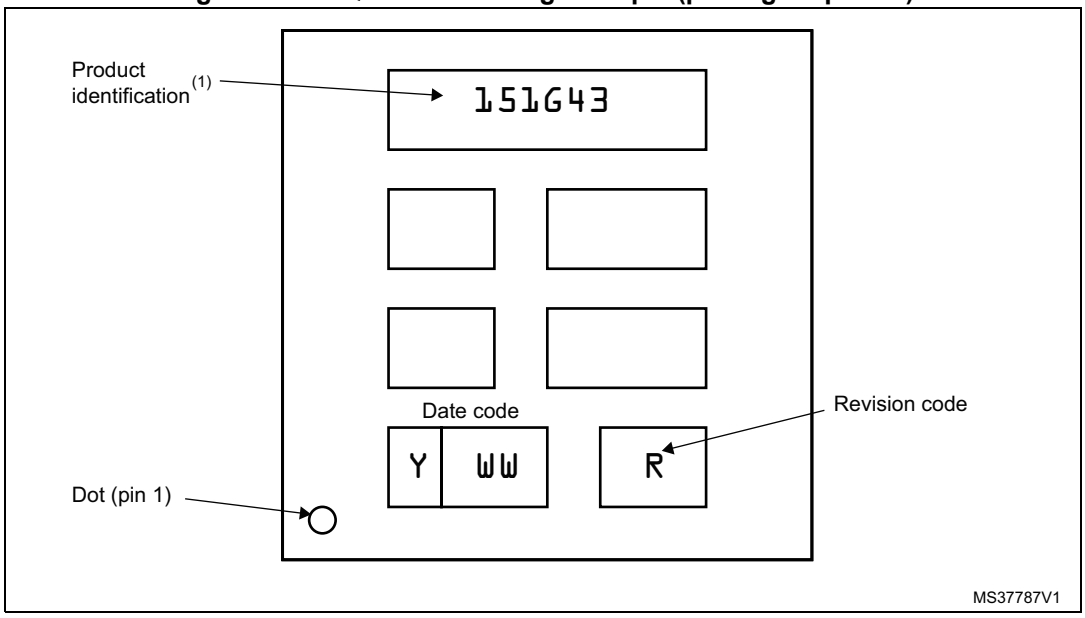


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

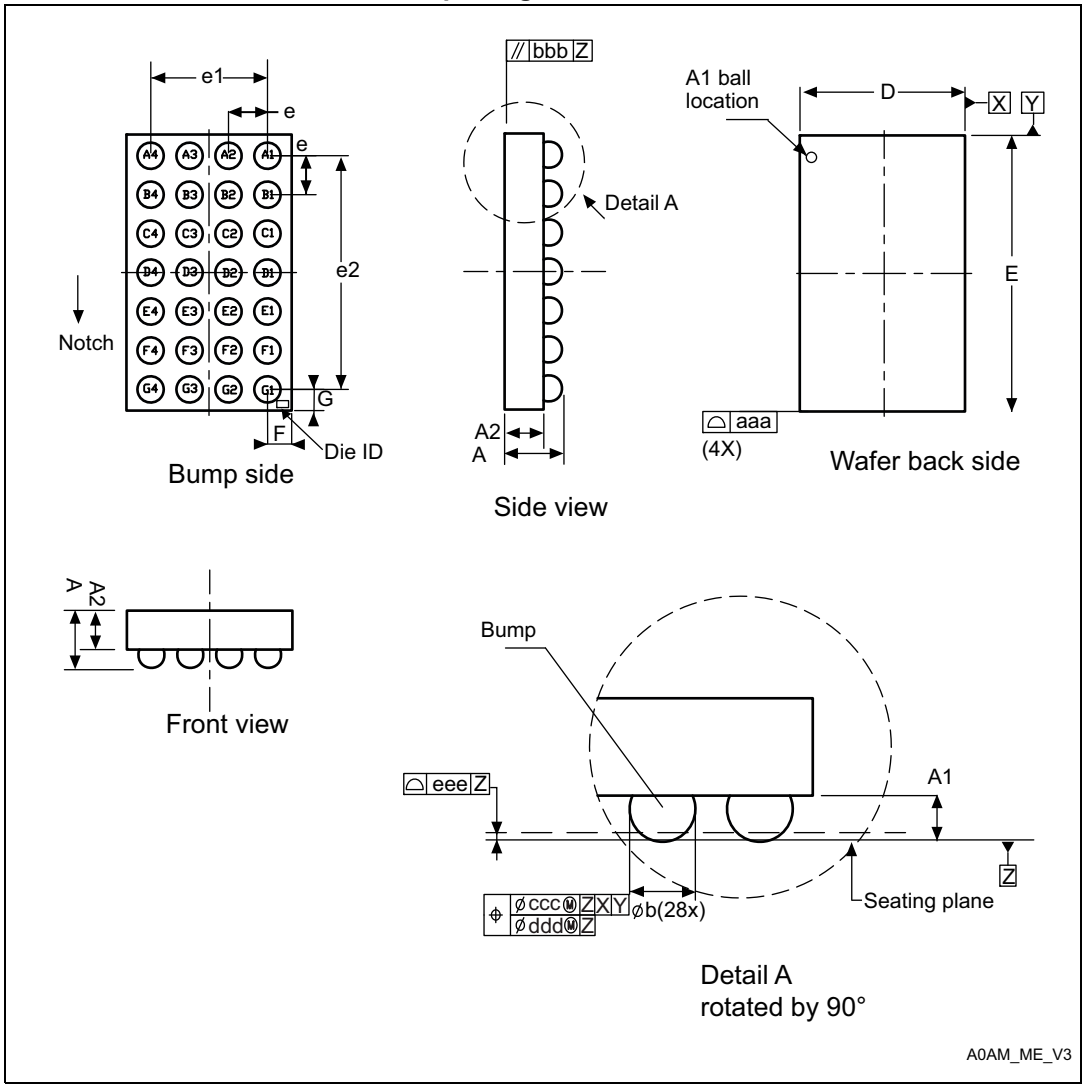
Figure 57. UFQFPN28 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

10.7 WLCSP28 package information

Figure 58. WLCSP28 - 28-pin, 1.703 x 2.841 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.