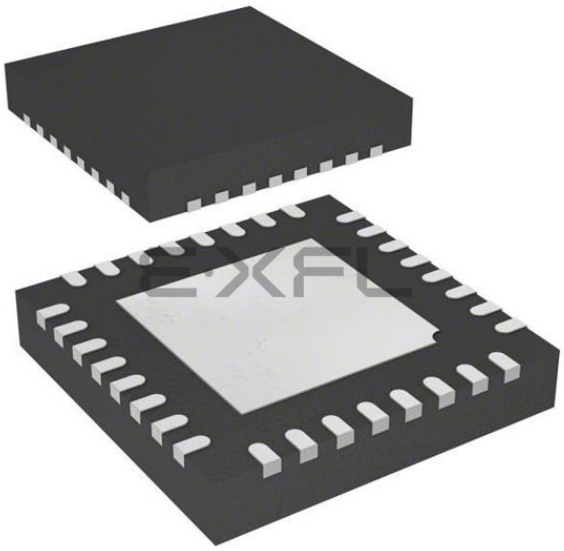

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	30
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151k4u6tr

List of tables

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1}; V_{DD1} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD1} pins, the corresponding ground pin is V_{SS1}.
- $V_{SSA;}$ V_{DDA} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{SS2}; V_{DD2} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for I/Os. V_{DD2} and V_{SS2} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{REF+}; V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.
- V_{REF+} (for DAC): external voltage reference for DAC must be provided externally through V_{REF+}.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min value at power down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains under reset when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

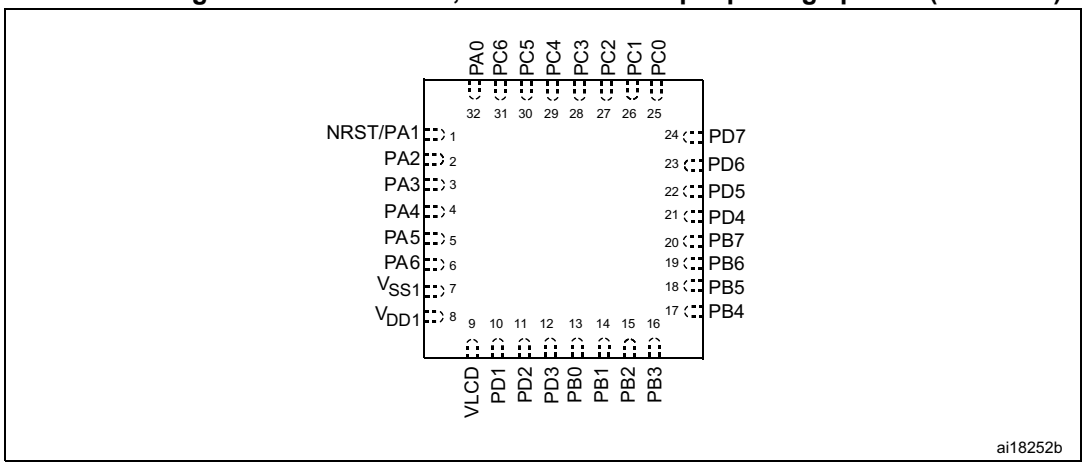
The medium-density STM8L151x4/6 and STM8L152x4/6 embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

Figure 8. STM8L152K4, STM8L152K6 32-pin package pinout (with LCD)



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	5	5	D4	PA5/TIM3_BKIN/ *[TIM3_ETR]*(4)/ LCD_COM1(2)/ADC1_IN1/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input / *[Timer 3 - external trigger]* / LCD_COM 1 / ADC1 input 1 / Comparator 1 positive input
7	6	-	-	PA6/*[ADC1_TRIG]*(4)/ LCD_COM2(2)/ADC1_IN0/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port A6**	*[ADC1 - trigger]* / LCD_COM2 / ADC1 input 0 / Comparator 1 positive input
8	-	-	-	PA7/LCD_SEG0(2)(5)	I/O	FT	**X**	X	X	HS	X	X	**Port A7**	LCD segment 0
24	13	12	E3	PB0(6)/TIM2_CH1/ LCD_SEG10(2)/ ADC1_IN18/COMP1_INP	I/O	TT (3)	**X**(6)	X(6)	X	HS	X	X	**Port B0**	Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18 / Comparator 1 positive input
25	14	13	G1	PB1/TIM3_CH1/ LCD_SEG11(2)/ ADC1_IN17/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B1**	Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17 / Comparator 1 positive input
26	15	14	F2	PB2/ TIM2_CH2/ LCD_SEG12(2)/ ADC1_IN16/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B2**	Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16/ Comparator 1 positive input
27	-	-	-	PB3/TIM2_ETR/ LCD_SEG13(2)/ ADC1_IN15/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B3**	Timer 2 - external trigger / LCD segment 13 /ADC1_IN15 / Comparator 1 positive input

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
44	30	26	A3	PC5/OSC32_IN /*[SPI1_NSS]*(4)/ *[USART1_TX]*(4)	I/O		**X**	X	X	HS	X	X	**Port C5**	LSE oscillator input / *[SPI1 master/slave select] / [USART1 transmit]*
45	31	27	B3	PC6/OSC32_OUT/ *[SPI1_SCK]*(4)/ *[USART1_RX]*(4)	I/O		**X**	X	X	HS	X	X	**Port C6**	LSE oscillator output / *[SPI1 clock] / [USART1 receive]*
46	-	-	-	PC7/LCD_SEG25(2)/ ADC1_IN3/COMP2_INM/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C7**	LCD segment 25 /ADC1_IN3/ Comparator negative input / Comparator 1 positive input
20	-	8	G3	PD0/TIM3_CH2/ *[ADC1_TRIG]*(4)/ LCD_SEG7(2)/ADC1_IN22/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / LCD segment 7 / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input
-	9	-	-	PD0/TIM3_CH2/ *[ADC1_TRIG]*(4)/ ADC1_IN22/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D0(8)**	Timer 3 - channel 2 / *[ADC1_Trigger]* / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input
21	-	-	-	PD1/TIM3_ETR/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - external trigger / LCD_COM3 / ADC1_IN21 / comparator 2 positive input / Comparator 1 positive input
-	10	-	-	PD1/TIM1_CH3N/[*TIM3_ETR*](4)/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D1**	*[Timer 3 - external trigger]/* TIM1 inverted channel 3 / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
36	24	-	-	PD7/TIM1_CH1N /LCD_SEG21(2)/ ADC1_IN7/RTC_ALARM/ VREFINT/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D7**	Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm / Internal voltage reference output /Comparator 1 positive input
14	-	-	-	PE0(5)/LCD_SEG1(2)	I/O	FT	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1
15	-	-	-	PE1/TIM1_CH2N /LCD_SEG2(2)	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2
16	-	-	-	PE2/TIM1_CH3N /LCD_SEG3(2)	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3
17	-	-	-	PE3/LCD_SEG4(2)	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4
18	-	-	-	PE4/LCD_SEG5(2)	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5
19	-	-	-	PE5/LCD_SEG6(2)/ ADC1_IN23/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23 / Comparator 2 positive input / Comparator 1 positive input
47	-	-	-	PE6/LCD_SEG26(2)/ PVD_IN	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E6**	LCD segment 26/PVD_IN
48	-	-	-	PE7/LCD_SEG27(2)	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E7**	LCD segment 27
32	-	-	-	PF0/ADC1_IN24/ DAC_OUT	I/O	TT (3)	**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC_OUT
13	9	-	-	VLCD(2)	S	-	**-**	-	-	-	-	-	LCD booster external capacitor	
13	-	-	-	Reserved(8)	-	-	**-**	-	-	-	-	-	Reserved. Must be tied to V_{DD}	
10	-	-	-	V_{DD}	S	-	**-**	-	-	-	-	-	Digital power supply	
11	-	-	-	V_{DDA}	S	-	**-**	-	-	-	-	-	Analog supply voltage	
12	-	-	-	V_{REF+}	S	-	**-**	-	-	-	-	-	ADC1 and DAC positive voltage reference	

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 501E to 0x00 5049	Reserved area (28 bytes)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5055 to 0x00 506F	Reserved area (27 bytes)			
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 bytes)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00
0x00 507D to 0x00 507E		Reserved area (2 bytes)		
0x00 507F		DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083		DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	USART1	USART1_SR	USART1 status register	0xC0
0x00 5231		USART1_DR	USART1 data register	undefined
0x00 5232		USART1_BRR1	USART1 baud rate register 1	0x00
0x00 5233		USART1_BRR2	USART1 baud rate register 2	0x00
0x00 5234		USART1_CR1	USART1 control register 1	0x00
0x00 5235		USART1_CR2	USART1 control register 2	0x00
0x00 5236		USART1_CR3	USART1 control register 3	0x00
0x00 5237		USART1_CR4	USART1 control register 4	0x00
0x00 5238		USART1_CR5	USART1 control register 5	0x00
0x00 5239		USART1_GTR	USART1 guard time register	0x00
0x00 523A		USART1_PSCR	USART1 prescaler register	0x00
0x00 523B to 0x00 524F	Reserved area (21 bytes)			

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics is indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

9.1.2 Typical values

Unless otherwise specified, typical data is based on T_A = 25 °C, V_{DD} = 3 V. It is given only as design guidelines and is not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

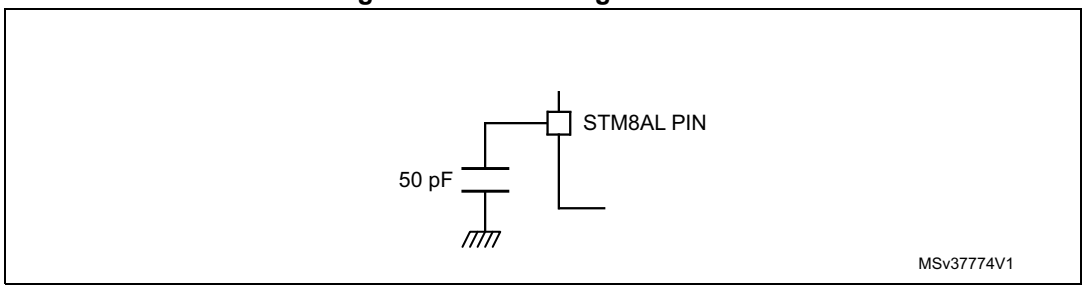
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

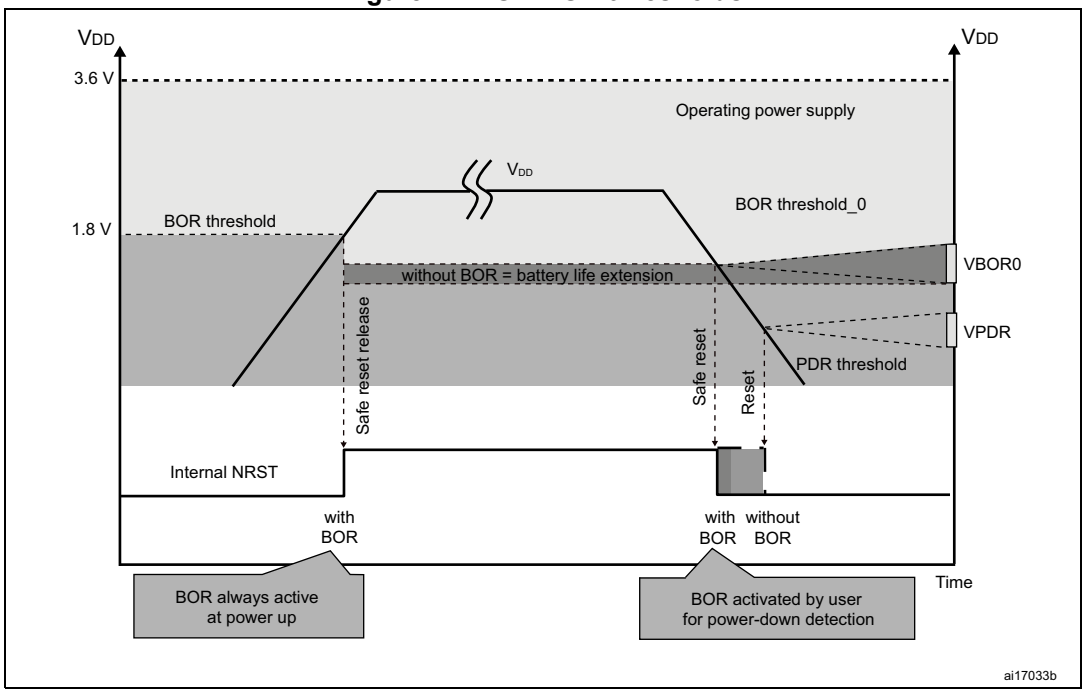
The loading conditions used for pin parameter measurement are shown in *Figure 10*.

Figure 10. Pin loading conditions



1. Data guaranteed by design.
2. Data based on characterization results.

Figure 12. POR/BOR thresholds



9.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

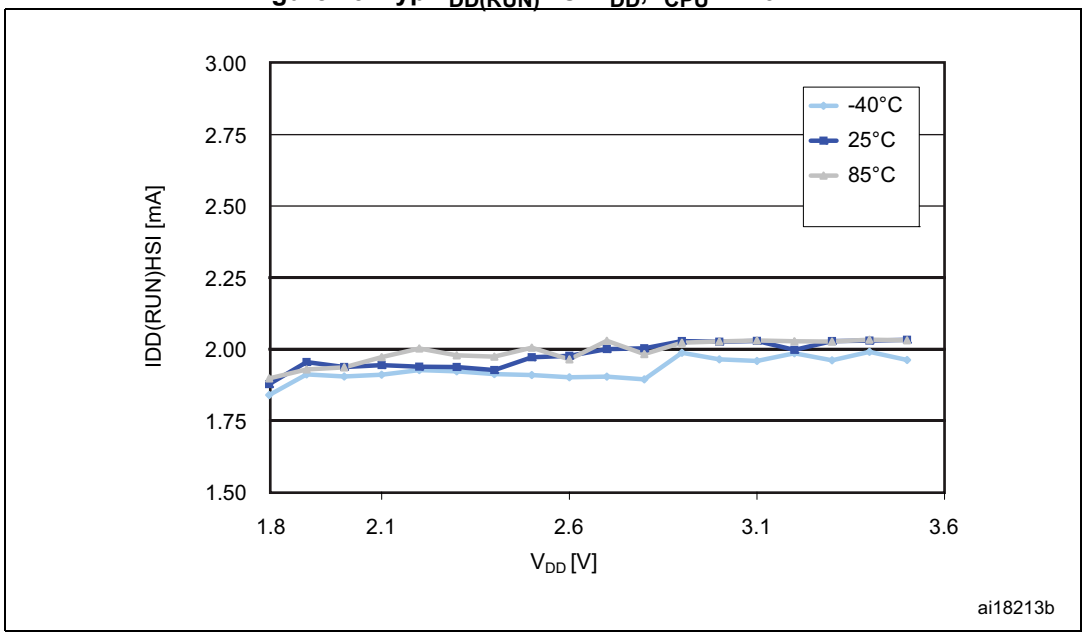
- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

In the following table, data is based on characterization results, unless otherwise specified.

Subject to general operating conditions for V_{DD} and T_A.

5. CPU executing typical data processing
6. The run from RAM consumption can be approximated with the linear formula:
   I_{DD}(run_from_RAM) = Freq * 90 µA/MHz + 380 µA
7. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 31*.
8. Tested in production.
9. The run from Flash consumption can be approximated with the linear formula:
   I_{DD}(run_from_Flash) = Freq * 195 µA/MHz + 440 µA
10. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*.

Figure 13. Typ. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from RAM

Table 21. Total current consumption in Wait mode (continued)

Symbol	Parameter	Conditions[1]			Typ	Max				Unit
						55°C	85 °C[2]	105 °C (3)	125 °C (4)	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.38	0.48	0.49	0.50	0.56	mA
				f_{CPU} = 1 MHz	0.41	0.49	0.51	0.53	0.59	
				f_{CPU} = 4 MHz	0.50	0.57	0.58	0.62	0.66	
				f_{CPU} = 8 MHz	0.60	0.66	0.68	0.72	0.74	
				f_{CPU} = 16 MHz	0.79	0.84	0.86	0.87	0.90	
			HSE[6] external clock (f_{CPU}=HSE)	f_{CPU} = 125 kHz	0.06	0.08	0.09	0.10	0.12	
				f_{CPU} = 1 MHz	0.10	0.17	0.18	0.19	0.22	
				f_{CPU} = 4 MHz	0.24	0.36	0.39	0.41	0.44	
				f_{CPU} = 8 MHz	0.50	0.58	0.61	0.62	0.64	
				f_{CPU} = 16 MHz	1.00	1.08	1.14	1.16	1.18	
			LSI	$f_{CPU} = f_{LSI}$	0.055	0.058	0.065	0.073	0.080	
			LSE[8] external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.051	0.056	0.060	0.065	0.073	

1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU} = f_{SYSCLK}$
2. For temperature range 6.
3. For temperature range 7.
4. For temperature range 3.
5. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
6. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 31*.
7. Tested in production.
8. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*.

Figure 25. Typ. V_{OL} @ V_{DD} = 3.0 V (high sink ports)

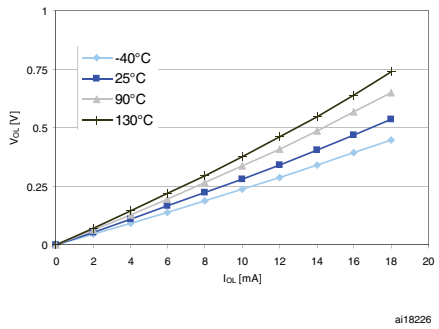


Figure 26. Typ. V_{OL} @ V_{DD} = 1.8 V (high sink ports)

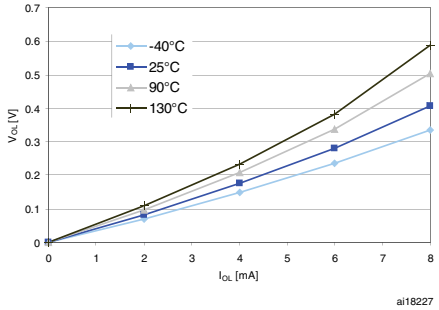


Figure 27. Typ. V_{OL} @ V_{DD} = 3.0 V (true open drain ports)

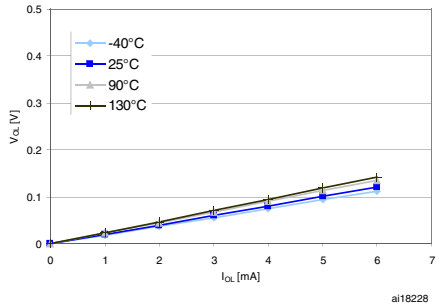


Figure 28. Typ. V_{OL} @ V_{DD} = 1.8 V (true open drain ports)

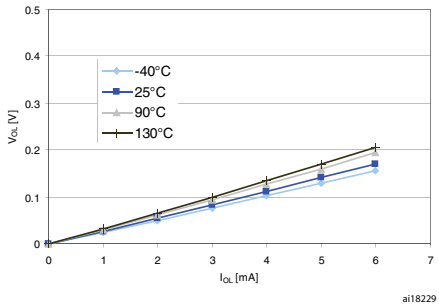


Figure 29. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.0 V (high sink ports)

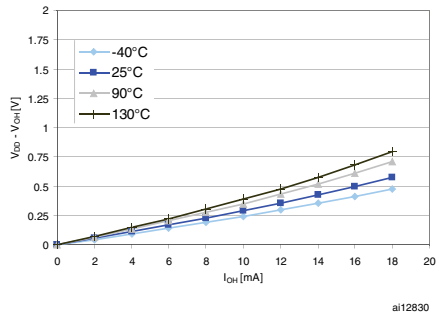
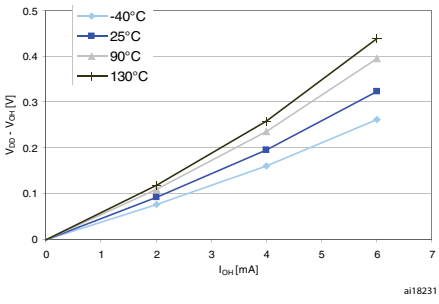


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 1.8 V (high sink ports)



NRST pin

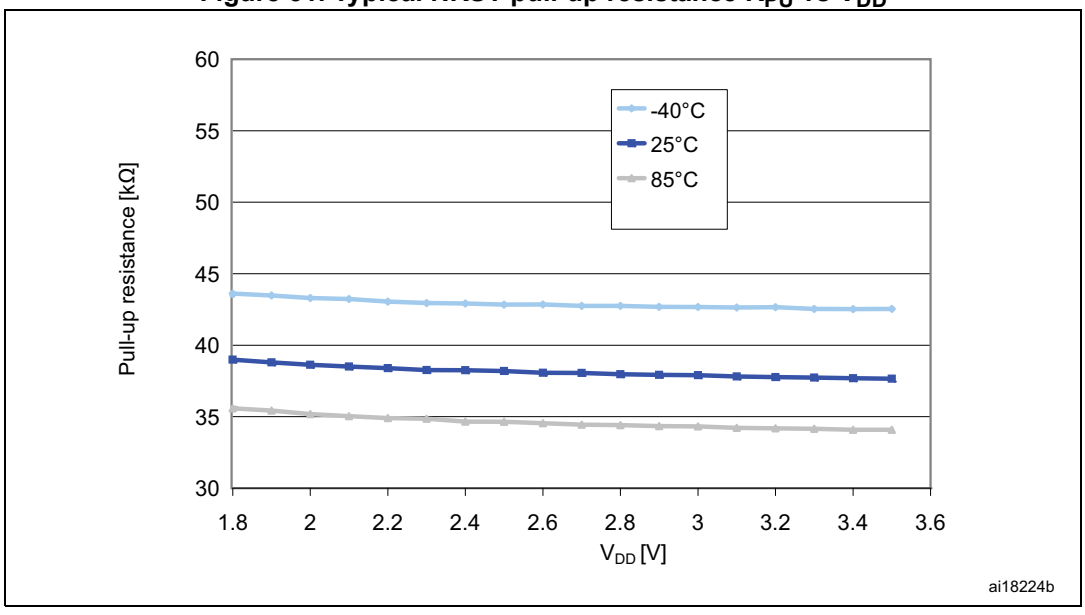
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. $\overline{\text{NRST}}$ pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage (1)	I_{OL} = 2 mA for 2.7 V ≤V_{DD} ≤3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA for V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis(3)	-	10%V_{DD} (2)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor (1)	-	30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse (3)	-	-	-	50	ns
$V_{NF(NRST)}$	NRST input not filtered pulse (3)	-	300	-	-	

1. Data based on characterization results.
2. 200 mV min.
3. Data guaranteed by design.

Figure 31. Typical NRST pull-up resistance R_{PU} vs V_{DD}



In the following three tables, data is guaranteed by characterization result, not tested in production.

Table 54. ADC1 accuracy with V_{DDA} = 3.3 V to 2.5 V

Symbol	Parameter	Conditions	Typ	Max	Unit
DNL	Differential non linearity	f_{ADC} = 16 MHz	1	1.6	LSB
		f_{ADC} = 8 MHz	1	1.6	
		f_{ADC} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC} = 16 MHz	1.2	2	
		f_{ADC} = 8 MHz	1.2	1.8	
		f_{ADC} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC} = 16 MHz	2.2	3.0	
		f_{ADC} = 8 MHz	1.8	2.5	
		f_{ADC} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC} = 16 MHz	1.5	2	LSB
		f_{ADC} = 8 MHz	1	1.5	
		f_{ADC} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC} = 16 MHz	1	1.5	
		f_{ADC} = 8 MHz			
		f_{ADC} = 4 MHz			

Table 55. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	LSB
TUE	Total unadjusted error	2	4	LSB
Offset	Offset error	1	2	LSB
Gain	Gain error	1.5	3	LSB

Table 56. ADC1 accuracy with $V_{DDA} = V_{REF}^+$ = 1.8 V to 2.4 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	LSB
TUE	Total unadjusted error	3	5	LSB
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

Figure 40. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

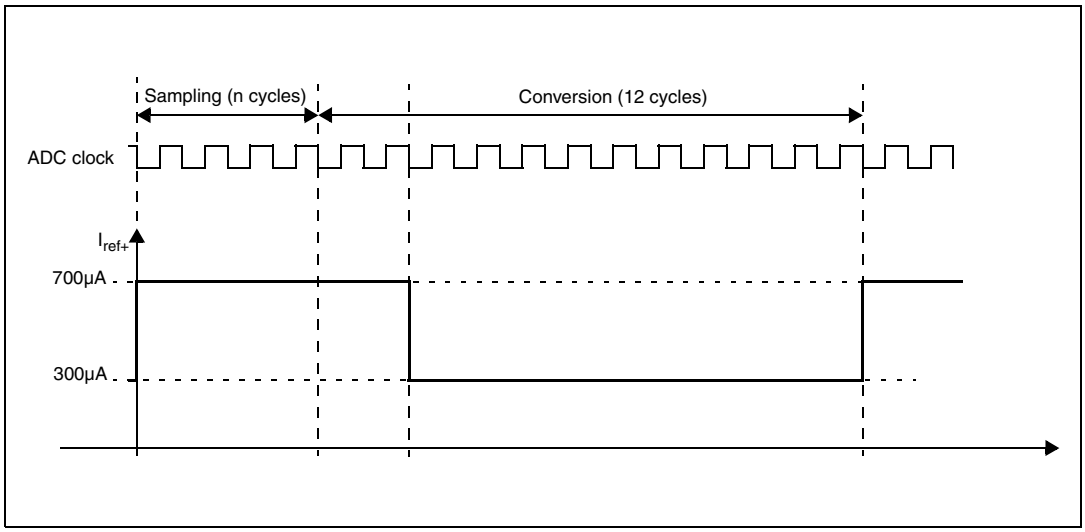


Table 57. R_{AIN} max for f_{ADC} = 16 MHz(1)

Ts (cycles)	Ts (µs)	R_{AIN} max (kohm)			
		Slow channels		Fast channels	
		2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA} < 3.3 V	1.8 V < V_{DDA} < 2.4 V
4	0.25	Not allowed	Not allowed	0.7	Not allowed
9	0.5625	0.8	Not allowed	2.0	1.0
16	1	2.0	0.8	4.0	3.0
24	1.5	3.0	1.8	6.0	4.5
48	3	6.8	4.0	15.0	10.0
96	6	15.0	10.0	30.0	20.0
192	12	32.0	25.0	50.0	40.0
384	24	50.0	50.0	50.0	50.0

1. Guaranteed by design.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 41* or *Figure 42*, depending on whether V_{REF+} is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

10.8 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 18: General operating conditions on page 66*.

The maximum chip-junction temperature, T_{Jmax}, in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 68. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 48- 7 x 7 mm	65	°C/W
Θ_{JA}	Thermal resistance junction-ambient UFQFPN 48- 7 x 7mm	32	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	°C/W
Θ_{JA}	Thermal resistance junction-ambient UFQFPN 32 - 5 x 5 mm	38	°C/W
Θ_{JA}	Thermal resistance junction-ambient UFQFPN28 - 4 x 4 mm	118	°C/W
Θ_{JA}	Thermal resistance junction-ambient WLCSP28	70	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.