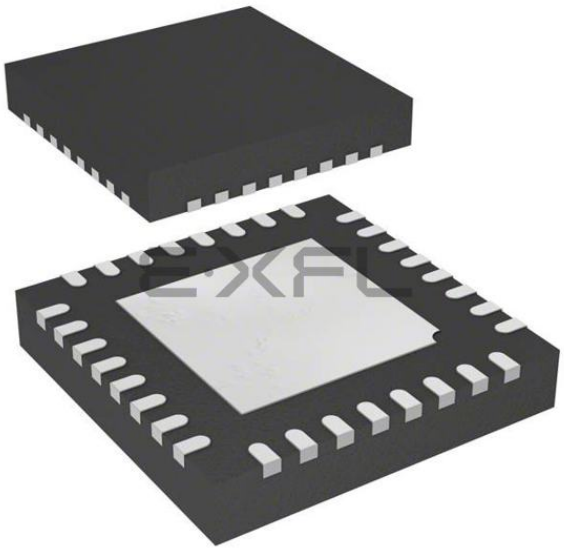

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	30
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151k6u3

IWDG: Independent watchdog
LCD: Liquid crystal display
POR/PDR: Power on reset / power down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

3.1 Low-power modes

The medium-density STM8L151x4/6 and STM8L152x4/6 devices support five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: The CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt, event or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode). Wait consumption: refer to *Table 21*.
- **Low power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power run mode consumption: refer to *Table 22*.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power wait mode consumption: refer to *Table 23*.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset. Active-halt consumption: refer to *Table 24* and *Table 25*.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs. Halt consumption: refer to *Table 26*.

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
30	-	-	-	PB6/[*SPI1_MOSI*](4)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out/slave in]*/ LCD segment 16 / ADC1_IN12 / Comparator 1 positive input
-	19	18	F1	PB6/*[SPI1_MOSI]*(4)/ LCD_SEG16(2)/ ADC1_IN12/COMP1_INP/ DAC_OUT	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out]*/ slave in / LCD segment 16 / ADC1_IN12 / DAC output / Comparator 1 positive input
31	20	19	E1	PB7/*[SPI1_MISO]*(4)/ LCD_SEG17(2)/ ADC1_IN11/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port B7**	*[SPI1 master in- slave out]* / LCD segment 17 / ADC1_IN11 / Comparator 1 positive input
37	25	21	B1	PC0(5)/I2C1_SDA	I/O	FT	**X**		X		T(7)		**Port C0**	I2C1 data
38	26	22	A1	PC1(5)/I2C1_SCL	I/O	FT	**X**		X		T(7)		**Port C1**	I2C1 clock
41	27	23	B2	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREFINT	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6 / Comparator 1 positive input / Internal voltage reference output
42	28	24	A2	PC3/USART1_TX/ LCD_SEG23(2)/ ADC1_IN5/COMP1_INP/ COMP2_INM	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5 / Comparator 1 positive input / Comparator 2 negative input
43	29	25	C2	PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24(2)/ ADC1_IN4/COMP2_INM/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C4**	USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
36	24	-	-	PD7/TIM1_CH1N /LCD_SEG21(2)/ ADC1_IN7/RTC_ALARM/ VREFINT/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D7**	Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm / Internal voltage reference output /Comparator 1 positive input
14	-	-	-	PE0(5)/LCD_SEG1(2)	I/O	FT	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1
15	-	-	-	PE1/TIM1_CH2N /LCD_SEG2(2)	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2
16	-	-	-	PE2/TIM1_CH3N /LCD_SEG3(2)	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E2**	Timer 1 - inverted channel 3 / LCD segment 3
17	-	-	-	PE3/LCD_SEG4(2)	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E3**	LCD segment 4
18	-	-	-	PE4/LCD_SEG5(2)	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E4**	LCD segment 5
19	-	-	-	PE5/LCD_SEG6(2)/ ADC1_IN23/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E5**	LCD segment 6 / ADC1_IN23 / Comparator 2 positive input / Comparator 1 positive input
47	-	-	-	PE6/LCD_SEG26(2)/ PVD_IN	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E6**	LCD segment 26/PVD_IN
48	-	-	-	PE7/LCD_SEG27(2)	I/O	TT (3)	**X**	X	X	HS	X	X	**Port E7**	LCD segment 27
32	-	-	-	PF0/ADC1_IN24/ DAC_OUT	I/O	TT (3)	**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC_OUT
13	9	-	-	VLCD(2)	S	-	**-**	-	-	-	-	-	LCD booster external capacitor	
13	-	-	-	Reserved(8)	-	-	**-**	-	-	-	-	-	Reserved. Must be tied to V_{DD}	
10	-	-	-	V_{DD}	S	-	**-**	-	-	-	-	-	Digital power supply	
11	-	-	-	V_{DDA}	S	-	**-**	-	-	-	-	-	Analog supply voltage	
12	-	-	-	V_{REF+}	S	-	**-**	-	-	-	-	-	ADC1 and DAC positive voltage reference	

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_DIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00
0x00 50C2		CLK_ICKR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x80
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0bxxxx0000
0x00 50CA		CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0xxx
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11100x

Table 20. Total current consumption in Run mode

Symbol	Parameter	Conditions(1)			Typ	Max				Unit
						55 °C	85 °C(2)	105°C(3)	125 °C(4)	
$I_{DD(RUN)}$	Supply current in run mode(5)	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)(6)	f_{CPU} = 125 kHz	0.39	0.47	0.49	0.52	0.55	mA
				f_{CPU} = 1 MHz	0.48	0.56	0.58	0.61	0.65	
				f_{CPU} = 4 MHz	0.75	0.84	0.86	0.91	0.99	
				f_{CPU} = 8 MHz	1.10	1.20	1.25	1.31	1.40	
				f_{CPU} = 16 MHz	1.85	1.93	2.12(8)	2.29(8)	2.36(8)	
			HSE external clock ($f_{CPU}=f_{HSE}$)(7)	f_{CPU} = 125 kHz	0.05	0.06	0.09	0.11	0.12	
				f_{CPU} = 1 MHz	0.18	0.19	0.20	0.22	0.23	
				f_{CPU} = 4 MHz	0.55	0.62	0.64	0.71	0.77	
				f_{CPU} = 8 MHz	0.99	1.20	1.21	1.22	1.24	
				f_{CPU} = 16 MHz	1.90	2.22	2.23(8)	2.24(8)	2.28(8)	
			LSI RC osc. (typ. 38 kHz)	$f_{CPU} = f_{LSI}$	0.040	0.045	0.046	0.048	0.050	
			LSE external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.035	0.040	0.048(8)	0.050	0.062	
$I_{DD(RUN)}$	Supply current in Run mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI RC osc.(9)	f_{CPU} = 125 kHz	0.43	0.55	0.56	0.58	0.62	mA
				f_{CPU} = 1 MHz	0.60	0.77	0.80	0.82	0.87	
				f_{CPU} = 4 MHz	1.11	1.34	1.37	1.39	1.43	
				f_{CPU} = 8 MHz	1.90	2.20	2.23	2.31	2.40	
				f_{CPU} = 16 MHz	3.8	4.60	4.75	4.87	4.88	
			HSE external clock ($f_{CPU}=f_{HSE}$) (7)	f_{CPU} = 125 kHz	0.30	0.36	0.39	0.44	0.47	
				f_{CPU} = 1 MHz	0.40	0.50	0.52	0.55	0.56	
				f_{CPU} = 4 MHz	1.15	1.31	1.40	1.45	1.48	
				f_{CPU} = 8 MHz	2.17	2.33	2.44	2.56	2.77	
				f_{CPU} = 16 MHz	4.0	4.46	4.52	4.59	4.77	
			LSI RC osc.	$f_{CPU} = f_{LSI}$	0.110	0.123	0.130	0.140	0.150	
			LSE ext. clock (32.768 kHz)(10)	$f_{CPU} = f_{LSE}$	0.100	0.101	0.104	0.119	0.122	

1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU}=f_{SYSCLK}$
2. For devices with suffix 6
3. For devices with suffix 7
4. For devices with suffix 3

Table 21. Total current consumption in Wait mode (continued)

Symbol	Parameter	Conditions[1]			Typ	Max				Unit
						55°C	85 °C[2]	105 °C (3)	125 °C (4)	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.38	0.48	0.49	0.50	0.56	mA
				f_{CPU} = 1 MHz	0.41	0.49	0.51	0.53	0.59	
				f_{CPU} = 4 MHz	0.50	0.57	0.58	0.62	0.66	
				f_{CPU} = 8 MHz	0.60	0.66	0.68	0.72	0.74	
				f_{CPU} = 16 MHz	0.79	0.84	0.86	0.87	0.90	
			HSE[6] external clock (f_{CPU}=HSE)	f_{CPU} = 125 kHz	0.06	0.08	0.09	0.10	0.12	
				f_{CPU} = 1 MHz	0.10	0.17	0.18	0.19	0.22	
				f_{CPU} = 4 MHz	0.24	0.36	0.39	0.41	0.44	
				f_{CPU} = 8 MHz	0.50	0.58	0.61	0.62	0.64	
				f_{CPU} = 16 MHz	1.00	1.08	1.14	1.16	1.18	
			LSI	$f_{CPU} = f_{LSI}$	0.055	0.058	0.065	0.073	0.080	
			LSE[8] external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.051	0.056	0.060	0.065	0.073	

1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU} = f_{SYSCLK}$
2. For temperature range 6.
3. For temperature range 7.
4. For temperature range 3.
5. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
6. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 31*.
7. Tested in production.
8. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*.

In the following table, data is based on characterization results, unless otherwise specified.

Table 22. Total current consumption and timing in Low power run mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions[1]			Typ	Max	Unit
$I_{DD(LPR)}$	Supply current in Low power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.1	5.4	µA
				T_A = 55 °C	5.7	6	
				T_A = 85 °C	6.8	7.5	
				T_A = 105 °C	9.2	10.4	
				T_A = 125 °C	13.4	16.6	
			with TIM2 active[2]	T_A = -40 °C to 25 °C	5.4	5.7	
				T_A = 55 °C	6.0	6.3	
				T_A = 85 °C	7.2	7.8	
				T_A = 105 °C	9.4	10.7	
				T_A = 125 °C	13.8	17	
		LSE [3] external clock (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.25	5.6	
				T_A = 55 °C	5.67	6.1	
				T_A = 85 °C	5.85	6.3	
				T_A = 105 °C	7.11	7.6	
				T_A = 125 °C	9.84	12	
			with TIM2 active [2]	T_A = -40 °C to 25 °C	5.59	6	
				T_A = 55 °C	6.10	6.4	
				T_A = 85 °C	6.30	7	
				T_A = 105 °C	7.55	8.4	
				T_A = 125 °C	10.1	15	

1. No floating I/Os
2. Timer 2 clock enabled and counter running
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*

HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Motional resistance (see crystal specification), L_m: Motional inductance (see crystal specification),
C_m: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification),
C_{L1}=C_{L2}=C: Grounded external capacitance
$g_m >> g_{mcrit}$

LSE crystal/ceramic resonator oscillator

The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 32. LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	ΔV = 200 mV	-	1.2	-	MΩ
C(1)	Recommended load capacitance (2)	-	-	8	-	pF
$I_{DD(LSE)}$	LSE oscillator power consumption	-	-	-	1.4(3)	µA
		V_{DD} = 1.8 V	-	450	-	nA
		V_{DD} = 3 V	-	600	-	
		V_{DD} = 3.6 V	-	750	-	
g_m	Oscillator transconductance	-	3(3)	-	-	µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	s

1. C=C_{L1}=C_{L2} is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details.
3. Data guaranteed by design.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

9.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 35. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

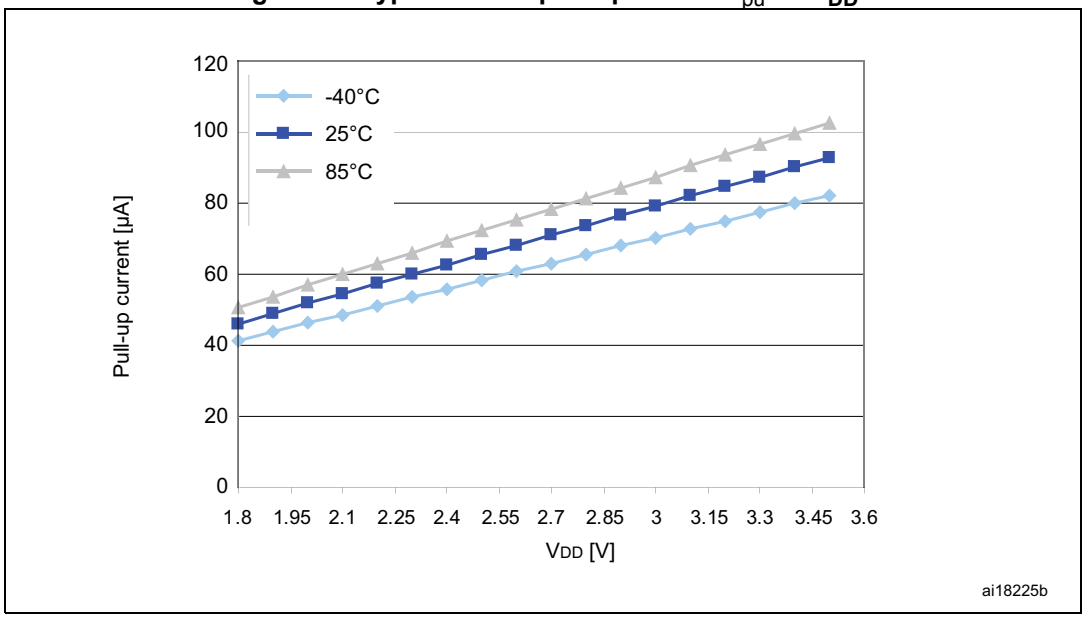
Flash memory

Table 36. Flash program and data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1 or 64 bytes (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 64 bytes (block) write cycles (on erased byte)	-	-	3	-	ms
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-	0.7	-	
t_{RET} (2)	Data retention (program memory) after 10000 erase/write cycles at T_A= –40 to +85 °C (6 suffix)	T_{RET} = +85 °C	30(1)	-	-	years
	Data retention (program memory) after 10000 erase/write cycles at T_A= –40 to +125 °C (3 suffix)	T_{RET} = +125 °C	5(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A= –40 to +85 °C (6 suffix)	T_{RET} = +85 °C	30(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A= –40 to +125 °C (3 suffix)	T_{RET} = +125 °C	5(1)	-	-	
N_{RW} (3)	Erase/write cycles (program memory)	T_A = –40 to +85 °C (6 suffix), T_A = –40 to +125 °C (3 suffix)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)		300(1) (4)	-	-	

1. Data based on characterization results.
2. Conforming to JEDEC JESD22a117
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.
4. Data based on characterization performed on the whole data memory.

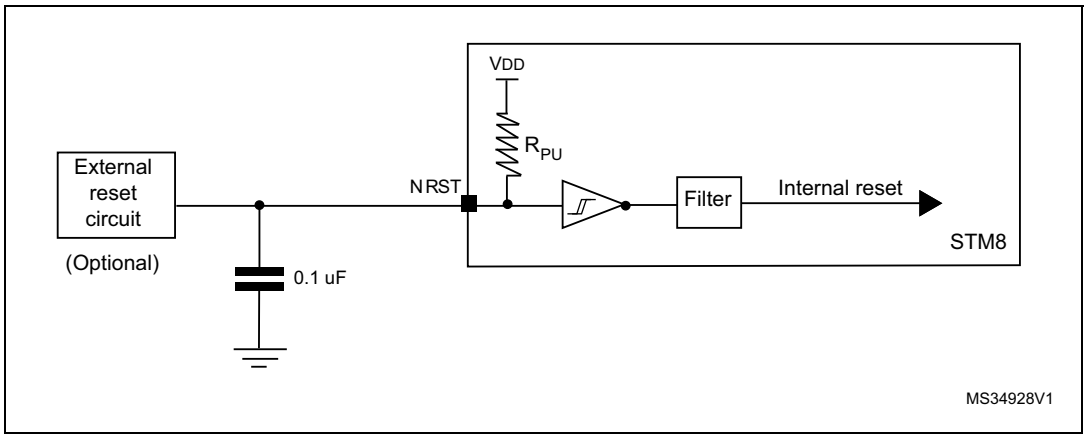
Figure 32. Typical NRST pull-up current I_{pu} vs V_{DD}



The reset network shown in *Figure 33* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max. level specified in *Table 42*. Otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, attention must be paid to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. The minimum recommended capacity is 10 nF.

Figure 33. Recommended NRST pin configuration



In the following three tables, data is guaranteed by characterization result, not tested in production.

Table 54. ADC1 accuracy with V_{DDA} = 3.3 V to 2.5 V

Symbol	Parameter	Conditions	Typ	Max	Unit
DNL	Differential non linearity	f_{ADC} = 16 MHz	1	1.6	LSB
		f_{ADC} = 8 MHz	1	1.6	
		f_{ADC} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC} = 16 MHz	1.2	2	
		f_{ADC} = 8 MHz	1.2	1.8	
		f_{ADC} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC} = 16 MHz	2.2	3.0	
		f_{ADC} = 8 MHz	1.8	2.5	
		f_{ADC} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC} = 16 MHz	1.5	2	LSB
		f_{ADC} = 8 MHz	1	1.5	
		f_{ADC} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC} = 16 MHz	1	1.5	
		f_{ADC} = 8 MHz			
		f_{ADC} = 4 MHz			

Table 55. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	LSB
TUE	Total unadjusted error	2	4	LSB
Offset	Offset error	1	2	LSB
Gain	Gain error	1.5	3	LSB

Table 56. ADC1 accuracy with $V_{DDA} = V_{REF}^+$ = 1.8 V to 2.4 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	LSB
TUE	Total unadjusted error	3	5	LSB
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

Figure 41. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

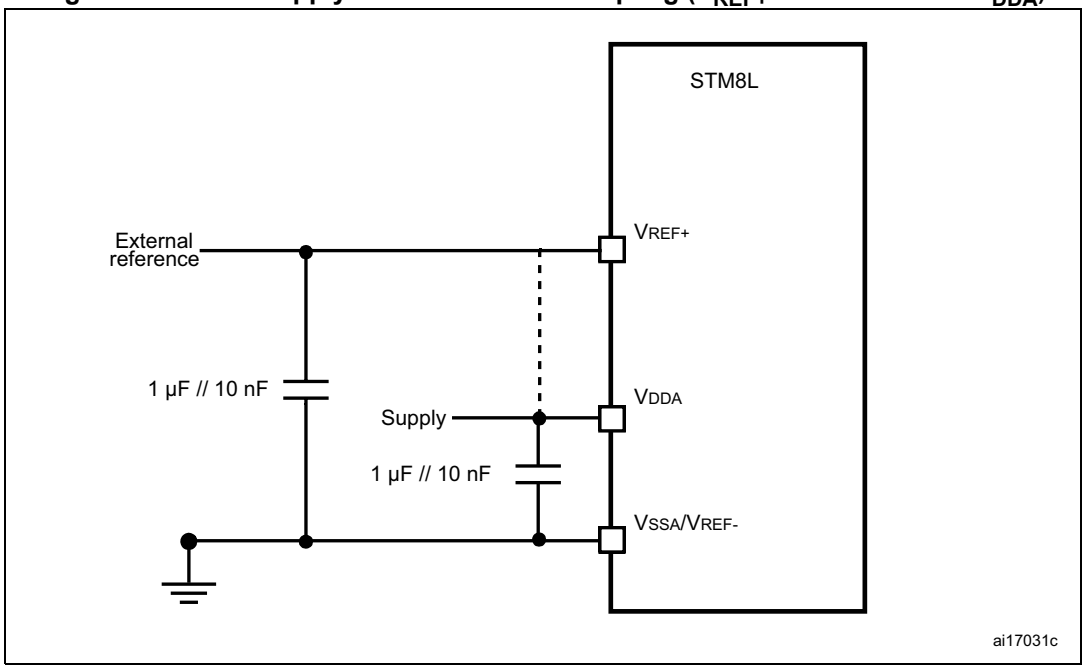
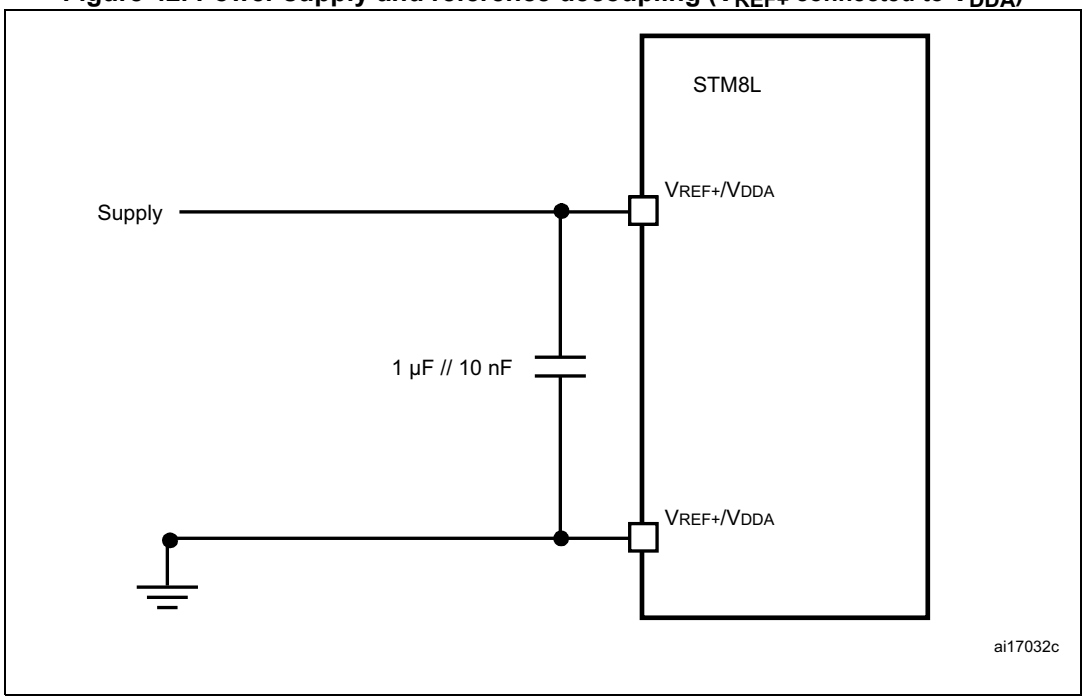


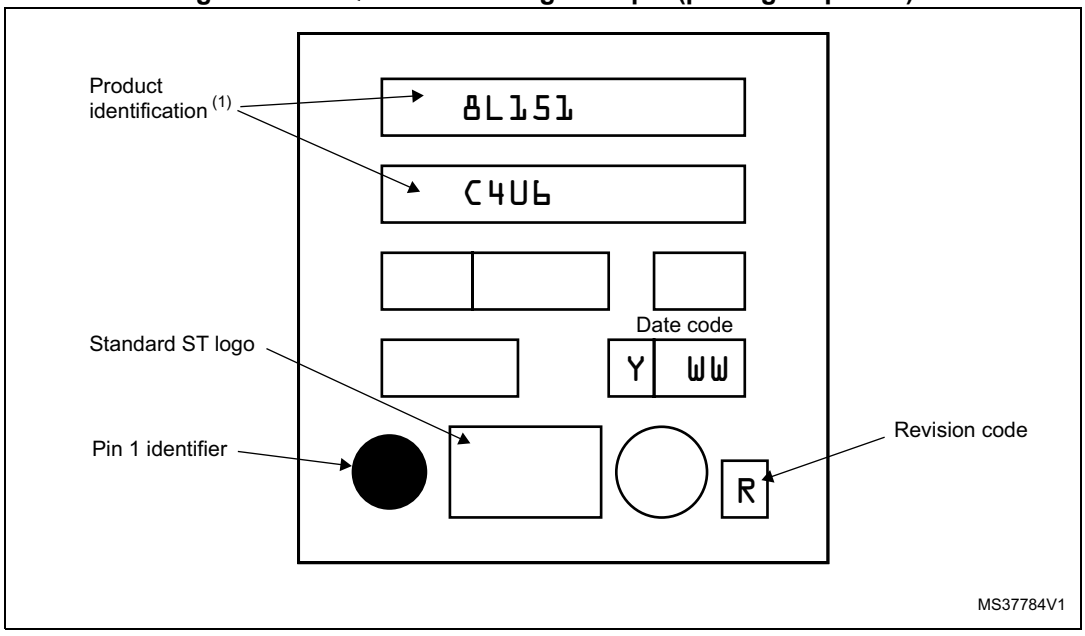
Figure 42. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 48. UFQFPN48 marking example (package top view)

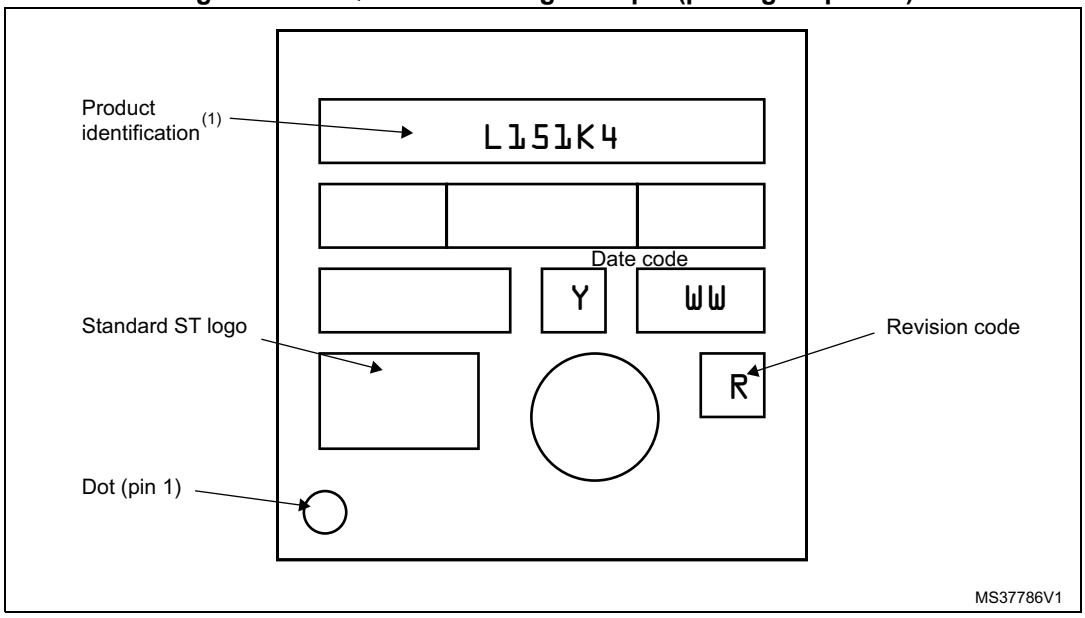


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

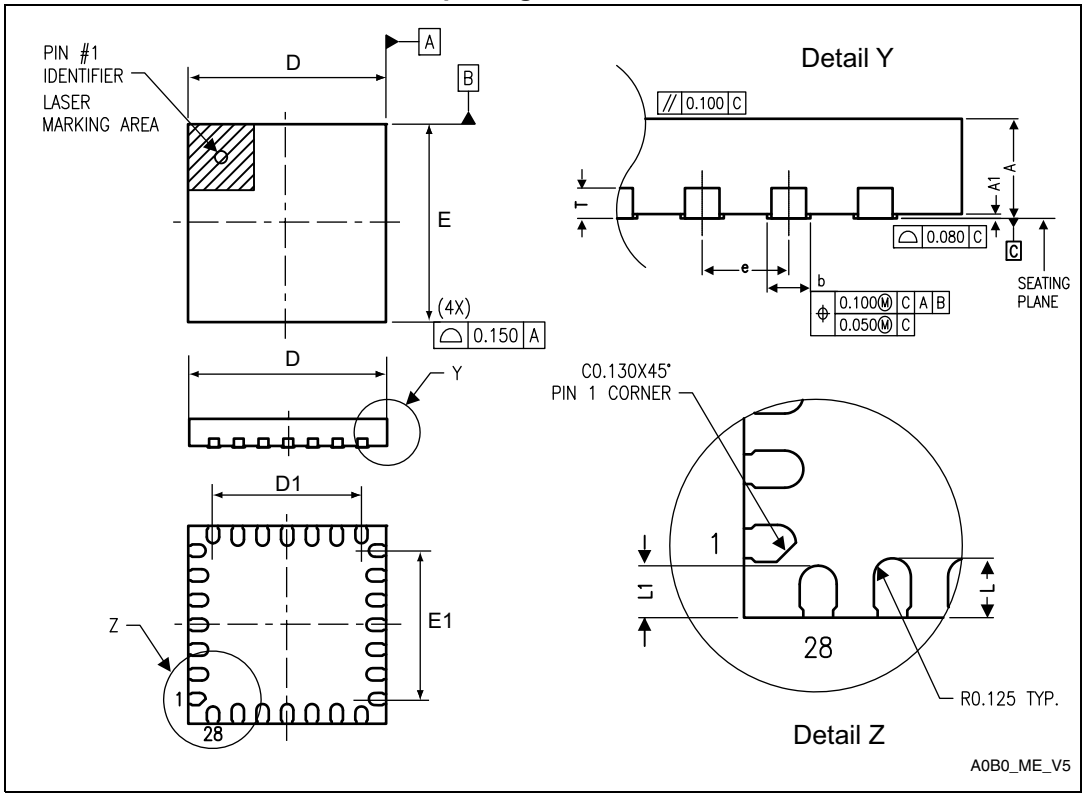
Figure 54. UFQFPN32 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

10.6 UFQFPN28 package information

Figure 55. UFQFPN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



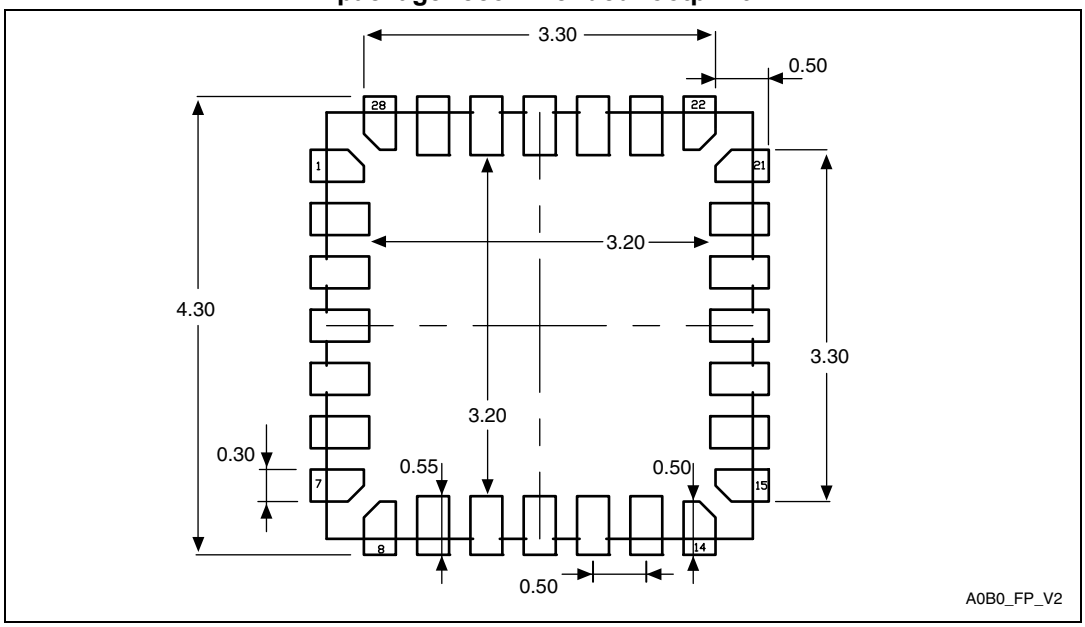
1. Drawing is not to scale.

Table 66. UFQFPN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data(1)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 56. UFQFPN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

10.8 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 18: General operating conditions on page 66*.

The maximum chip-junction temperature, T_{Jmax}, in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 68. Thermal characteristics(1)

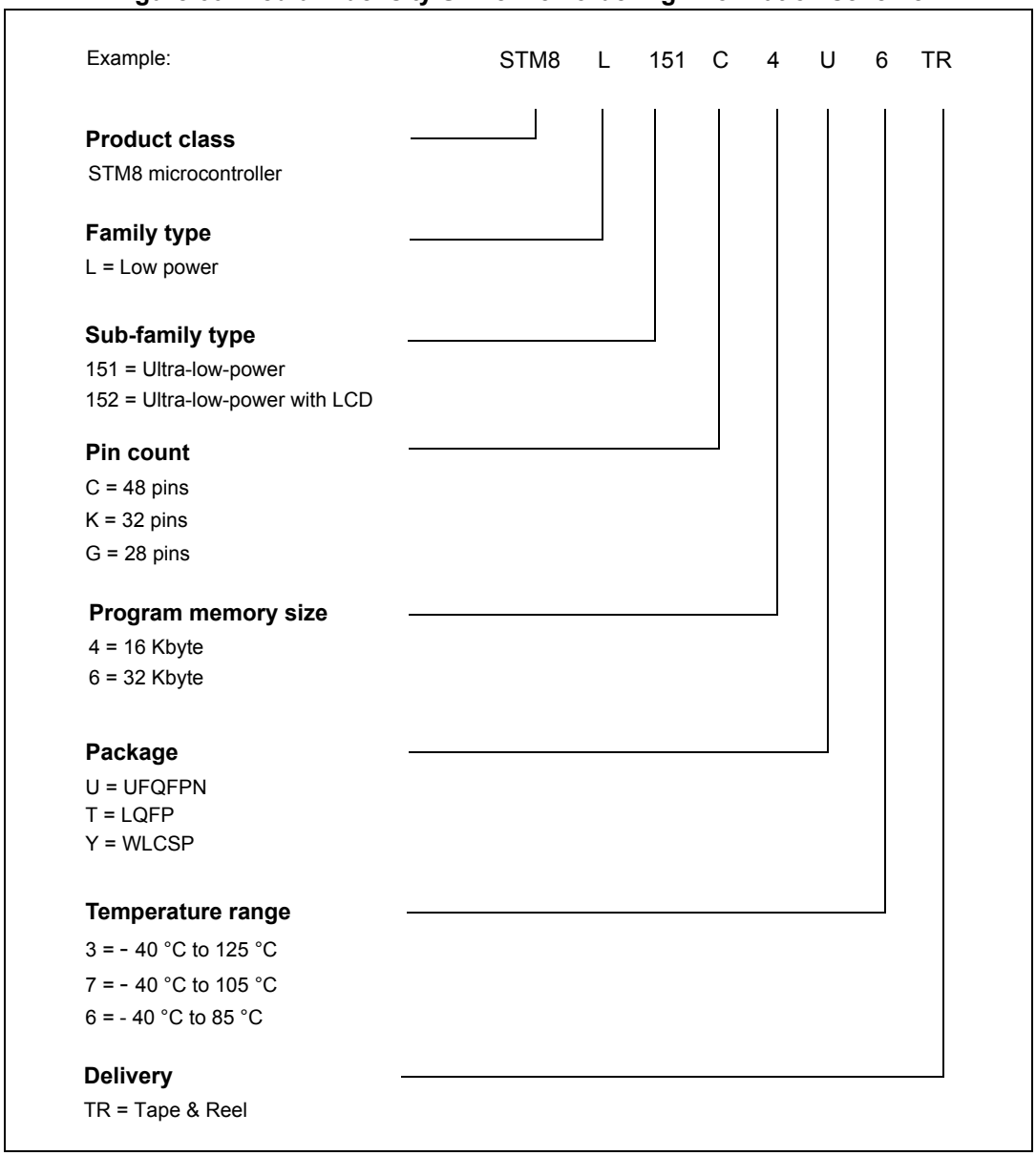
Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 48- 7 x 7 mm	65	°C/W
Θ_{JA}	Thermal resistance junction-ambient UFQFPN 48- 7 x 7mm	32	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	°C/W
Θ_{JA}	Thermal resistance junction-ambient UFQFPN 32 - 5 x 5 mm	38	°C/W
Θ_{JA}	Thermal resistance junction-ambient UFQFPN28 - 4 x 4 mm	118	°C/W
Θ_{JA}	Thermal resistance junction-ambient WLCSP28	70	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Figure 60. Medium-density STM8L15x ordering information scheme



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please contact the ST sales office nearest to you.