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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | STM8 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT |
| Number of I/O | 41 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 25x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l152c4t3 |

## 3.2 Central processing unit STM8

### 3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

#### Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

#### Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

#### Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

### 3.2.2 Interrupt controller

The medium-density STM8L151x4/6 and STM8L152x4/6 feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

## 3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

### Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources can be used to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 kHz Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC and LCD clock sources:** the above four sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

*Note: ADC1 can be served by DMA1.*

## 3.10 Digital-to-analog converter (DAC)

- 12-bit DAC with output buffer
- Synchronized update capability using TIM4
- DMA capability
- External triggers for conversion
- Input reference voltage $V_{REF+}$ for better resolution

*Note: DAC can be served by DMA1.*

## 3.11 Ultra-low-power comparators

The medium-density STM8L151x4/6 and STM8L152x4/6 embed two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage or internal reference voltage sub multiple (1/4, 1/2, 3/4)

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

## 3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC and the internal reference voltage $V_{REFINT}$. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (*Section 3.13: Touch sensing*).

## 3.13 Touch sensing

Medium-density STM8L151x4/6 and STM8L152x4/6 devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (example, glass, plastic). The capacitive variation introduced by a finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. In medium-density STM8L151x4/6

### 3.14.2 16-bit general purpose timers

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

### 3.14.3 8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow or for DAC trigger generation.

## 3.15 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

### 3.15.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

### 3.15.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

## 3.16 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

**Table 4. Legend/abbreviation for table 5**

| | | |
|---|---|---|
| **Type** | I= input, O = output, S = power supply | |
| **Level** | FT | Five-volt tolerant |
| | TT | 3.6 V tolerant |
| | Output | HS = high sink/source (20 mA) |
| **Port and control configuration** | Input | float = floating, wpu = weak pull-up |
| | Output | T = true open drain, OD = open drain, PP = push pull |
| **Reset state** | Bold X (pin state after reset release).<br>Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state). | |

**Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48/UFQFPN48 | LQFP32/UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 2 | 1 | 1 | C3 | NRST/PA1(1) | I/O | | | **X** | | HS | | X | **Reset** | PA1 |
| 3 | 2 | 2 | B4 | PA2/OSC_IN/ *[USART1_TX]*(4)/ *[SPI1_MISO]* (4) | I/O | | **X** | X | X | HS | X | X | **Port A2** | HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out] /* |
| 4 | 3 | 3 | C4 | PA3/OSC_OUT/*[USART1_RX]*(4)/*[SPI1_MOSI]*(4) | I/O | | **X** | X | X | HS | X | X | **Port A3** | HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/* |
| 5 | - | - | - | PA4/TIM2_BKIN/ LCD_COM0(2)/ADC1_IN2/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port A4** | Timer 2 - break input / LCD COM 0 / ADC1 input 2 / Comparator 1 positive input |
| - | 4 | 4 | D3 | PA4/TIM2_BKIN/ *[TIM2_ETR]*(4)/ LCD_COM0(2)/ ADC1_IN2/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port A4** | Timer 2 - break input / *[Timer 2 - external trigger]* / LCD_COM 0 / ADC1 input 2 / Comparator 1 positive input |
| 6 | - | - | - | PA5/TIM3_BKIN/ LCD_COM1(2)/ADC1_IN1/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port A5** | Timer 3 - break input / LCD_COM 1 / ADC1 input 1/ Comparator 1 positive input |

**Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48/UFQFPN48 | LQFP32/UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| - | - | 9 | G2 | PD1/TIM1_CH3/[*TIM3_ETR*](4)/LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port D1** | Timer 1 channel 3 / *[Timer 3 - external trigger]* / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input |
| 22 | 11 | 10 | E4 | PD2/TIM1_CH1 /LCD_SEG8(2)/ ADC1_IN20/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port D2** | Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20 / Comparator 1 positive input |
| 23 | 12 | - | - | PD3/ TIM1_ETR/ LCD_SEG9(2)/ADC1_IN19/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port D3** | Timer 1 - external trigger / LCD segment 9 / ADC1_IN19 / Comparator 1 positive input |
| - | - | 11 | F3 | PD3/ TIM1_ETR/ LCD_SEG9(2)/ ADC1_IN19/TIM1_BKIN/ COMP1_INP/ RTC_CALIB | I/O | TT (3) | **X** | X | X | HS | X | X | **Port D3** | Timer 1 - external trigger / LCD segment 9 / ADC1_IN19 / Timer 1 break input / RTC calibration / Comparator 1 positive input |
| 33 | 21 | 20 | C1 | PD4/TIM1_CH2 /LCD_SEG18(2)/ ADC1_IN10/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port D4** | Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/ Comparator 1 positive input |
| 34 | 22 | - | - | PD5/TIM1_CH3 /LCD_SEG19(2)/ ADC1_IN9/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port D5** | Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ Comparator 1 positive input |
| 35 | 23 | - | - | PD6/TIM1_BKIN /LCD_SEG20(2)/ ADC1_IN8/RTC_CALIB/ /VREFINT/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port D6** | Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration / Internal voltage reference output / Comparator 1 positive input |

## 4.1 System configuration options

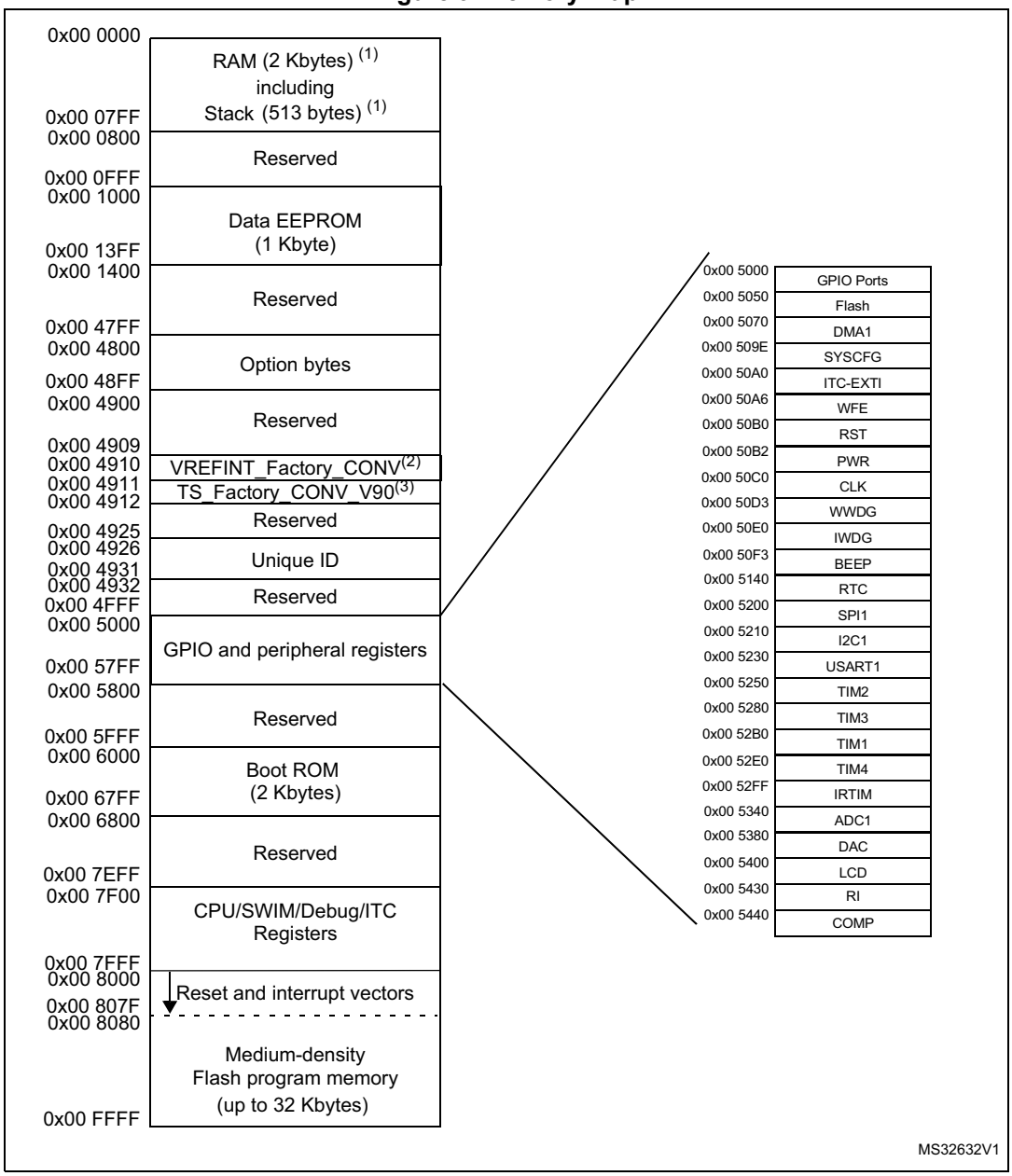
As shown in *Table 5: Medium-density STM8L151x4/6, STM8L152x4/6 pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the “Routing interface (RI) and system configuration controller” section in the STM8L15xxx and STM8L16xxx reference manual (RM0031).

# 5 Memory and register map

## 5.1 Memory mapping

The memory map is shown in *Figure 9*.

**Figure 9. Memory map**

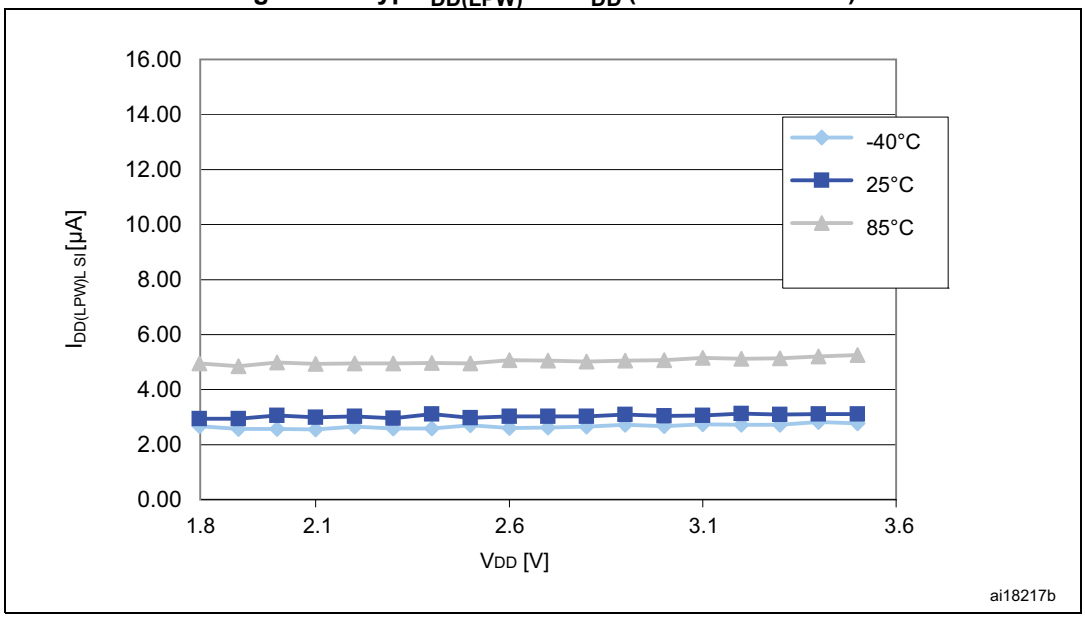



1. *Table 6* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. The VREFINT_Factory_CONV byte represents the LSB of the $V_{REFINT}$ 12-bit ADC conversion result. The MSB have a fixed value: 0x6.
3. The TS_Factory_CONV_V90 byte represents the LSB of the $V_{90}$ 12-bit ADC conversion result. The MSB

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 52B0 | TIM1 | TIM1_CR1 | TIM1 control register 1 | 0x00 |
| 0x00 52B1 | | TIM1_CR2 | TIM1 control register 2 | 0x00 |
| 0x00 52B2 | | TIM1_SMCR | TIM1 Slave mode control register | 0x00 |
| 0x00 52B3 | | TIM1_ETR | TIM1 external trigger register | 0x00 |
| 0x00 52B4 | | TIM1_DER | TIM1 DMA1 request enable register | 0x00 |
| 0x00 52B5 | | TIM1_IER | TIM1 Interrupt enable register | 0x00 |
| 0x00 52B6 | | TIM1_SR1 | TIM1 status register 1 | 0x00 |
| 0x00 52B7 | | TIM1_SR2 | TIM1 status register 2 | 0x00 |
| 0x00 52B8 | | TIM1_EGR | TIM1 event generation register | 0x00 |
| 0x00 52B9 | | TIM1_CCMR1 | TIM1 Capture/Compare mode register 1 | 0x00 |
| 0x00 52BA | | TIM1_CCMR2 | TIM1 Capture/Compare mode register 2 | 0x00 |
| 0x00 52BB | | TIM1_CCMR3 | TIM1 Capture/Compare mode register 3 | 0x00 |
| 0x00 52BC | | TIM1_CCMR4 | TIM1 Capture/Compare mode register 4 | 0x00 |
| 0x00 52BD | | TIM1_CCER1 | TIM1 Capture/Compare enable register 1 | 0x00 |
| 0x00 52BE | | TIM1_CCER2 | TIM1 Capture/Compare enable register 2 | 0x00 |
| 0x00 52BF | | TIM1_CNTRH | TIM1 counter high | 0x00 |
| 0x00 52C0 | | TIM1_CNTRL | TIM1 counter low | 0x00 |
| 0x00 52C1 | | TIM1_PSCRH | TIM1 prescaler register high | 0x00 |
| 0x00 52C2 | | TIM1_PSCRL | TIM1 prescaler register low | 0x00 |
| 0x00 52C3 | | TIM1_ARRH | TIM1 Auto-reload register high | 0xFF |
| 0x00 52C4 | | TIM1_ARRL | TIM1 Auto-reload register low | 0xFF |
| 0x00 52C5 | | TIM1_RCR | TIM1 Repetition counter register | 0x00 |
| 0x00 52C6 | | TIM1_CCR1H | TIM1 Capture/Compare register 1 high | 0x00 |
| 0x00 52C7 | | TIM1_CCR1L | TIM1 Capture/Compare register 1 low | 0x00 |
| 0x00 52C8 | | TIM1_CCR2H | TIM1 Capture/Compare register 2 high | 0x00 |
| 0x00 52C9 | | TIM1_CCR2L | TIM1 Capture/Compare register 2 low | 0x00 |
| 0x00 52CA | | TIM1_CCR3H | TIM1 Capture/Compare register 3 high | 0x00 |
| 0x00 52CB | | TIM1_CCR3L | TIM1 Capture/Compare register 3 low | 0x00 |
| 0x00 52CC | | TIM1_CCR4H | TIM1 Capture/Compare register 4 high | 0x00 |
| 0x00 52CD | | TIM1_CCR4L | TIM1 Capture/Compare register 4 low | 0x00 |
| 0x00 52CE | | TIM1_BKR | TIM1 break register | 0x00 |
| 0x00 52CF | | TIM1_DTR | TIM1 dead-time register | 0x00 |
| 0x00 52D0 | | TIM1_OISR | TIM1 output idle state register | 0x00 |
| 0x00 52D1 | | TIM1_DCR1 | DMA1 control register 1 | 0x00 |

Figure 16. Typ. $I_{DD(LPW)}$ vs. $V_{DD}$ (LSI clock source)



### Output driving current

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 39. Output driving current (high sink ports)**

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| High sink | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +2 mA, $V_{DD}$ = 3.0 V | - | 0.45 | V |
| | | | $I_{IO}$ = +2 mA, $V_{DD}$ = 1.8 V | - | 0.45 | V |
| | | | $I_{IO}$ = +10 mA, $V_{DD}$ = 3.0 V | - | 0.7 | V |
| | $V_{OH}$ (2) | Output high level voltage for an I/O pin | $I_{IO}$ = -2 mA, $V_{DD}$ = 3.0 V | $V_{DD}$-0.45 | - | V |
| | | | $I_{IO}$ = -1 mA, $V_{DD}$ = 1.8 V | $V_{DD}$-0.45 | - | V |
| | | | $I_{IO}$ = -10 mA, $V_{DD}$ = 3.0 V | $V_{DD}$-0.7 | - | V |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. The $I_{IO}$ current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.

**Table 40. Output driving current (true open drain ports)**

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Open drain | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +3 mA, $V_{DD}$ = 3.0 V | - | 0.45 | V |
| | | | $I_{IO}$ = +1 mA, $V_{DD}$ = 1.8 V | - | 0.45 | |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

**Table 41. Output driving current (PA0 with high sink LED driver capability)**

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| IR | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +20 mA, $V_{DD}$ = 2.0 V | - | 0.45 | V |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

## 9.3.8 Communication interfaces

### SPI1 - Serial peripheral interface

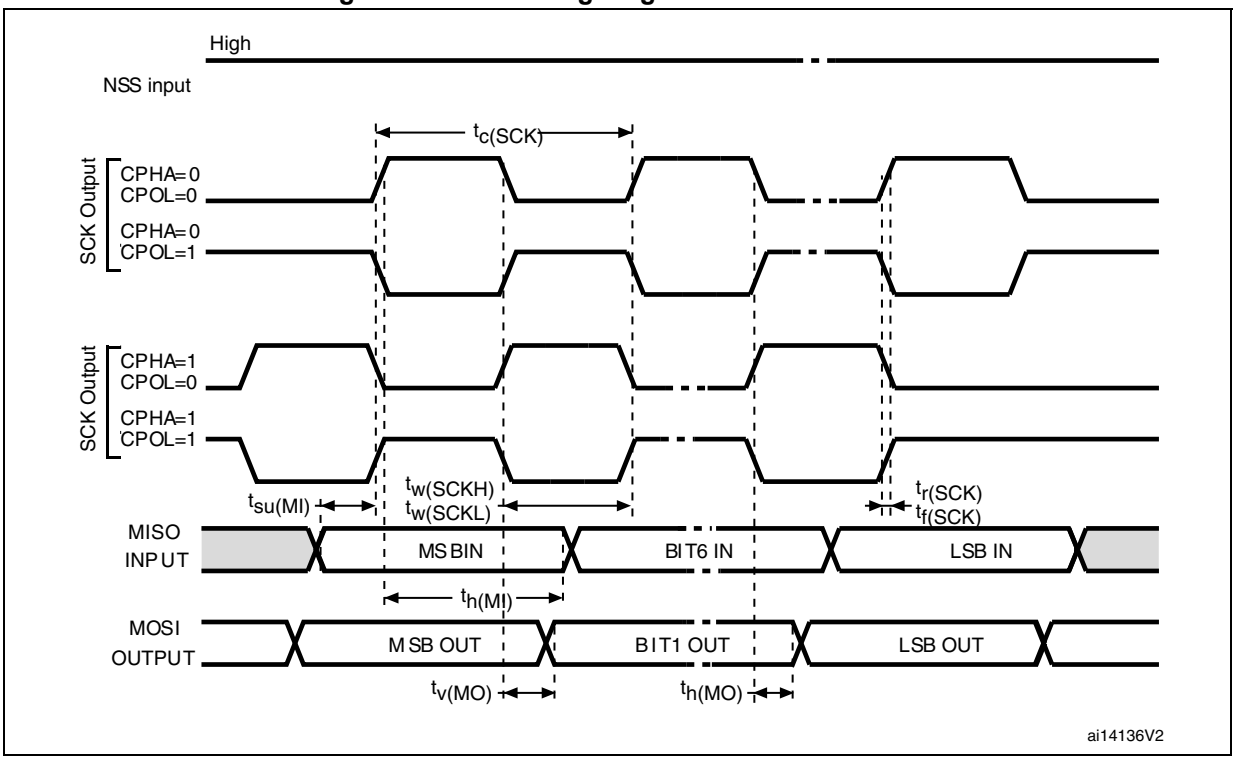
Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, $f_{SYSCLK}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 43. SPI1 characteristics**

| Symbol | Parameter | Conditions(1) | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI1 clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 8 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI1 clock rise and fall time | Capacitive load: C = 30 pF | - | 30 | ns |
| $t_{su(NSS)}$(2) | NSS setup time | Slave mode | 4 x $1/f_{SYSCLK}$ | - | |
| $t_{h(NSS)}$(2) | NSS hold time | Slave mode | 80 | - | |
| $t_{w(SCKH)}$(2)<br>$t_{w(SCKL)}$(2) | SCK high and low time | Master mode,<br>$f_{MASTER}$ = 8 MHz, $f_{SCK}$= 4 MHz | 105 | 145 | |
| $t_{su(MI)}$(2)<br>$t_{su(SI)}$(2) | Data input setup time | Master mode | 30 | - | |
| | | Slave mode | 3 | - | |
| $t_{h(MI)}$(2)<br>$t_{h(SI)}$(2) | Data input hold time | Master mode | 15 | - | |
| | | Slave mode | 0 | - | |
| $t_{a(SO)}$(2)(3) | Data output access time | Slave mode | - | 3x $1/f_{SYSCLK}$ | |
| $t_{dis(SO)}$(2)(4) | Data output disable time | Slave mode | 30 | - | |
| $t_{v(SO)}$(2) | Data output valid time | Slave mode (after enable edge) | - | 60 | |
| $t_{v(MO)}$(2) | Data output valid time | Master mode (after enable edge) | - | 20 | |
| $t_{h(SO)}$(2) | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| $t_{h(MO)}$(2) | | Master mode (after enable edge) | 1 | - | |

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

**Figure 36. SPI1 timing diagram - master mode(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 41. Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)**

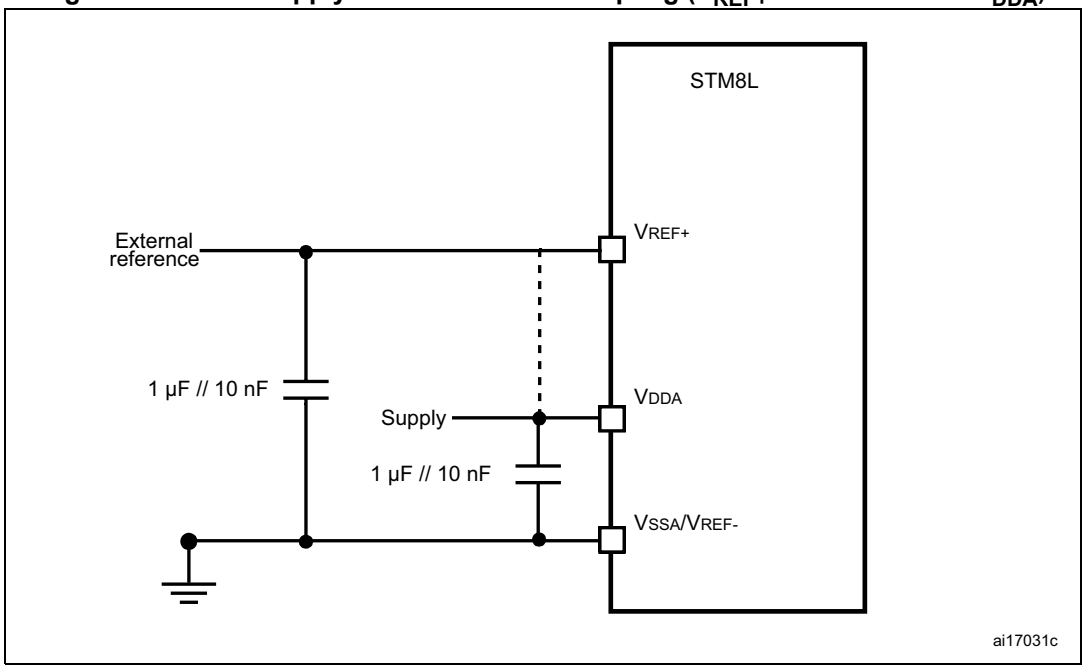
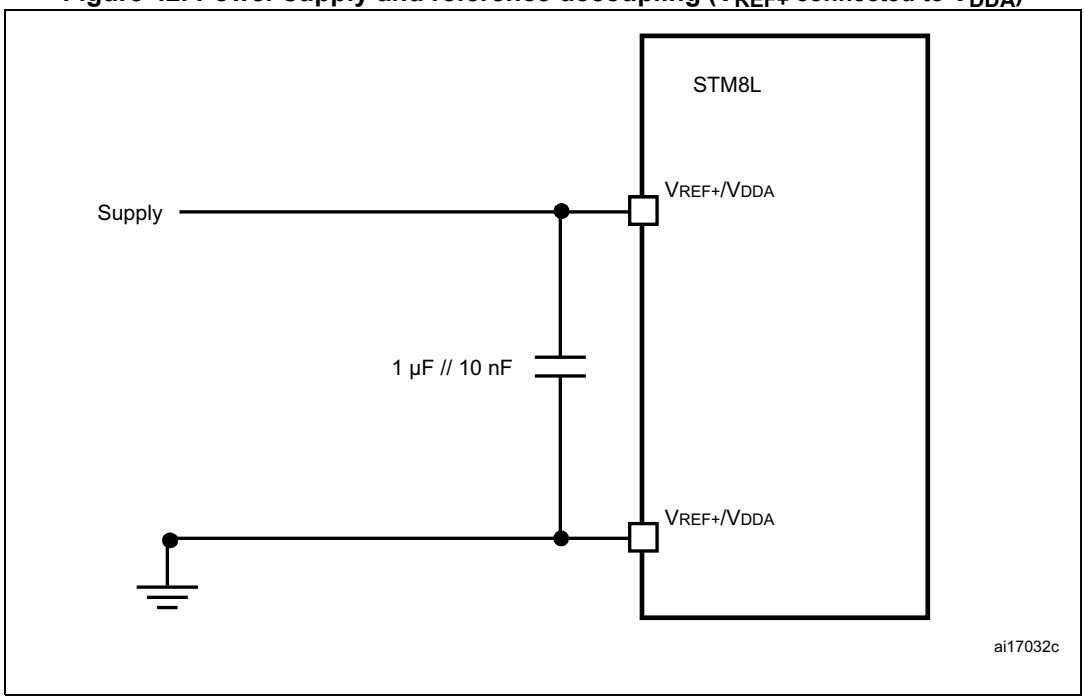


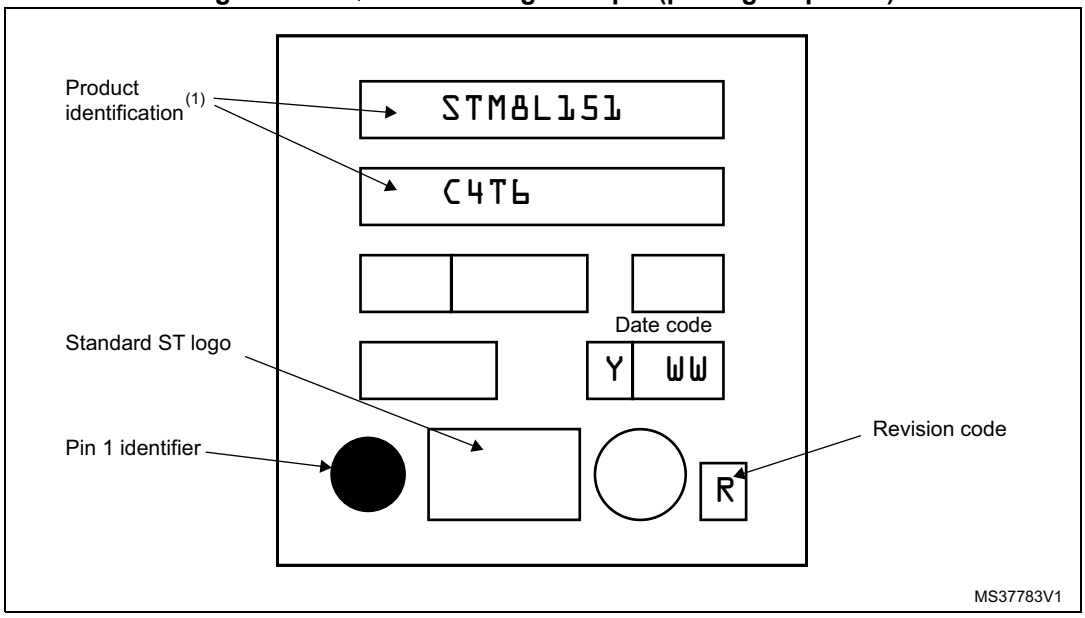

**Figure 42. Power supply and reference decoupling ($V_{REF+}$ connected to $V_{DDA}$)**



### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 45. LQFP48 marking example (package top view)**

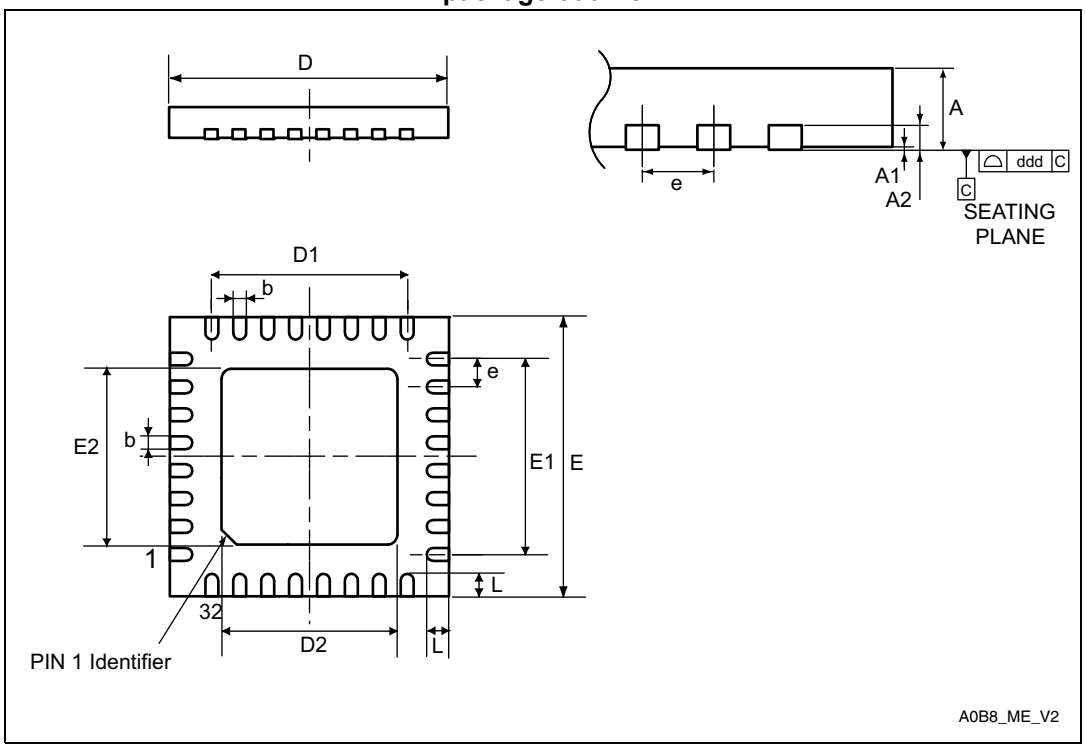



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Samples to run qualification activity.

## 10.5 UFQFPN32 package information

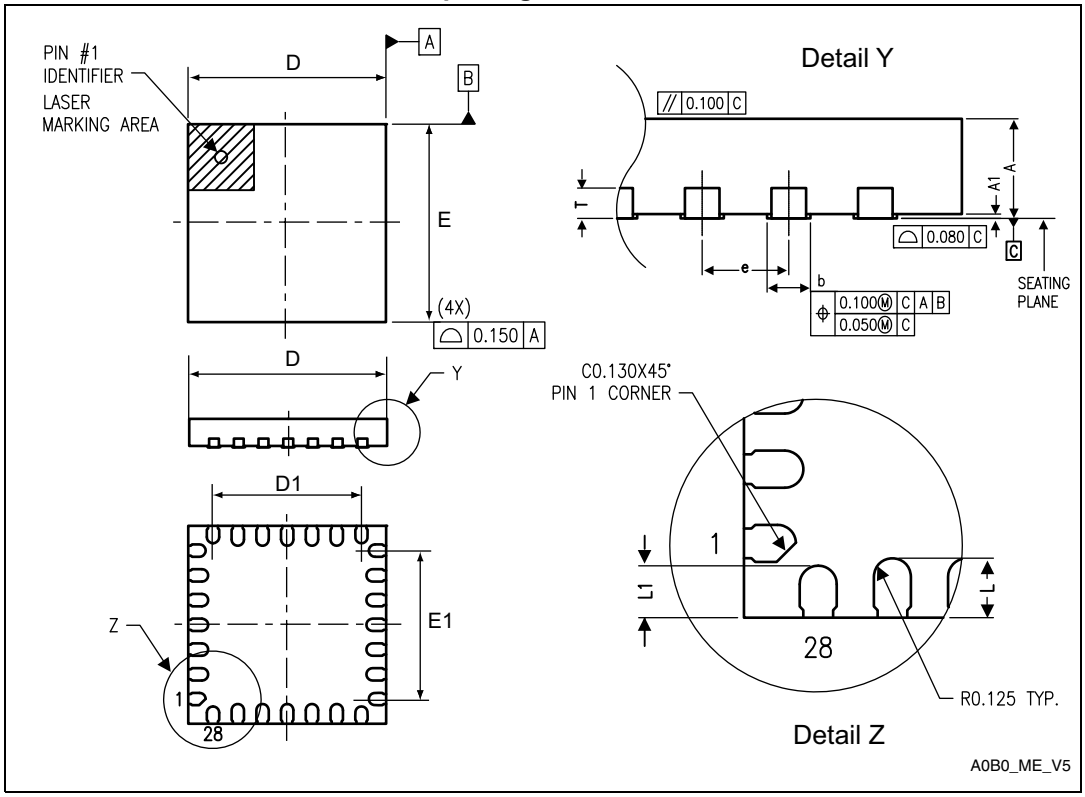
**Figure 52. UFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline**




1. Drawing is not to scale.

## 10.6 UFQFPN28 package information

**Figure 55. UFQFPN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline**




1. Drawing is not to scale.

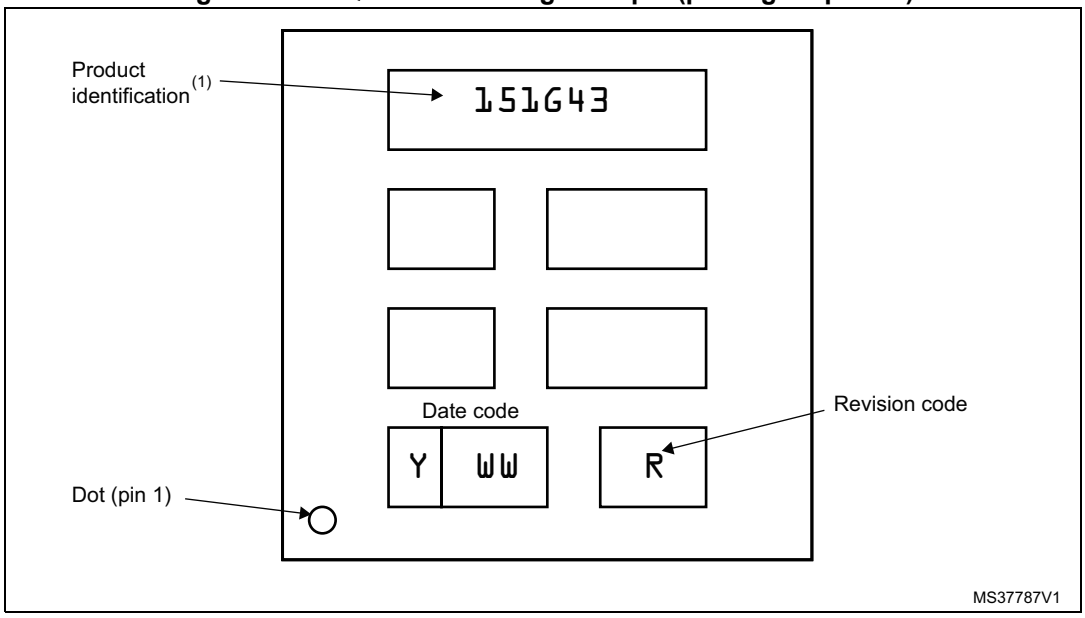
**Table 66. UFQFPN28 - 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data(1)**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | - | 0.000 | 0.050 | - | 0.0000 | 0.0020 |
| D | 3.900 | 4.000 | 4.100 | 0.1535 | 0.1575 | 0.1614 |
| D1 | 2.900 | 3.000 | 3.100 | 0.1142 | 0.1181 | 0.1220 |
| E | 3.900 | 4.000 | 4.100 | 0.1535 | 0.1575 | 0.1614 |
| E1 | 2.900 | 3.000 | 3.100 | 0.1142 | 0.1181 | 0.1220 |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| L1 | 0.250 | 0.350 | 0.450 | 0.0098 | 0.0138 | 0.0177 |
| T | - | 0.152 | - | - | 0.0060 | - |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 57. UFQFPN28 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

**Table 67. WLCSP28 - 28-pin, 1.703 x 2.841 mm, 0.4 mm pitch wafer level chip scale package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.540 | 0.570 | 0.600 | 0.0213 | 0.0224 | 0.0236 |
| A1 | - | 0.190 | - | - | 0.0075 | - |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| b[2] | 0.240 | 0.270 | 0.300 | 0.0094 | 0.0106 | 0.0118 |
| D | 1.668 | 1.703 | 1.738 | 0.0657 | 0.0670 | 0.0684 |
| E | 2.806 | 2.841 | 2.876 | 0.1105 | 0.1119 | 0.1132 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 1.200 | - | - | 0.0472 | - |
| e2 | - | 2.400 | - | - | 0.0945 | - |
| F | - | 0.251 | - | - | 0.0099 | - |
| G | - | 0.222 | - | - | 0.0087 | - |
| aaa | - | - | 0.100 | - | - | 0.0039 |
| bbb | - | - | 0.100 | - | - | 0.0039 |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| ddd | - | - | 0.050 | - | - | 0.0020 |
| eee | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

## Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

# 12 Revision history

**Table 69. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 06-Aug-2009 | 1 | Initial release |
| 10-Sep-2009 | 2 | Updated peripheral naming throughout document.<br>Added *Figure: STM8L151Cx 48-pin pinout (without LCD).*<br>Added capacitive sensing channels in *Features.*<br>Updated PA7, PC0 and PC1 in *Table: Medium density STM8L15x pin description.*<br>Changed CLK and REMAP register names.<br>Changed description of WDGHALT.<br>Added typical power consumption values in *Table 18* to *Table 26.*<br>Corrected VIH max value. |
| 11-Dec-2009 | 3 | Added WLCSP28 package<br>Modified *Figure: Memory map* and added 2 notes.<br>Modified Low power run mode in *Section: Low power modes.*<br>Added *Section: Unique ID.*<br>Modified *Table: Interrupt mapping* (added reserved area at address 0x00 8008)<br>Modified OPT4 option bits in *Table: Option byte addresses.*<br>*Table: Option byte description:* modified OPT0 description (“disable” instead of “enable”) and OPT1 description<br>Added OPTBL option bytes<br>Modified *Section: Electrical parameters.* |
| 02-Apr-2010 | 4 | Changed title of the document (STM8L151x4, STM8L151x6, STM8L152x4, STM8L152x6)<br>Changed pinout ($V_{SS1}$, $V_{DD1}$, $V_{SS2}$, $V_{DD\ 2}$ instead of $V_{SS}$, $V_{DD,}$ $V_{SSIO}$, $V_{DDIO}$<br>Changed packages<br>Changed first page<br>Modified note 1 in *Table: Medium density STM8L15x pin description.*<br>Added note to PA7, PC0, PC1 and PE0 in *Table: Medium density STM8L15x pin description.*<br>Modified *Figure: Memory map.*<br>Modified *Table: WLCSP28 – 28-pin wafer level chip scale package, package mechanical data* (min and max columns swapped)<br>Modified *Figure: WLCSP28 – 28-pin wafer level chip scale package, package outline* (A1 ball location)<br>Renamed Rm, Lm and Cm<br>EXTI_CONF replaced with EXTI_CONF1 in *Table: General hardware register map.*<br>Updated *Section: Electrical parameters.* |