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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l152c4t6

3.17 Communication interfaces

3.17.1 SPI

The serial peripheral interface (SPI1) provides half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s (f_{SYSCLK}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 can be served by the DMA1 Controller.

3.17.2 I²C

The I^2C bus interface (I^2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz.
- 7-bit and 10-bit addressing modes.
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.17.3 USART

The USART interface (USART1) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- SmartCard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1 can be served by the DMA1 Controller.

3.18 Infrared (IR) interface

The medium-density STM8L151x4/6 and STM8L152x4/6 devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	16	-	-	PB3/*[TIM2_ETR]*(4)/ TIM1_CH2N/LCD_SEG13(2)/ADC1_IN15/ COMP1_INP	I/O	TT(3)	**X**	X	X	HS	X	X	**Port B3**	*[Timer 2 - external trigger]* / Timer 1 inverted channel 2 / LCD segment 13 / ADC1_IN15 / Comparator 1 positive input
-	-	15	E2	PB3/*[TIM2_ETR]*(4)/ TIM1_CH1N/ LCD_SEG13(2)/ ADC1_IN15/RTC_ALARM /COMP1_INP	I/O	TT(3)	**X**	X	X	HS	X	X	**Port B3**	*[Timer 2 - external trigger]* / Timer 1 inverted channel 1/ LCD segment 13 / ADC1_IN15 / RTC alarm/ Comparator 1 positive input
28	-	-	-	PB4(6)/*[SPI1_NSS]*(4)/ LCD_SEG14(2)/ ADC1_IN14/COMP1_INP	I/O	TT(3)	**X**(6)	X(6)	X	HS	X	X	**Port B4**	*[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14 / Comparator 1 positive input
-	17	16	D2	PB4(6)/*[SPI1_NSS]*(4)/ LCD_SEG14(2)/ ADC1_IN14/ COMP1_INP/DAC_OUT	I/O	TT(3)	**X**(6)	X(6)	X	HS	X	X	**Port B4**	*[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14 / DAC output / Comparator 1 positive input
29	-	-	-	PB5/*[SPI1_SCK]*(4)/ LCD_SEG15(2)/ ADC1_IN13/COMP1_INP	I/O	TT(3)	**X**	X	X	HS	X	X	**Port B5**	*[SPI1 clock]* / LCD segment 15 / ADC1_IN13 / Comparator 1 positive input
-	18	17	D1	PB5/*[SPI1_SCK]*(4)/ LCD_SEG15(2)/ ADC1_IN13/DAC_OUT/ COMP1_INP	I/O	TT(3)	**X**	X	X	HS	X	X	**Port B5**	*[SPI1 clock]* / LCD segment 15 / ADC1_IN13 / DAC output/ Comparator 1 positive input

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 501E to 0x00 5049	Reserved area (28 bytes)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50D0 to 0x00 50D2	Reserved area (3 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 bytes)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to 0x00 513F	Reserved area (76 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 Slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_DER	TIM3 DMA1 request enable register	0x00
0x00 5285		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5286		TIM3_SR1	TIM3 status register 1	0x00
0x00 5287		TIM3_SR2	TIM3 status register 2	0x00
0x00 5288		TIM3_EGR	TIM3 event generation register	0x00
0x00 5289		TIM3_CCMR1	TIM3 Capture/Compare mode register 1	0x00
0x00 528A		TIM3_CCMR2	TIM3 Capture/Compare mode register 2	0x00
0x00 528B		TIM3_CCER1	TIM3 Capture/Compare enable register 1	0x00
0x00 528C		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528D		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528E		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528F		TIM3_ARRH	TIM3 Auto-reload register high	0xFF
0x00 5290		TIM3_ARRL	TIM3 Auto-reload register low	0xFF
0x00 5291		TIM3_CCR1H	TIM3 Capture/Compare register 1 high	0x00
0x00 5292		TIM3_CCR1L	TIM3 Capture/Compare register 1 low	0x00
0x00 5293		TIM3_CCR2H	TIM3 Capture/Compare register 2 high	0x00
0x00 5294		TIM3_CCR2L	TIM3 Capture/Compare register 2 low	0x00
0x00 5295		TIM3_BKR	TIM3 break register	0x00
0x00 5296		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5297 to 0x00 52AF	Reserved area (25 bytes)			

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option bytes can also be modified 'on the fly' by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 12. Option byte addresses

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved										0x00
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x00
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

In the following table, data is based on characterization results, unless otherwise specified.

Table 23. Total current consumption in Low power wait mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions(1)			Typ	Max	Unit
$I_{DD(LPW)}$	Supply current in Low power wait mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	3	3.3	µA
				T_A = 55 °C	3.3	3.6	
				T_A = 85 °C	4.4	5	
				T_A = 105 °C	6.7	8	
				T_A = 125 °C	11	14	
			with TIM2 active(2)	T_A = -40 °C to 25 °C	3.4	3.7	
				T_A = 55 °C	3.7	4	
				T_A = 85 °C	4.8	5.4	
				T_A = 105 °C	7	8.3	
				T_A = 125 °C	11.3	14.5	
		LSE external clock(3) (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	2.35	2.7	
				T_A = 55 °C	2.42	2.82	
				T_A = 85 °C	3.10	3.71	
				T_A = 105 °C	4.36	5.7	
				T_A = 125 °C	7.20	11	
			with TIM2 active (2)	T_A = -40 °C to 25 °C	2.46	2.75	
				T_A = 55 °C	2.50	2.81	
				T_A = 85 °C	3.16	3.82	
				T_A = 105 °C	4.51	5.9	
				T_A = 125 °C	7.28	11	

1. No floating I/Os.
2. Timer 2 clock enabled and counter is running.
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*.

Table 25. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal

Symbol	Parameter	Condition(1)		Typ	Unit
$I_{DD(AH)}$ (2)	Supply current in Active-halt mode	V_{DD} = 1.8 V	LSE	1.15	µA
			LSE/32(3)	1.05	
		V_{DD} = 3 V	LSE	1.30	
			LSE/32(3)	1.20	
		V_{DD} = 3.6 V	LSE	1.45	
			LSE/32(3)	1.35	

1. No floating I/O, unless otherwise specified.
2. Based on measurements on bench with 32.768 kHz external crystal oscillator.
3. RTC clock is LSE divided by 32.

In the following table, data is based on characterization results, unless otherwise specified.

Table 26. Total current consumption and timing in Halt mode at V_{DD} = 1.65 to 3.6 V

Symbol	Parameter	Condition(1)	Typ	Max	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (Ultra-low-power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	350	1400(2)	nA
		T_A = 55 °C	580	2000	
		T_A = 85 °C	1160	2800(2)	
		T_A = 105 °C	2560	6700(2)	
		T_A = 125 °C	4.4	13(2)	µA
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)	-	2.4	-	mA
$t_{WU\_HSI(Halt)}$ (3)(4)	Wakeup time from Halt to Run mode (using HSI)	-	4.7	7	µs
$t_{WU\_LSI(Halt)}$ (3)(4)	Wakeup time from Halt mode to Run mode (using LSI)	-	150	-	µs

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. Tested in production.
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.
4. Wakeup time until start of interrupt vector fetch.
The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.

Current consumption of on-chip peripherals

Table 27. Peripheral current consumption

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)		13	µA/MHz
$I_{DD(TIM2)}$	TIM2 supply current (1)		8	
$I_{DD(TIM3)}$	TIM3 supply current (1)		8	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (2)		6	
$I_{DD(SPI1)}$	SPI1 supply current (2)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (2)		5	
$I_{DD(DMA1)}$	DMA1 supply current(2)		3	
$I_{DD(WWDG)}$	WWDG supply current(2)		2	
$I_{DD(ALL)}$	Peripherals ON(3)		44	µA/MHz
$I_{DD(ADC1)}$	ADC1 supply current(4)		1500	µA
$I_{DD(DAC)}$	DAC supply current(5)		370	µA
$I_{DD(COMP1)}$	Comparator 1 supply current(6)		0.160	µA
$I_{DD(COMP2)}$	Comparator 2 supply current(6)	Slow mode	2	
		Fast mode	5	
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (7)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (7)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, USART1, SPI1, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.
5. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of V_{DD} /2. Floating DAC output.
6. Data based on a differential I_{DD} measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
7. Including supply current of internal reference voltage.

9.3.6 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

Table 37. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on true open-drain pins (PC0 and PC1)	-5	+0	mA
	Injected current on all five-volt tolerant (FT) pins	-5	+0	
	Injected current on all 3.6 V tolerant (TT) pins	-5	+0	
	Injected current on any other pin	-5	+5	

9.3.7 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Figure 23. Typical pull-up resistance R_{PU} vs V_{DD} with $V_{IN}=V_{SS}$

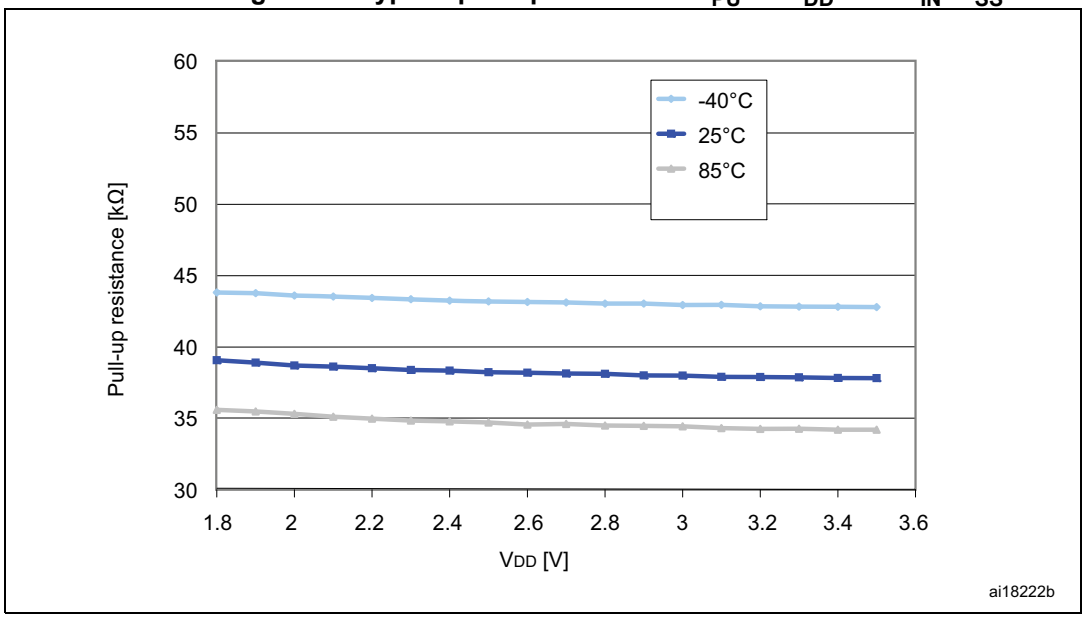
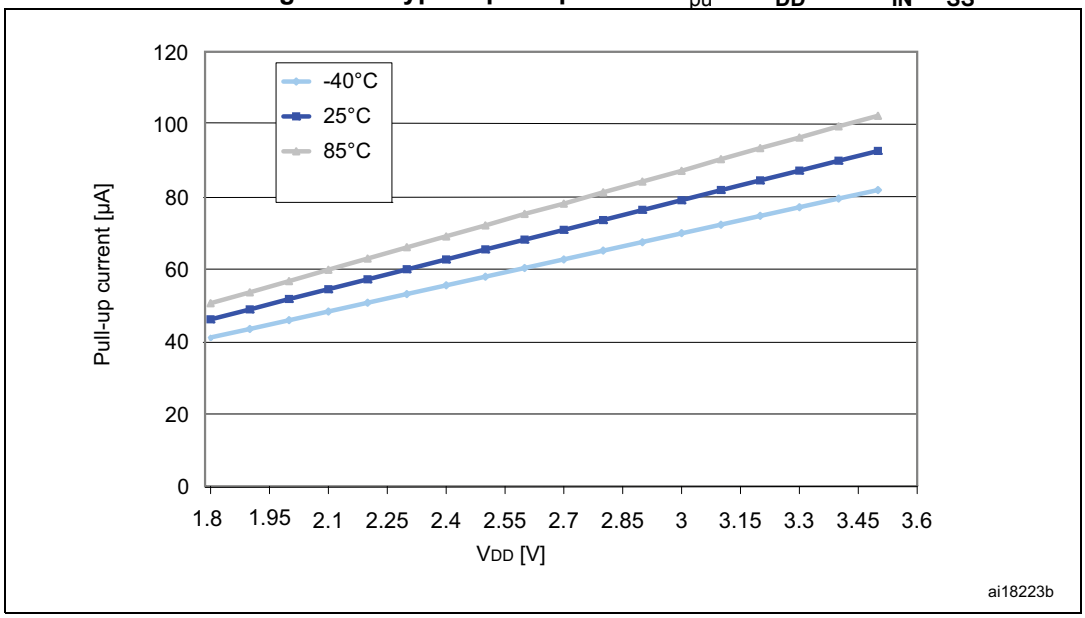


Figure 24. Typical pull-up current I_{pu} vs V_{DD} with $V_{IN}=V_{SS}$



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
High sink	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	V
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	V
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	V
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 40. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

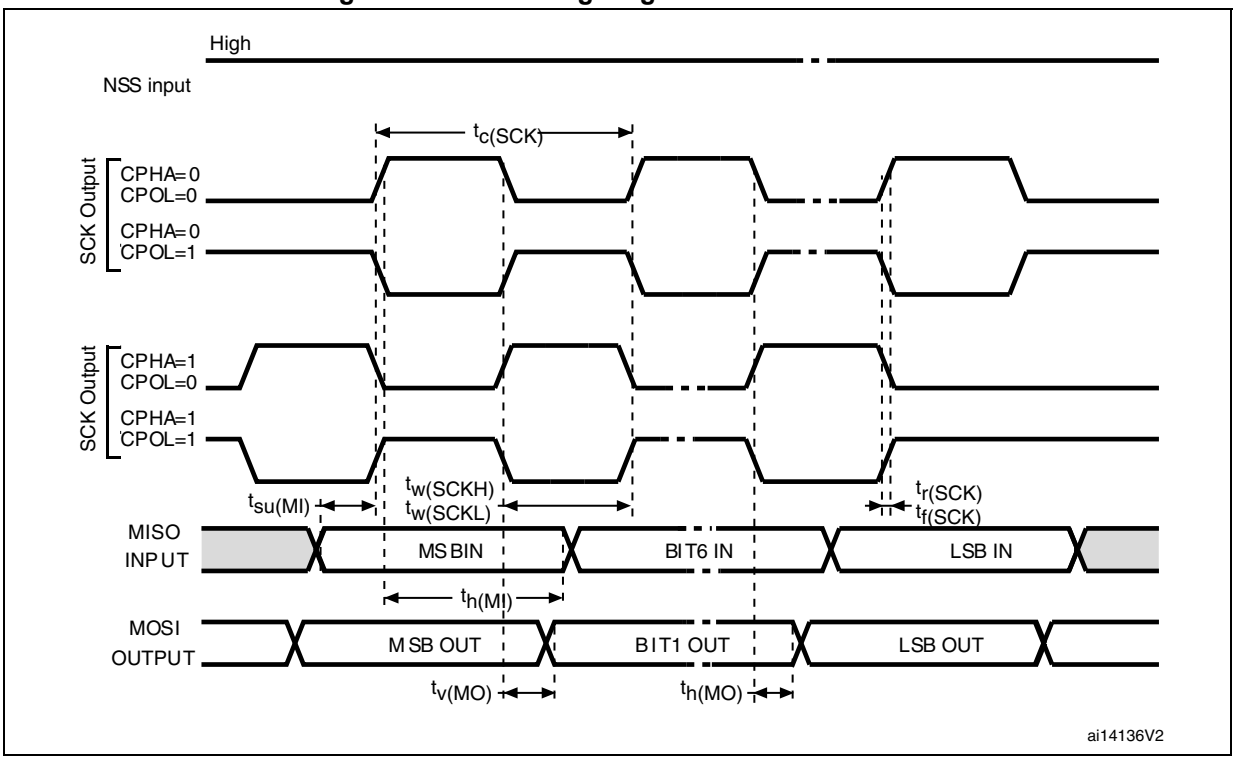
1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 41. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Figure 36. SPI1 timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

9.3.11 Temperature sensor

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 47. TS characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{90}(1)	Sensor reference voltage at 90°C ±5 °C,	0.580	0.597	0.614	V
T_L	V_{SENSOR} linearity with temperature	-	±1	±2	°C
Avg_slope (2)	Average slope	1.59	1.62	1.65	mV/°C
$I_{DD(TEMP)}$(2)	Consumption	-	3.4	6	µA
T_{START}(2)(3)	Temperature sensor startup time	-	-	10	µs
T_{S_TEMP}(2)	ADC sampling time when reading the temperature sensor	10	-	-	µs

1. Tested in production at V_{DD} = 3 V ±10 mV. The 8 LSB of the V_{90} ADC conversion result are stored in the TS_Factory_CONV_V90 byte.
2. Data guaranteed by design.
3. Defined for ADC output reaching its final value ±1/2LSB.

9.3.12 Comparator characteristics

In the following table, data is guaranteed by design, not tested in production, unless otherwise specified.

Table 48. Comparator 1 characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	1.65	-	3.6	V
T_A	Temperature range	-40	-	125	°C
R_{400K}	R_{400K} value	300	400	500	kΩ
R_{10K}	R_{10K} value	7.5	10	12.5	
V_{IN}	Comparator 1 input voltage range	0.6	-	V_{DDA}	V
V_{REFINT}	Internal reference voltage(2)	1.202	1.224	1.242	
t_{START}	Comparator startup time	-	7	10	µs
t_d	Propagation delay(3)	-	3	10	
V_{offset}	Comparator offset error	-	±3	±10	mV
I_{COMP1}	Current consumption(4)	-	160	260	nA

1. Based on characterization.
2. Tested in production at V_{DD} = 3 V ±10 mV.
3. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
4. Comparator consumption only. Internal reference voltage not included.

In the following three tables, data is guaranteed by characterization result, not tested in production.

Table 54. ADC1 accuracy with V_{DDA} = 3.3 V to 2.5 V

Symbol	Parameter	Conditions	Typ	Max	Unit
DNL	Differential non linearity	f_{ADC} = 16 MHz	1	1.6	LSB
		f_{ADC} = 8 MHz	1	1.6	
		f_{ADC} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC} = 16 MHz	1.2	2	
		f_{ADC} = 8 MHz	1.2	1.8	
		f_{ADC} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC} = 16 MHz	2.2	3.0	
		f_{ADC} = 8 MHz	1.8	2.5	
		f_{ADC} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC} = 16 MHz	1.5	2	LSB
		f_{ADC} = 8 MHz	1	1.5	
		f_{ADC} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC} = 16 MHz	1	1.5	
		f_{ADC} = 8 MHz			
		f_{ADC} = 4 MHz			

Table 55. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	LSB
TUE	Total unadjusted error	2	4	LSB
Offset	Offset error	1	2	LSB
Gain	Gain error	1.5	3	LSB

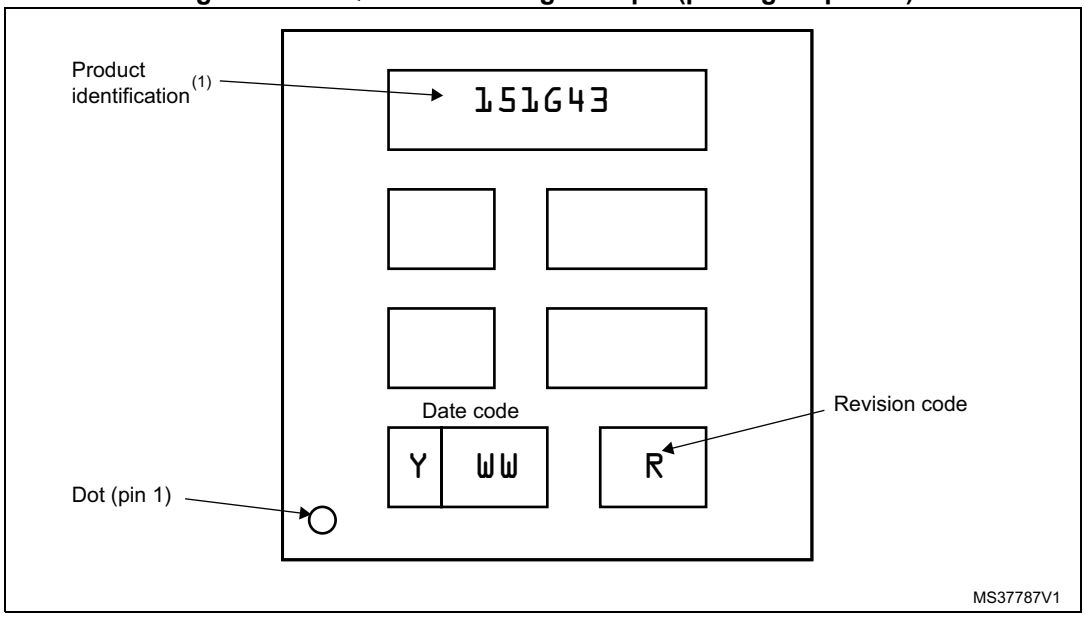
Table 56. ADC1 accuracy with $V_{DDA} = V_{REF}^+$ = 1.8 V to 2.4 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	LSB
TUE	Total unadjusted error	3	5	LSB
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 57. UFQFPN28 marking example (package top view)

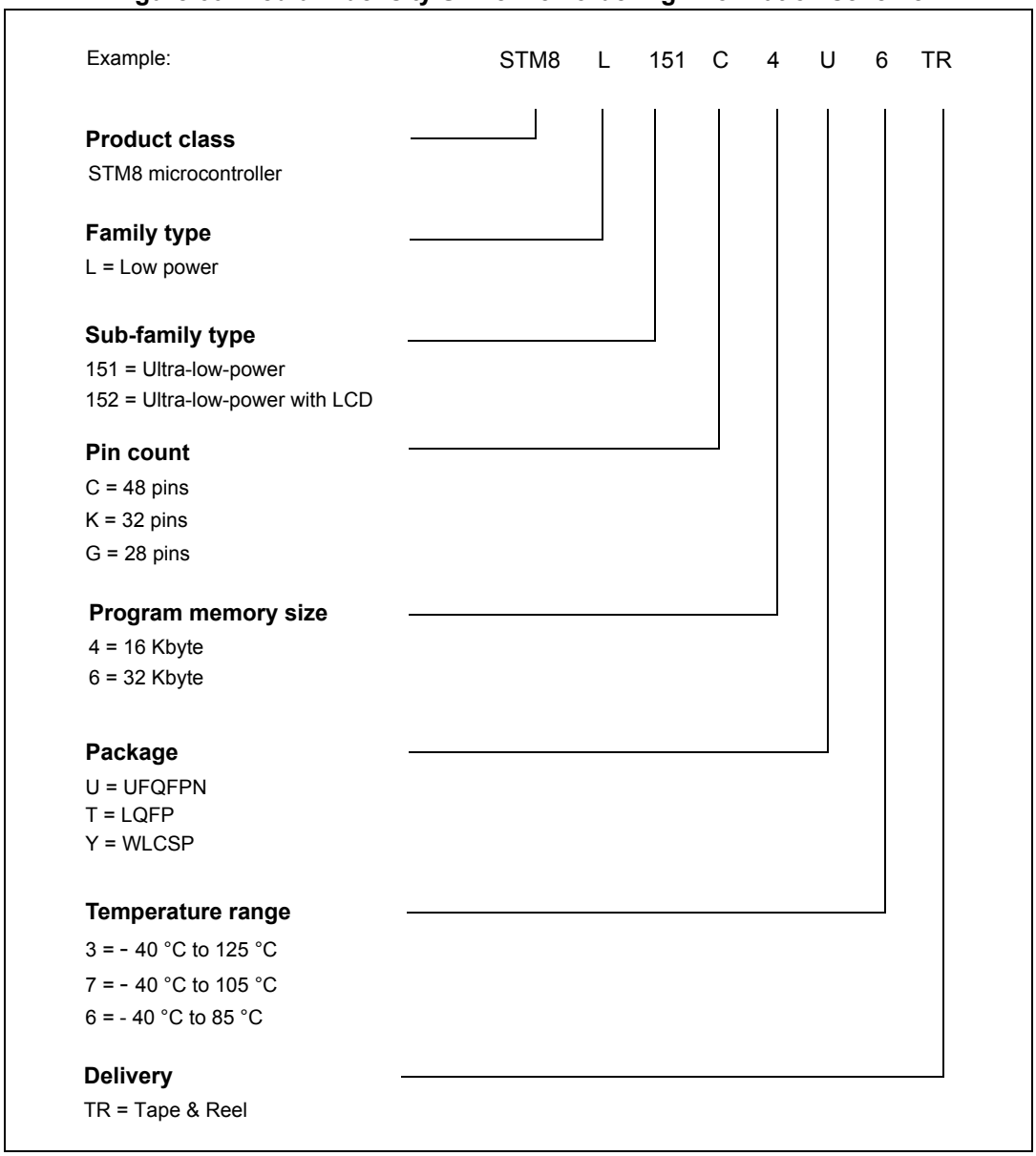


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

11 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Figure 60. Medium-density STM8L15x ordering information scheme



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please contact the ST sales office nearest to you.

12 Revision history

Table 69. Document revision history

Date	Revision	Changes
06-Aug-2009	1	Initial release
10-Sep-2009	2	Updated peripheral naming throughout document. Added *Figure: STM8L151Cx 48-pin pinout (without LCD).* Added capacitive sensing channels in *Features.* Updated PA7, PC0 and PC1 in *Table: Medium density STM8L15x pin description.* Changed CLK and REMAP register names. Changed description of WDGHALT. Added typical power consumption values in *Table 18* to *Table 26.* Corrected VIH max value.
11-Dec-2009	3	Added WLCSP28 package Modified *Figure: Memory map* and added 2 notes. Modified Low power run mode in *Section: Low power modes.* Added *Section: Unique ID.* Modified *Table: Interrupt mapping* (added reserved area at address 0x00 8008) Modified OPT4 option bits in *Table: Option byte addresses.* *Table: Option byte description:* modified OPT0 description (“disable” instead of “enable”) and OPT1 description Added OPTBL option bytes Modified *Section: Electrical parameters.*
02-Apr-2010	4	Changed title of the document (STM8L151x4, STM8L151x6, STM8L152x4, STM8L152x6) Changed pinout (V_{SS1}, V_{DD1}, V_{SS2}, $V_{DD\ 2}$ instead of V_{SS}, $V_{DD,}$ V_{SSIO}, V_{DDIO} Changed packages Changed first page Modified note 1 in *Table: Medium density STM8L15x pin description.* Added note to PA7, PC0, PC1 and PE0 in *Table: Medium density STM8L15x pin description.* Modified *Figure: Memory map.* Modified *Table: WLCSP28 – 28-pin wafer level chip scale package, package mechanical data* (min and max columns swapped) Modified *Figure: WLCSP28 – 28-pin wafer level chip scale package, package outline* (A1 ball location) Renamed Rm, Lm and Cm EXTI_CONF replaced with EXTI_CONF1 in *Table: General hardware register map.* Updated *Section: Electrical parameters.*

Table 69. Document revision history (continued)

Date	Revision	Changes
11-Mar-2011	6 cont'd	Modified OPT1 and OPT4 description in *Table: Option byte description.* Updated *Section: Electrical parameters* "standard I/Os" replaced with "high sink I//Os". Updated $R_{HN\ and}$ R_{HN} descriptions in *Table: LCD characteristics.* Added Tape & Reel option to *Figure: Medium density STM8L15x ordering information scheme*.
06-Sep-2011	7	*Features:* updated bullet point concerning capacitive sensing channels. *Section: Low power modes:* updated Wait mode and Halt mode definitions. *Section: Clock management:* added 'kHz' to 32.768 in the 'System clock sources bullet point'. *Section: System configuration controller and routing interface:* replaced last sentence concerning management of charge transfer acquisition sequence. Added *Section: Touchsensing* *Section Development support:* updated the *Bootloader.* *Table: Medium density STM8L15x pin description:* added LQFP32 to second column (same pinout as UFQFPN32); "Timer X - trigger" replaced by "Timer X - external trigger"; added note at the end of this table concerning the slope control of all GPIO pins. *Table: Interrupt mapping:* merged footnotes 1 and 2; updated some of the source blocks and descriptions. *Section: Option bytes*: replaced PM0051 by PM0054 and UM0320 by UM0470. *Table: Option byte description:* replaced the factory default setting (0xAA) for OPT0. *NRST pin:* updated text above the *Figure*; updated *Figure: Recommended NRST pin configuration*. *Table: TS characteristics:* removed typ and max values for the parameter T_{S_TEMP}; added min value for same. *Table: Comparator 1 characteristics:* added typ value for 'Comparator offset error'; added footnote *1.* *Table: Comparator 2 characteristics:* updated t_{START}, t_{dslow}, t_{dfast}, V_{offset}, I_{COMP2}; added footnotes *1.* and *3.* *Table: DAC characteristics:* updated max value for DAC_OUT voltage (DACOUT buffer ON). *Section: 12-bit ADC1 characteristics:* updated. Replaced *Figure: UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline* and *Figure: UFQFPN48 7 x 7 mm recommended footprint (dimensions in mm)*. *Figure: Medium density STM8L15x ordering information scheme*: removed 'TR = Tape & Reel".

Table 69. Document revision history (continued)

Date	Revision	Changes
21-Apr-2015	14	Added: – *Figure 45: LQFP48 marking example (package top view)*, – *Figure 48: UFQFPN48 marking example (package top view)*, – *Figure 51: LQFP32 marking example (package top view)*, – *Figure 54: UFQFPN32 marking example (package top view)*, – *Figure 57: UFQFPN28 marking example (package top view)*, – *Figure 59: WLCSP28 marking example (package top view)*.
07-Apr-2017	15	Changed symbol V_{125} to V_{90} in *Table 47: TS characteristics* and updated related Min/Typ/Max values. Updated *Section 9.2: Absolute maximum ratings*. Updated table notes for *Table 30*, *Table 31*, *Table 32*, *Table 33*, *Table 34*, *Table 36*, *Table 38*, *Table 42*, *Table 43*, *Table 46*, *Table 47*, *Table 48*, *Table 49*, *Table 53*, *Table 57*, and *Table 60*. Updated device marking paragraphs in *Section 10.2*, *Section 10.3*, *Section 10.4*, *Section 10.5*, *Section 10.6*, and *Section 10.7*.