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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l152c4t6tr

Note: ADC1 can be served by DMA1.

3.10 Digital-to-analog converter (DAC)

- 12-bit DAC with output buffer
- Synchronized update capability using TIM4
- DMA capability
- External triggers for conversion
- Input reference voltage V_{REF+} for better resolution

Note: DAC can be served by DMA1.

3.11 Ultra-low-power comparators

The medium-density STM8L151x4/6 and STM8L152x4/6 embed two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage or internal reference voltage sub multiple (1/4, 1/2, 3/4)

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC and the internal reference voltage V_{REFINT}. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (*Section 3.13: Touch sensing*).

3.13 Touch sensing

Medium-density STM8L151x4/6 and STM8L152x4/6 devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (example, glass, plastic). The capacitive variation introduced by a finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. In medium-density STM8L151x4/6

Figure 6. STM8L151G4, STM8L151G6 WLCSP28 package pinout

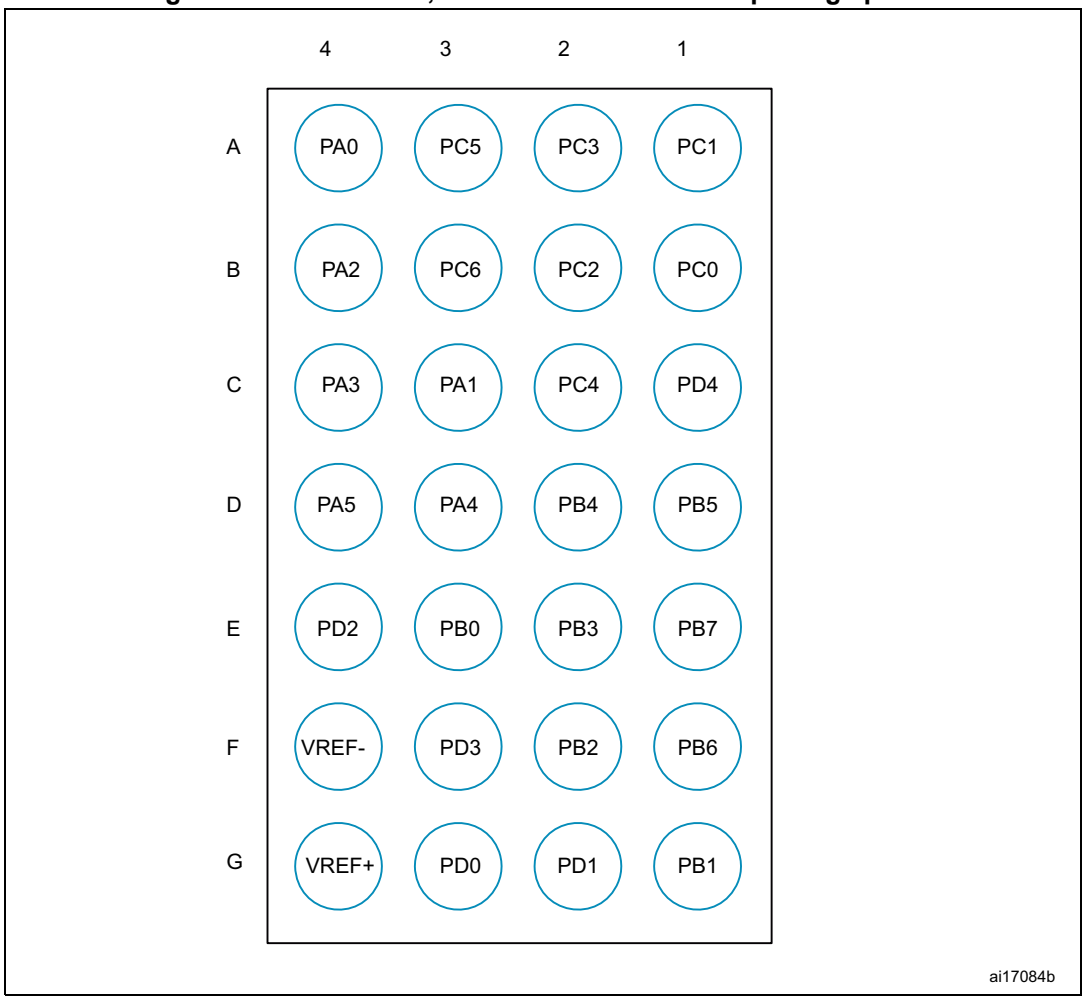


Figure 7. STM8L152C4, STM8L152C6 48-pin pinout (with LCD)

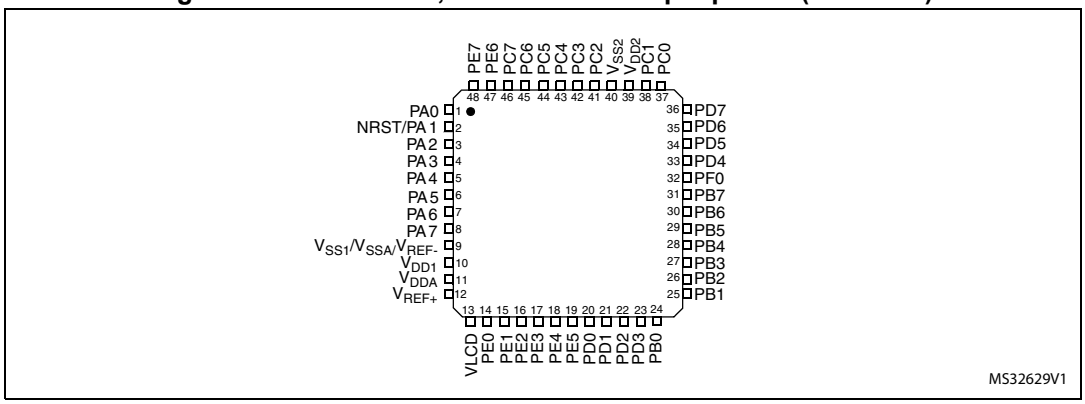
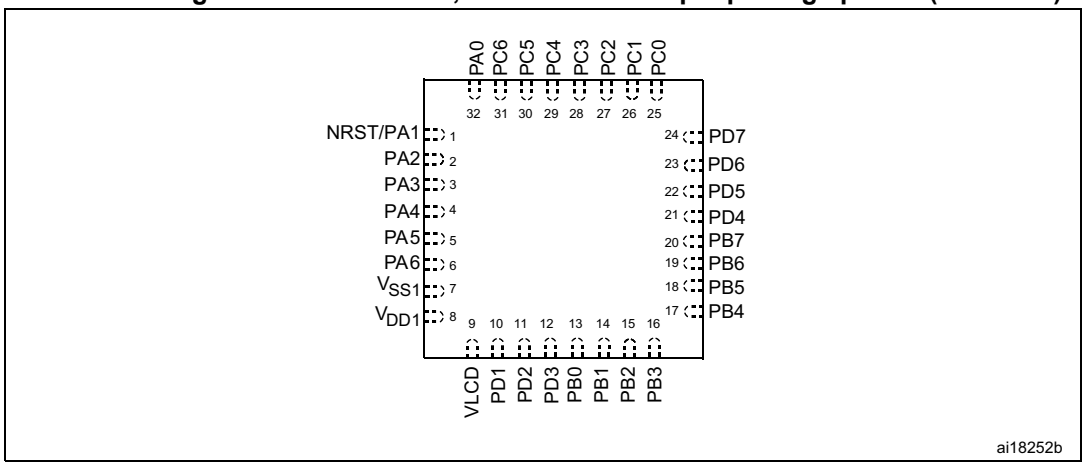


Figure 8. STM8L152K4, STM8L152K6 32-pin package pinout (with LCD)



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
44	30	26	A3	PC5/OSC32_IN /*[SPI1_NSS]*(4)/ *[USART1_TX]*(4)	I/O		**X**	X	X	HS	X	X	**Port C5**	LSE oscillator input / *[SPI1 master/slave select] / [USART1 transmit]*
45	31	27	B3	PC6/OSC32_OUT/ *[SPI1_SCK]*(4)/ *[USART1_RX]*(4)	I/O		**X**	X	X	HS	X	X	**Port C6**	LSE oscillator output / *[SPI1 clock] / [USART1 receive]*
46	-	-	-	PC7/LCD_SEG25(2)/ ADC1_IN3/COMP2_INM/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port C7**	LCD segment 25 /ADC1_IN3/ Comparator negative input / Comparator 1 positive input
20	-	8	G3	PD0/TIM3_CH2/ *[ADC1_TRIG]*(4)/ LCD_SEG7(2)/ADC1_IN22/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / LCD segment 7 / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input
-	9	-	-	PD0/TIM3_CH2/ *[ADC1_TRIG]*(4)/ ADC1_IN22/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D0(8)**	Timer 3 - channel 2 / *[ADC1_Trigger]* / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input
21	-	-	-	PD1/TIM3_ETR/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - external trigger / LCD_COM3 / ADC1_IN21 / comparator 2 positive input / Comparator 1 positive input
-	10	-	-	PD1/TIM1_CH3N/[*TIM3_ETR*](4)/ LCD_COM3(2)/ ADC1_IN21/COMP2_INP/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port D1**	*[Timer 3 - external trigger]/* TIM1 inverted channel 3 / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 501E to 0x00 5049	Reserved area (28 bytes)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	LCD	LCD_CR1	LCD control register 1	0x00
0x00 5401		LCD_CR2	LCD control register 2	0x00
0x00 5402		LCD_CR3	LCD control register 3	0x00
0x00 5403		LCD_FRQ	LCD frequency selection register	0x00
0x00 5404		LCD_PM0	LCD Port mask register 0	0x00
0x00 5405		LCD_PM1	LCD Port mask register 1	0x00
0x00 5406		LCD_PM2	LCD Port mask register 2	0x00
0x00 5407		LCD_PM3	LCD Port mask register 3	0x00
0x00 5408 to 0x00 540B	LCD	Reserved area (4 bytes)		
0x00 540C		LCD_RAM0	LCD display memory 0	0x00
0x00 540D		LCD_RAM1	LCD display memory 1	0x00
0x00 540E		LCD_RAM2	LCD display memory 2	0x00
0x00 540F		LCD_RAM3	LCD display memory 3	0x00
0x00 5410		LCD_RAM4	LCD display memory 4	0x00
0x00 5411		LCD_RAM5	LCD display memory 5	0x00
0x00 5412		LCD_RAM6	LCD display memory 6	0x00
0x00 5413		LCD_RAM7	LCD display memory 7	0x00
0x00 5414		LCD_RAM8	LCD display memory 8	0x00
0x00 5415		LCD_RAM9	LCD display memory 9	0x00
0x00 5416		LCD_RAM10	LCD display memory 10	0x00
0x00 5417		LCD_RAM11	LCD display memory 11	0x00
0x00 5418		LCD_RAM12	LCD display memory 12	0x00
0x00 5419		LCD_RAM13	LCD display memory 13	0x00
0x00 541A to 0x00 542F	Reserved area (22 bytes)			

Table 13. Option byte description

Option byte No.	Option description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Disable readout protection (write access via SWIM protocol) Refer to Readout protection section in the STM8L15x and STM8L16x reference manual (RM0031).
OPT1	**UBC[7:0]** Size of the user boot code area 0x00: no UBC 0x01: the UBC contains only the interrupt vectors. 0x02: Page 0 and 1 reserved for the UBC and read/write protected. Page 0 contains only the interrupt vectors. 0x03 - Page 0 to 2 reserved for UBC, memory write-protected 0xFF - Page 0 to 254 reserved for UBC, memory write-protected Refer to User boot code section in the STM8L15x and STM8L16x reference manual (RM0031).
OPT2	Reserved
OPT3	**IWDG_HW:** Independent watchdog 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: Independent window watchdog off on Halt/Active-halt 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode
	WWDG_HW: Window watchdog 0: Window watchdog activated by software 1: Window watchdog activated by hardware
	WWDG_HALT: Window window watchdog reset on Halt/Active-halt 0: Window watchdog stopped in Halt mode 1: Window watchdog generates a reset when MCU enters Halt mode
OPT4	**HSECNT**: Number of HSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles
	LSECNT: Number of LSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles Refer to *Table 32: LSE oscillator characteristics on page 84*.

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics is indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

9.1.2 Typical values

Unless otherwise specified, typical data is based on T_A = 25 °C, V_{DD} = 3 V. It is given only as design guidelines and is not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

Figure 10. Pin loading conditions

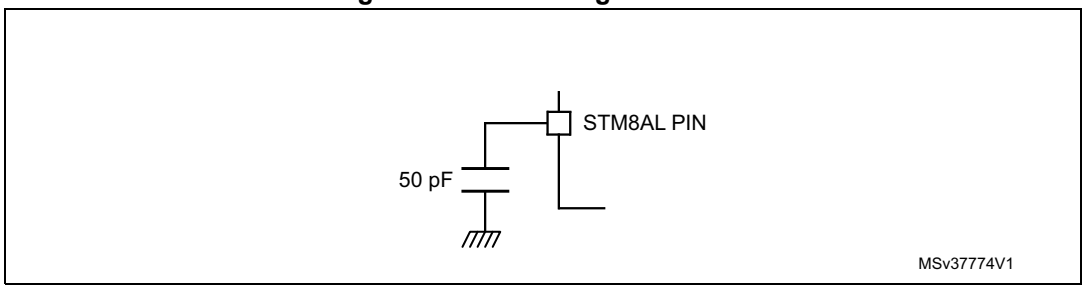


Table 20. Total current consumption in Run mode

Symbol	Parameter	Conditions(1)			Typ	Max				Unit
						55 °C	85 °C(2)	105°C(3)	125 °C(4)	
$I_{DD(RUN)}$	Supply current in run mode(5)	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)(6)	f_{CPU} = 125 kHz	0.39	0.47	0.49	0.52	0.55	mA
				f_{CPU} = 1 MHz	0.48	0.56	0.58	0.61	0.65	
				f_{CPU} = 4 MHz	0.75	0.84	0.86	0.91	0.99	
				f_{CPU} = 8 MHz	1.10	1.20	1.25	1.31	1.40	
				f_{CPU} = 16 MHz	1.85	1.93	2.12(8)	2.29(8)	2.36(8)	
			HSE external clock ($f_{CPU}=f_{HSE}$)(7)	f_{CPU} = 125 kHz	0.05	0.06	0.09	0.11	0.12	
				f_{CPU} = 1 MHz	0.18	0.19	0.20	0.22	0.23	
				f_{CPU} = 4 MHz	0.55	0.62	0.64	0.71	0.77	
				f_{CPU} = 8 MHz	0.99	1.20	1.21	1.22	1.24	
				f_{CPU} = 16 MHz	1.90	2.22	2.23(8)	2.24(8)	2.28(8)	
			LSI RC osc. (typ. 38 kHz)	$f_{CPU} = f_{LSI}$	0.040	0.045	0.046	0.048	0.050	
			LSE external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.035	0.040	0.048(8)	0.050	0.062	
$I_{DD(RUN)}$	Supply current in Run mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI RC osc.(9)	f_{CPU} = 125 kHz	0.43	0.55	0.56	0.58	0.62	mA
				f_{CPU} = 1 MHz	0.60	0.77	0.80	0.82	0.87	
				f_{CPU} = 4 MHz	1.11	1.34	1.37	1.39	1.43	
				f_{CPU} = 8 MHz	1.90	2.20	2.23	2.31	2.40	
				f_{CPU} = 16 MHz	3.8	4.60	4.75	4.87	4.88	
			HSE external clock ($f_{CPU}=f_{HSE}$) (7)	f_{CPU} = 125 kHz	0.30	0.36	0.39	0.44	0.47	
				f_{CPU} = 1 MHz	0.40	0.50	0.52	0.55	0.56	
				f_{CPU} = 4 MHz	1.15	1.31	1.40	1.45	1.48	
				f_{CPU} = 8 MHz	2.17	2.33	2.44	2.56	2.77	
				f_{CPU} = 16 MHz	4.0	4.46	4.52	4.59	4.77	
			LSI RC osc.	$f_{CPU} = f_{LSI}$	0.110	0.123	0.130	0.140	0.150	
			LSE ext. clock (32.768 kHz)(10)	$f_{CPU} = f_{LSE}$	0.100	0.101	0.104	0.119	0.122	

1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU}=f_{SYSCLK}$
2. For devices with suffix 6
3. For devices with suffix 7
4. For devices with suffix 3

HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 31. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High speed external oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$C^{(1)}$	Recommended load capacitance (2)	-	-	20	-	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} =16 MHz	-	-	2.5 (startup) 0.46 (stabilized)(3)	
g_m	Oscillator transconductance	-	3.5(3)	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data guaranteed by design.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 17. HSE oscillator circuit diagram

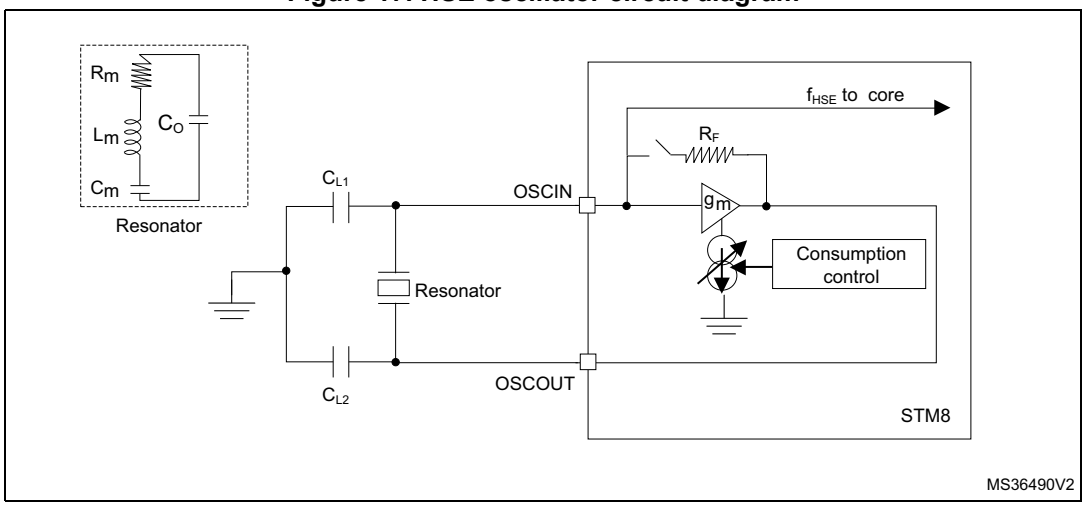
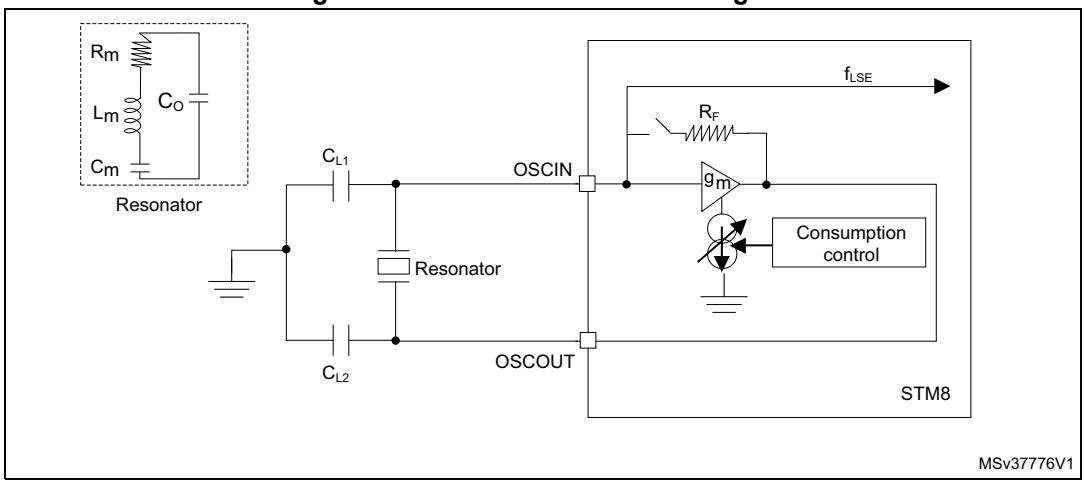


Figure 18. LSE oscillator circuit diagram



Internal clock sources

Subject to general operating conditions for V_{DD}, and T_A.

High speed internal RC oscillator (HSI)

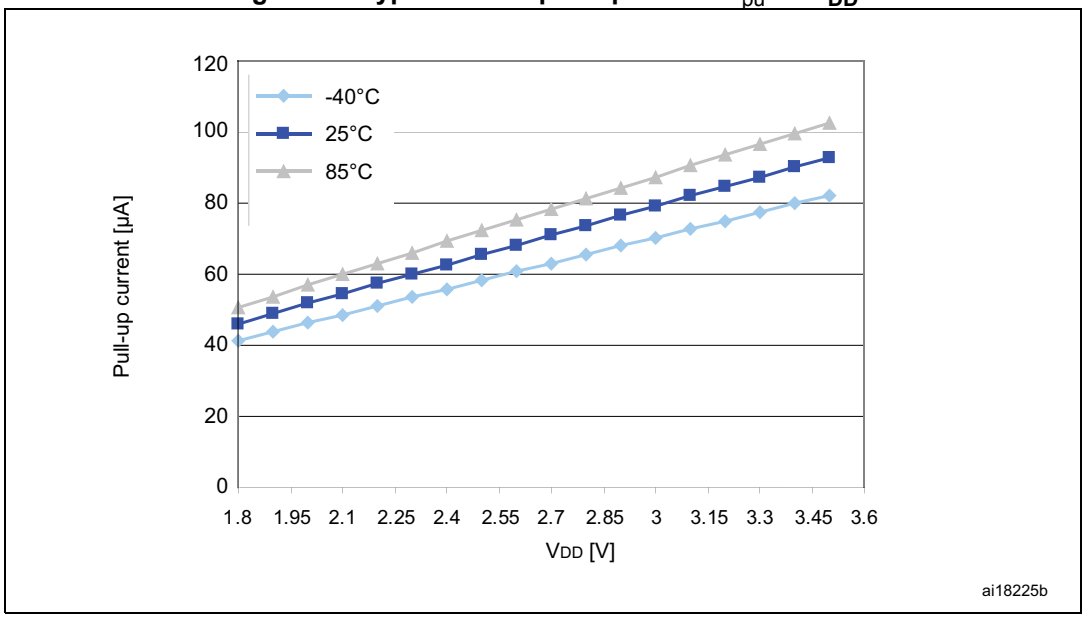
In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	-1 (2)	-	1(2)	%
		V_{DD} = 3.0 V, 0 °C ≤T_A ≤ 55 °C	-1.5	-	1.5	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 70 °C	-2	-	2	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 85 °C	-2.5	-	2	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 125 °C	-4.5	-	2	%
		1.65 V ≤V_{DD} ≤ 3.6 V, -40 °C ≤T_A ≤ 125 °C	-4.5	-	3	%
TRIM	HSI user trimming step(3)	Trimming code ≠ multiple of 16	-	0.4	0.7	%
		Trimming code = multiple of 16	-		± 1.5	%
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)	-	-	3.7	6(4)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	100	140(4)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Tested in production.
3. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.
4. Guaranteed by design.

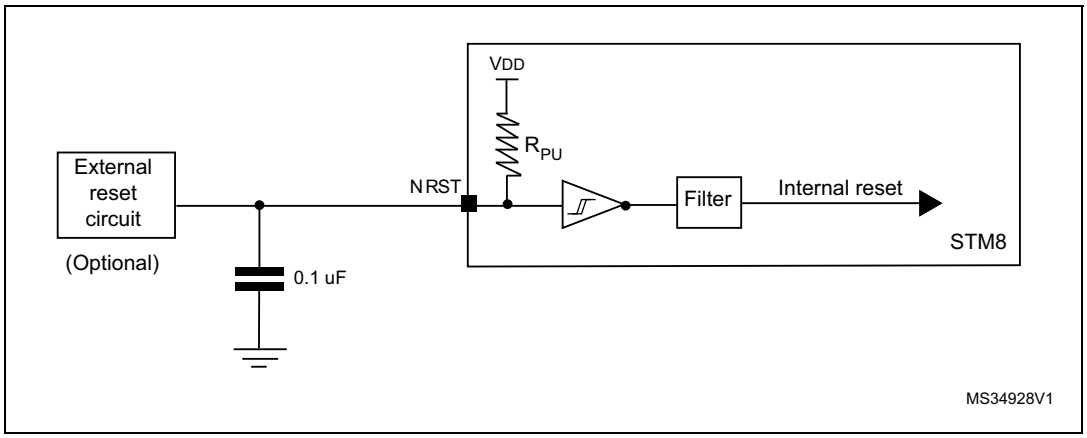
Figure 32. Typical NRST pull-up current I_{pu} vs V_{DD}



The reset network shown in *Figure 33* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max. level specified in *Table 42*. Otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, attention must be paid to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. The minimum recommended capacity is 10 nF.

Figure 33. Recommended NRST pin configuration



In the following table, data is based on characterization results, not tested in production.

Table 51. DAC accuracy

Symbol	Parameter	Conditions	Typ	Max	Unit
DNL	Differential non linearity(1)	R_L ≥5 kΩ, C_L≤50 pF DACOUT buffer ON(2)	1.5	3	12-bit LSB
		No load DACOUT buffer OFF	1.5	3	
INL	Integral non linearity(3)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	2	4	
		No load DACOUT buffer OFF	2	4	
Offset	Offset error(4)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	±10	±25	
		No load DACOUT buffer OFF	±5	±8	
Offset1	Offset error at Code 1 (5)	DACOUT buffer OFF	±1.5	±5	
Gain error	Gain error(6)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	+0.1/-0.2	+0.2/-0.5	%
		No load DACOUT buffer OFF	+0/-0.2	+0/-0.4	
TUE	Total unadjusted error	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(2)	12	30	12-bit LSB
		No load DACOUT buffer OFF	8	12	

1. Difference between two consecutive codes - 1 LSB.
2. For 48-pin packages only. For 28-pin and 32-pin packages, DAC output buffer must be kept off and no load must be applied.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
4. Difference between the value measured at Code (0x800) and the ideal value = V_{REF+}/2.
5. Difference between the value measured at Code (0x001) and the ideal value.
6. Difference between the ideal slope of the transfer function and the measured slope computed from Code 0x000 and 0xFFF when buffer is ON, and from Code giving 0.2 V and (V_{DDA} -0.2) V when buffer is OFF.

In the following table, data is guaranteed by design, not tested in production.

Table 52. DAC output on PB4-PB5-PB6(1)

Symbol	Parameter	Conditions	Max	Unit
R_{int}	Internal resistance between DAC output and PB4-PB5-PB6 output	2.7 V < V_{DD} < 3.6 V	1.4	kΩ
		2.4 V < V_{DD} < 3.6 V	1.6	
		2.0 V < V_{DD} < 3.6 V	3.2	
		1.8 V < V_{DD} < 3.6 V	8.2	

1. 32 or 28-pin packages only. The DAC channel can be routed either on PB4, PB5 or PB6 using the routing interface I/O switch registers.

In the following three tables, data is guaranteed by characterization result, not tested in production.

Table 54. ADC1 accuracy with V_{DDA} = 3.3 V to 2.5 V

Symbol	Parameter	Conditions	Typ	Max	Unit
DNL	Differential non linearity	f_{ADC} = 16 MHz	1	1.6	LSB
		f_{ADC} = 8 MHz	1	1.6	
		f_{ADC} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC} = 16 MHz	1.2	2	
		f_{ADC} = 8 MHz	1.2	1.8	
		f_{ADC} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC} = 16 MHz	2.2	3.0	
		f_{ADC} = 8 MHz	1.8	2.5	
		f_{ADC} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC} = 16 MHz	1.5	2	LSB
		f_{ADC} = 8 MHz	1	1.5	
		f_{ADC} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC} = 16 MHz	1	1.5	
		f_{ADC} = 8 MHz			
		f_{ADC} = 4 MHz			

Table 55. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	LSB
TUE	Total unadjusted error	2	4	LSB
Offset	Offset error	1	2	LSB
Gain	Gain error	1.5	3	LSB

Table 56. ADC1 accuracy with $V_{DDA} = V_{REF}^+$ = 1.8 V to 2.4 V

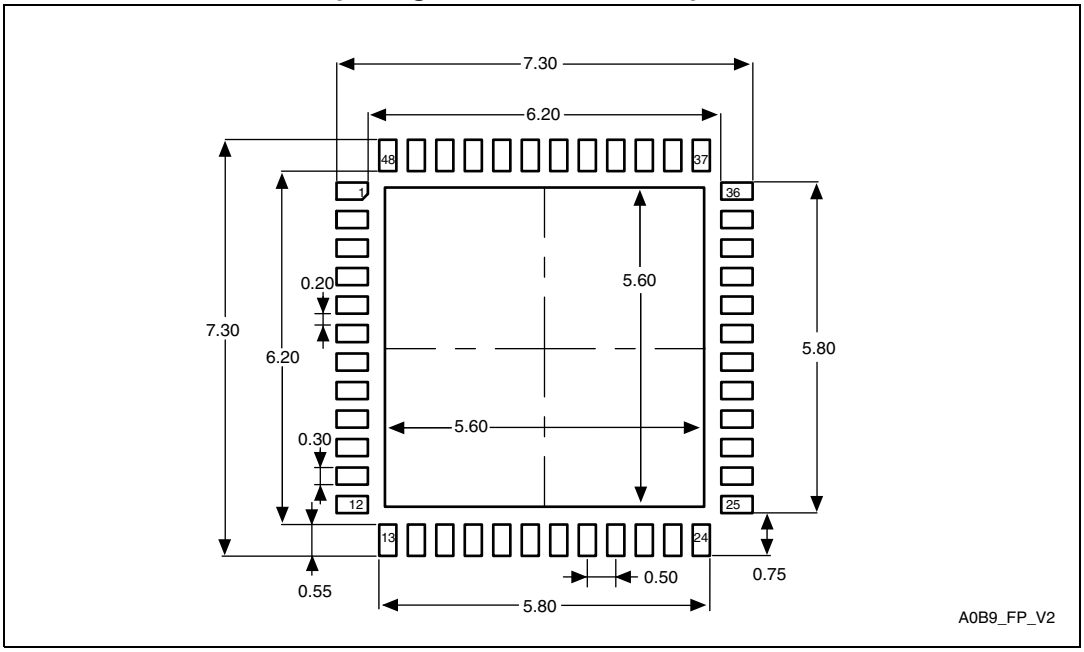
Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	LSB
TUE	Total unadjusted error	3	5	LSB
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

Table 63. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



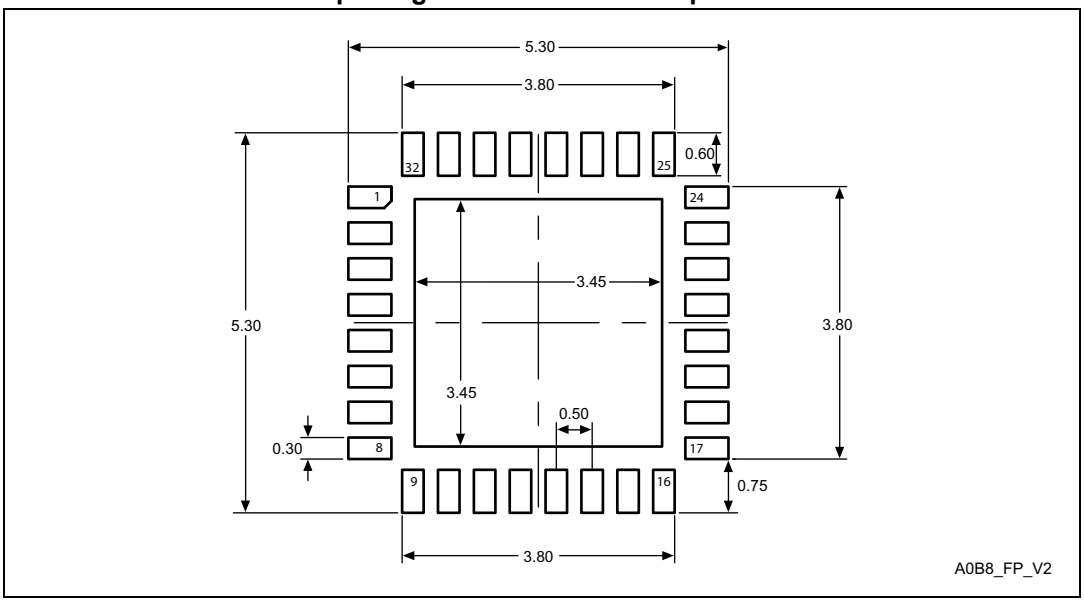
1. Dimensions are expressed in millimeters.

Table 65. UFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 53. UFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 69. Document revision history (continued)

Date	Revision	Changes
11-Mar-2011	6 cont'd	Modified OPT1 and OPT4 description in *Table: Option byte description.* Updated *Section: Electrical parameters* "standard I/Os" replaced with "high sink I//Os". Updated $R_{HN\ and}$ R_{HN} descriptions in *Table: LCD characteristics.* Added Tape & Reel option to *Figure: Medium density STM8L15x ordering information scheme*.
06-Sep-2011	7	*Features:* updated bullet point concerning capacitive sensing channels. *Section: Low power modes:* updated Wait mode and Halt mode definitions. *Section: Clock management:* added 'kHz' to 32.768 in the 'System clock sources bullet point'. *Section: System configuration controller and routing interface:* replaced last sentence concerning management of charge transfer acquisition sequence. Added *Section: Touchsensing* *Section Development support:* updated the *Bootloader.* *Table: Medium density STM8L15x pin description:* added LQFP32 to second column (same pinout as UFQFPN32); "Timer X - trigger" replaced by "Timer X - external trigger"; added note at the end of this table concerning the slope control of all GPIO pins. *Table: Interrupt mapping:* merged footnotes 1 and 2; updated some of the source blocks and descriptions. *Section: Option bytes*: replaced PM0051 by PM0054 and UM0320 by UM0470. *Table: Option byte description:* replaced the factory default setting (0xAA) for OPT0. *NRST pin:* updated text above the *Figure*; updated *Figure: Recommended NRST pin configuration*. *Table: TS characteristics:* removed typ and max values for the parameter T_{S_TEMP}; added min value for same. *Table: Comparator 1 characteristics:* added typ value for 'Comparator offset error'; added footnote *1.* *Table: Comparator 2 characteristics:* updated t_{START}, t_{dslow}, t_{dfast}, V_{offset}, I_{COMP2}; added footnotes *1.* and *3.* *Table: DAC characteristics:* updated max value for DAC_OUT voltage (DACOUT buffer ON). *Section: 12-bit ADC1 characteristics:* updated. Replaced *Figure: UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline* and *Figure: UFQFPN48 7 x 7 mm recommended footprint (dimensions in mm)*. *Figure: Medium density STM8L15x ordering information scheme*: removed 'TR = Tape & Reel".