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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | STM8 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT |
| Number of I/O | 41 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 25x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-UFQFN Exposed Pad |
| Supplier Device Package | 48-UFQFPN (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l152c6u6 |

# List of tables

# 1 Introduction

This document describes the features, pinout, mechanical data and ordering information of the medium-density STM8L151x4/6 and STM8L152x4/6 devices (STM8L151Cx/Kx/Gx, STM8L152Cx/Kx microcontrollers with a 16-Kbyte or 32-Kbyte Flash memory density). These devices are referred to as medium-density devices in the STM8L15x and STM8L16x reference manual (RM0031) and in the STM8L Flash programming manual (PM0054).

For more details on the whole STMicroelectronics ultra-low-power family please refer to *Section 2.2: Ultra-low-power continuum on page 13*.

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

The medium-density devices provide the following benefits:

- Integrated system
  - Up to 32 Kbyte of medium-density embedded Flash program memory
  - 1 Kbyte of data EEPROM
  - Internal high speed and low-power low speed RC
  - Embedded reset
- Ultra-low power consumption
  - 195 µA/MHz + 440 µA (consumption)
  - 0.9 µA with LSI in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low power wait mode and Low power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals
  - Wide choice of development tools

All devices offer 12-bit ADC, DAC, two comparators, Real-time clock three 16-bit timers, one 8-bit timer as well as standard communication interface such as SPI, I2C and USART. A 4x28-segment LCD is available on the medium-density STM8L152xx line. *Table 2: Medium-density STM8L151x4/6 and STM8L152x4/6 low-power device features and peripheral counts* and *Section 3: Functional overview* give an overview of the complete range of peripherals proposed in this family.

*Figure 1 on page 14* shows the general block diagram of the device family.

## 3.3 Reset and supply management

### 3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage ($V_{DD}$). The external power supply pins must be connected as follows:

- $V_{SS1}$; $V_{DD1}$ = 1.8 to 3.6 V, down to 1.65 V at power down: external power supply for I/Os and for the internal regulator. Provided externally through $V_{DD1}$ pins, the corresponding ground pin is $V_{SS1}$.
- $V_{SSA;}$ $V_{DDA}$ = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for analog peripherals (minimum voltage to be applied to $V_{DDA}$ is 1.8 V when the ADC1 is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD1}$ and $V_{SS1}$, respectively.
- $V_{SS2}$; $V_{DD2}$ = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for I/Os. $V_{DD2}$ and $V_{SS2}$ must be connected to $V_{DD1}$ and $V_{SS1}$, respectively.
- $V_{REF+}$; $V_{REF-}$ (for ADC1): external reference voltage for ADC1. Must be provided externally through $V_{REF+}$ and $V_{REF-}$ pin.
- $V_{REF+}$ (for DAC): external voltage reference for DAC must be provided externally through $V_{REF+}$.

### 3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the $V_{DD}$ min value at power down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains under reset when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.3.3 Voltage regulator

The medium-density STM8L151x4/6 and STM8L152x4/6 embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

**Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48/UFQFPN48 | LQFP32/UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| - | 5 | 5 | D4 | PA5/TIM3_BKIN/ *[TIM3_ETR]*(4)/ LCD_COM1(2)/ADC1_IN1/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port A5** | Timer 3 - break input / *[Timer 3 - external trigger]* / LCD_COM 1 / ADC1 input 1 / Comparator 1 positive input |
| 7 | 6 | - | - | PA6/*[ADC1_TRIG]*(4)/ LCD_COM2(2)/ADC1_IN0/ COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port A6** | *[ADC1 - trigger]* / LCD_COM2 / ADC1 input 0 / Comparator 1 positive input |
| 8 | - | - | - | PA7/LCD_SEG0(2)(5) | I/O | FT | **X** | X | X | HS | X | X | **Port A7** | LCD segment 0 |
| 24 | 13 | 12 | E3 | PB0(6)/TIM2_CH1/ LCD_SEG10(2)/ ADC1_IN18/COMP1_INP | I/O | TT (3) | **X**(6) | X(6) | X | HS | X | X | **Port B0** | Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18 / Comparator 1 positive input |
| 25 | 14 | 13 | G1 | PB1/TIM3_CH1/ LCD_SEG11(2)/ ADC1_IN17/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port B1** | Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17 / Comparator 1 positive input |
| 26 | 15 | 14 | F2 | PB2/ TIM2_CH2/ LCD_SEG12(2)/ ADC1_IN16/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port B2** | Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16/ Comparator 1 positive input |
| 27 | - | - | - | PB3/TIM2_ETR/ LCD_SEG13(2)/ ADC1_IN15/COMP1_INP | I/O | TT (3) | **X** | X | X | HS | X | X | **Port B3** | Timer 2 - external trigger / LCD segment 13 /ADC1_IN15 / Comparator 1 positive input |

**Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48/UFQFPN48 | LQFP32/UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| - | 8 | 7 | G4 | $V_{DD1}/V_{DDA}/V_{REF+}$ | S | - | - | - | - | - | - | - | Digital power supply / Analog supply voltage / ADC1 positive voltage reference | |
| 9 | 7 | 6 | F4 | $V_{SS1}/V_{SSA}/V_{REF-}$ | S | - | - | - | - | - | - | - | I/O ground / Analog ground voltage / ADC1 negative voltage reference | |
| 39 | - | - | - | $V_{DD2}$ | S | - | - | - | - | - | - | - | IOs supply voltage | |
| 40 | - | - | - | $V_{SS2}$ | S | - | - | - | - | - | - | - | IOs ground voltage | |
| 1 | 32 | 28 | A4 | PA0(9)/*[USART1_CK]*(4)/ SWIM/BEEP/IR_TIM (10) | I/O | | X | **X**(9) | X | HS (10) | X | X | **Port A0** | *[USART1 synchronous clock]*(4) / SWIM input and output / Beep output / Infrared Timer output |

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15x and STM8L16x reference manual (RM0031).
2. Available on STM8L152xx devices only.
3. In the 3.6 V tolerant I/Os, protection diode to $V_{DD}$ is not implemented.
4. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
5. In the 5 V tolerant I/Os, protection diode to $V_{DD}$ is not implemented.
6. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
7. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to $V_{DD}$ are not implemented).
8. Available on STM8L151xx devices only.
9. The PA0 pin is in input pull-up during the reset phase and after reset release.
10. High Sink LED driver capability available on PA0.

*Note: The slope control of all GPIO pins, except true open drain pins, can be programmed. By default, the slope control is limited to 2 MHz.*

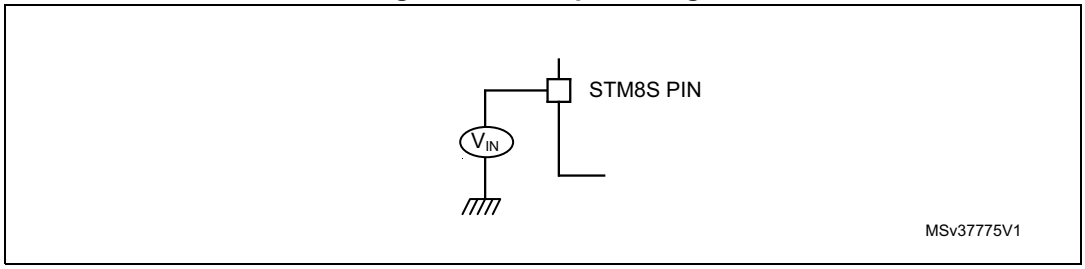
**Table 13. Option byte description**

| Option byte No. | Option description |
|---|---|
| OPT0 | **ROP[7:0]** Memory readout protection (ROP)<br>0xAA: Disable readout protection (write access via SWIM protocol)<br>Refer to Readout protection section in the STM8L15x and STM8L16x reference manual (RM0031). |
| OPT1 | **UBC[7:0]** Size of the user boot code area<br>0x00: no UBC<br>0x01: the UBC contains only the interrupt vectors.<br>0x02: Page 0 and 1 reserved for the UBC and read/write protected. Page 0 contains only the interrupt vectors.<br>0x03 - Page 0 to 2 reserved for UBC, memory write-protected<br>0xFF - Page 0 to 254 reserved for UBC, memory write-protected<br>Refer to User boot code section in the STM8L15x and STM8L16x reference manual (RM0031). |
| OPT2 | Reserved |
| OPT3 | **IWDG_HW:** Independent watchdog<br>0: Independent watchdog activated by software<br>1: Independent watchdog activated by hardware |
| | **IWDG_HALT:** Independent window watchdog off on Halt/Active-halt<br>0: Independent watchdog continues running in Halt/Active-halt mode<br>1: Independent watchdog stopped in Halt/Active-halt mode |
| | **WWDG_HW:** Window watchdog<br>0: Window watchdog activated by software<br>1: Window watchdog activated by hardware |
| | **WWDG_HALT:** Window window watchdog reset on Halt/Active-halt<br>0: Window watchdog stopped in Halt mode<br>1: Window watchdog generates a reset when MCU enters Halt mode |
| OPT4 | **HSECNT**: Number of HSE oscillator stabilization clock cycles<br>0x00 - 1 clock cycle<br>0x01 - 16 clock cycles<br>0x10 - 512 clock cycles<br>0x11 - 4096 clock cycles |
| | **LSECNT**: Number of LSE oscillator stabilization clock cycles<br>0x00 - 1 clock cycle<br>0x01 - 16 clock cycles<br>0x10 - 512 clock cycles<br>0x11 - 4096 clock cycles<br>Refer to *Table 32: LSE oscillator characteristics on page 84*. |

### 9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

**Figure 11. Pin input voltage**




## 9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 15: Voltage characteristics*, *Table 16: Current characteristics*, and *Table 17: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

**Table 15. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$- $V_{SS}$ | External supply voltage (including $V_{DDA}$ and $V_{DD2}$)(1) | - 0.3 | 4.0 | V |
| $V_{IN}$(2) | Input voltage on true open-drain pins (PC0 and PC1) | $V_{SS}$ - 0.3 | $V_{DD}$ + 4.0 | V |
| | Input voltage on five-volt tolerant (FT) pins (PA7 and PE0) | $V_{SS}$ - 0.3 | $V_{DD}$ + 4.0 | |
| | Input voltage on 3.6 V tolerant (TT) pins | $V_{SS}$ - 0.3 | 4.0 | |
| | Input voltage on any other pin | $V_{SS}$ - 0.3 | 4.0 | |
| $V_{ESD}$ | Electrostatic discharge voltage | see *Absolute maximum ratings (electrical sensitivity) on page 115* | | |

1. All power ($V_{DD1}$, $V_{DD2}$, $V_{DDA}$) and ground ($V_{SS1}$, $V_{SS2}$, $V_{SSA}$) pins must always be connected to the external power supply.
2. $V_{IN}$ maximum must always be respected. Refer to *Table 16.* for maximum allowed injected current values.

Figure 16. Typ. $I_{DD(LPW)}$ vs. $V_{DD}$ (LSI clock source)

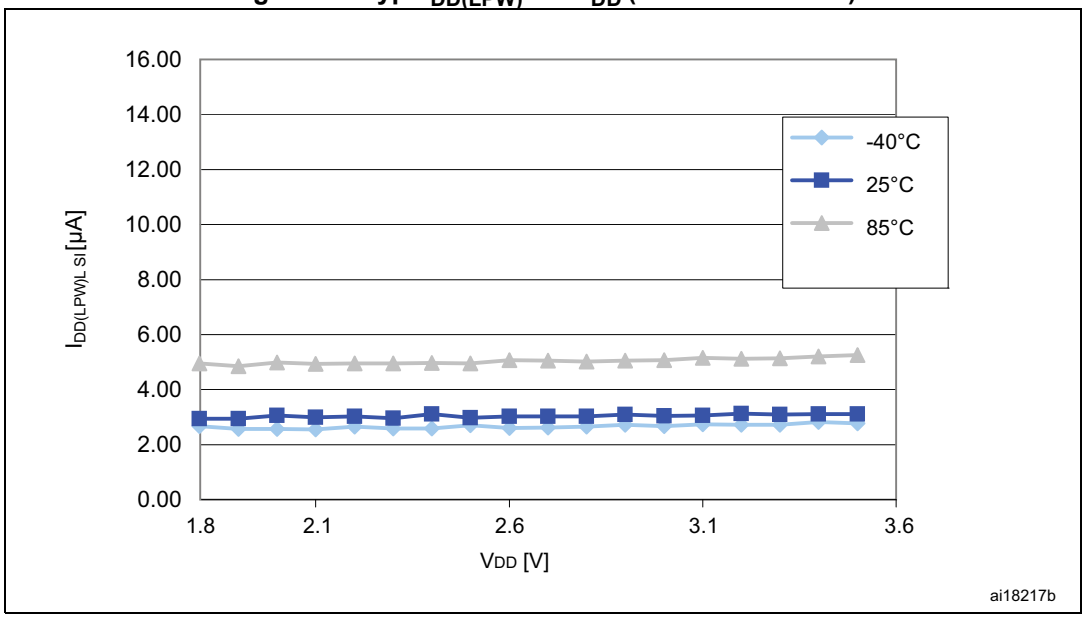


**Table 25. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal**

| Symbol | Parameter | Condition(1) | | Typ | Unit |
|---|---|---|---|---|---|
| $I_{DD(AH)}$ (2) | Supply current in Active-halt mode | $V_{DD}$ = 1.8 V | LSE | 1.15 | µA |
| | | | LSE/32(3) | 1.05 | |
| | | $V_{DD}$ = 3 V | LSE | 1.30 | |
| | | | LSE/32(3) | 1.20 | |
| | | $V_{DD}$ = 3.6 V | LSE | 1.45 | |
| | | | LSE/32(3) | 1.35 | |

1. No floating I/O, unless otherwise specified.
2. Based on measurements on bench with 32.768 kHz external crystal oscillator.
3. RTC clock is LSE divided by 32.

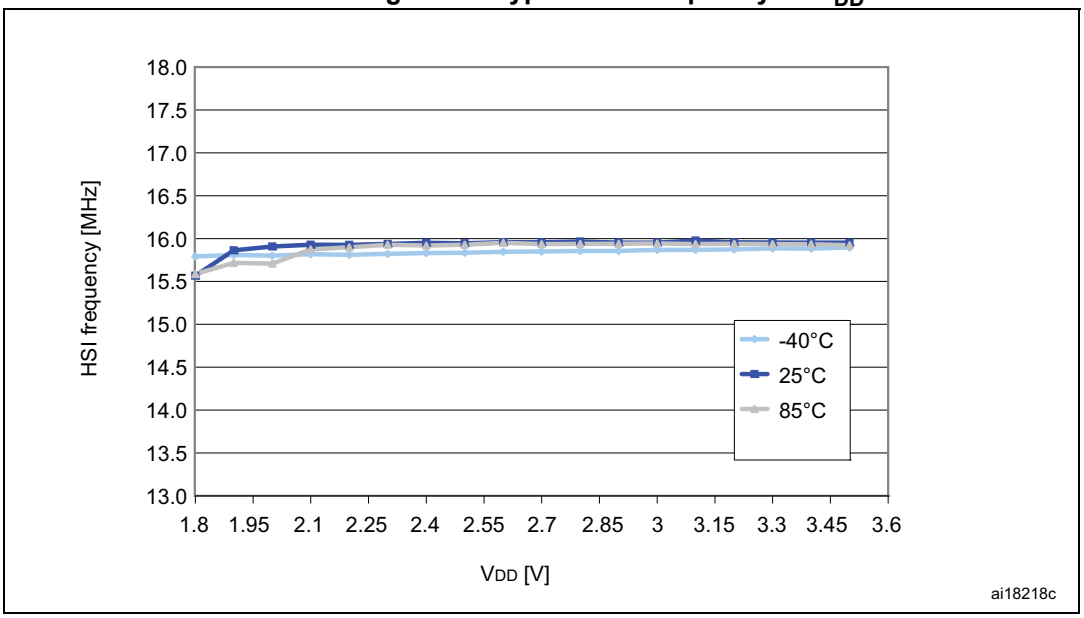
In the following table, data is based on characterization results, unless otherwise specified.

**Table 26. Total current consumption and timing in Halt mode at $V_{DD}$ = 1.65 to 3.6 V**

| Symbol | Parameter | Condition(1) | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{DD(Halt)}$ | Supply current in Halt mode (Ultra-low-power ULP bit =1 in the PWR_CSR2 register) | $T_A$ = -40 °C to 25 °C | 350 | 1400(2) | nA |
| | | $T_A$ = 55 °C | 580 | 2000 | |
| | | $T_A$ = 85 °C | 1160 | 2800(2) | |
| | | $T_A$ = 105 °C | 2560 | 6700(2) | |
| | | $T_A$ = 125 °C | 4.4 | 13(2) | µA |
| $I_{DD(WUHalt)}$ | Supply current during wakeup time from Halt mode (using HSI) | - | 2.4 | - | mA |
| $t_{WU\_HSI(Halt)}$ (3)(4) | Wakeup time from Halt to Run mode (using HSI) | - | 4.7 | 7 | µs |
| $t_{WU\_LSI(Halt)}$ (3)(4) | Wakeup time from Halt mode to Run mode (using LSI) | - | 150 | - | µs |

1. $T_A$ = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. Tested in production.
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.
4. Wakeup time until start of interrupt vector fetch.
The first word of interrupt routine is fetched 4 CPU cycles after $t_{WU}$.

Figure 19. Typical HSI frequency vs $V_{DD}$




### Low speed internal RC oscillator (LSI)

In the following table, data is based on characterization results, not tested in production.

Table 34. LSI oscillator characteristics

| Symbol | Parameter (1) | Conditions(1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSI}$ | Frequency | - | 26 | 38 | 56 | kHz |
| $t_{su(LSI)}$ | LSI oscillator wakeup time | - | - | - | 200(2) | µs |
| $I_{DD(LSI)}$ | LSI oscillator frequency drift(3) | 0 °C ≤$T_A$ ≤85 °C | -12 | - | 11 | % |

1. $V_{DD}$ = 1.65 V to 3.6 V, $T_A$ = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

## 9.3.8 Communication interfaces

### SPI1 - Serial peripheral interface

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, $f_{SYSCLK}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 43. SPI1 characteristics**

| Symbol | Parameter | Conditions(1) | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI1 clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 8 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI1 clock rise and fall time | Capacitive load: C = 30 pF | - | 30 | ns |
| $t_{su(NSS)}$(2) | NSS setup time | Slave mode | 4 x $1/f_{SYSCLK}$ | - | |
| $t_{h(NSS)}$(2) | NSS hold time | Slave mode | 80 | - | |
| $t_{w(SCKH)}$(2)<br>$t_{w(SCKL)}$(2) | SCK high and low time | Master mode,<br>$f_{MASTER}$ = 8 MHz, $f_{SCK}$= 4 MHz | 105 | 145 | |
| $t_{su(MI)}$(2)<br>$t_{su(SI)}$(2) | Data input setup time | Master mode | 30 | - | |
| | | Slave mode | 3 | - | |
| $t_{h(MI)}$(2)<br>$t_{h(SI)}$(2) | Data input hold time | Master mode | 15 | - | |
| | | Slave mode | 0 | - | |
| $t_{a(SO)}$(2)(3) | Data output access time | Slave mode | - | 3x $1/f_{SYSCLK}$ | |
| $t_{dis(SO)}$(2)(4) | Data output disable time | Slave mode | 30 | - | |
| $t_{v(SO)}$(2) | Data output valid time | Slave mode (after enable edge) | - | 60 | |
| $t_{v(MO)}$(2) | Data output valid time | Master mode (after enable edge) | - | 20 | |
| $t_{h(SO)}$(2) | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| $t_{h(MO)}$(2) | | Master mode (after enable edge) | 1 | - | |

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

**Figure 38. ADC1 accuracy characteristics**

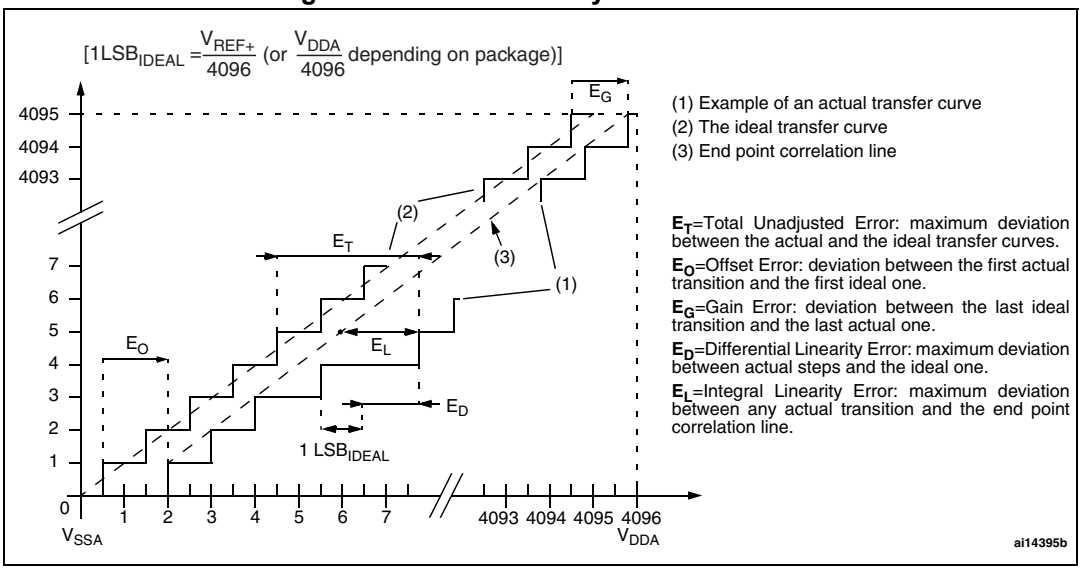
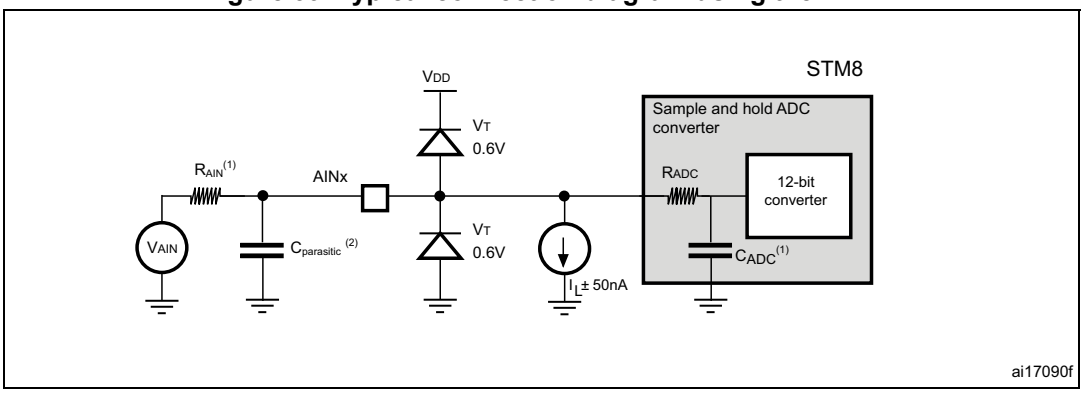
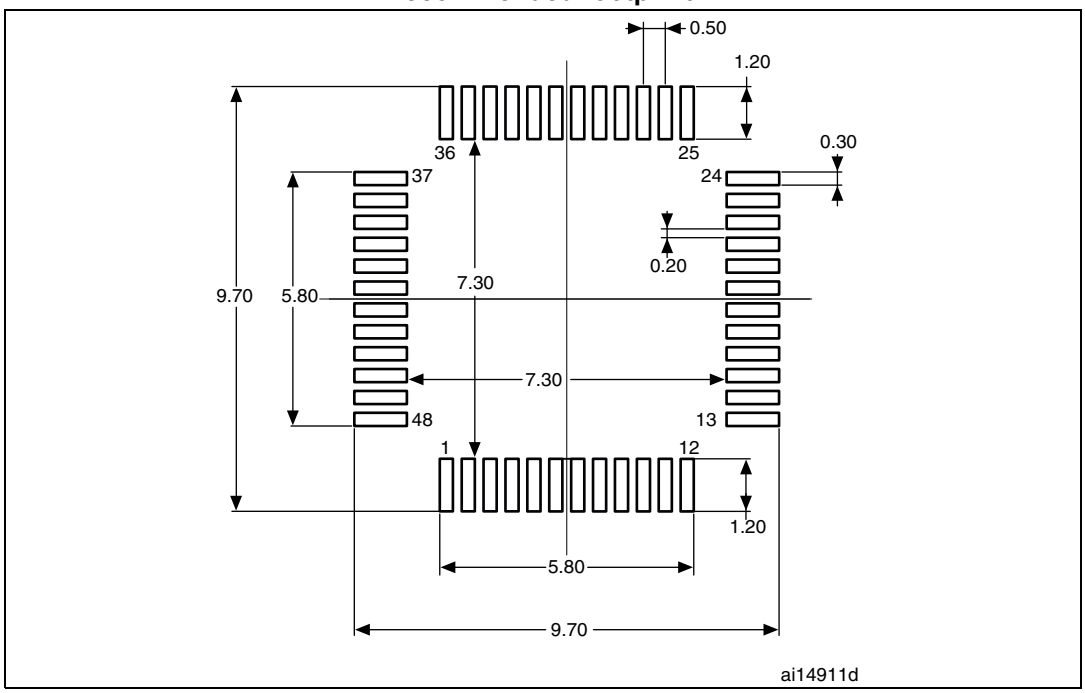



**Figure 39. Typical connection diagram using the ADC**




1. Refer to *Table 53* for the values of $R_{AIN}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

**Figure 44. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint**



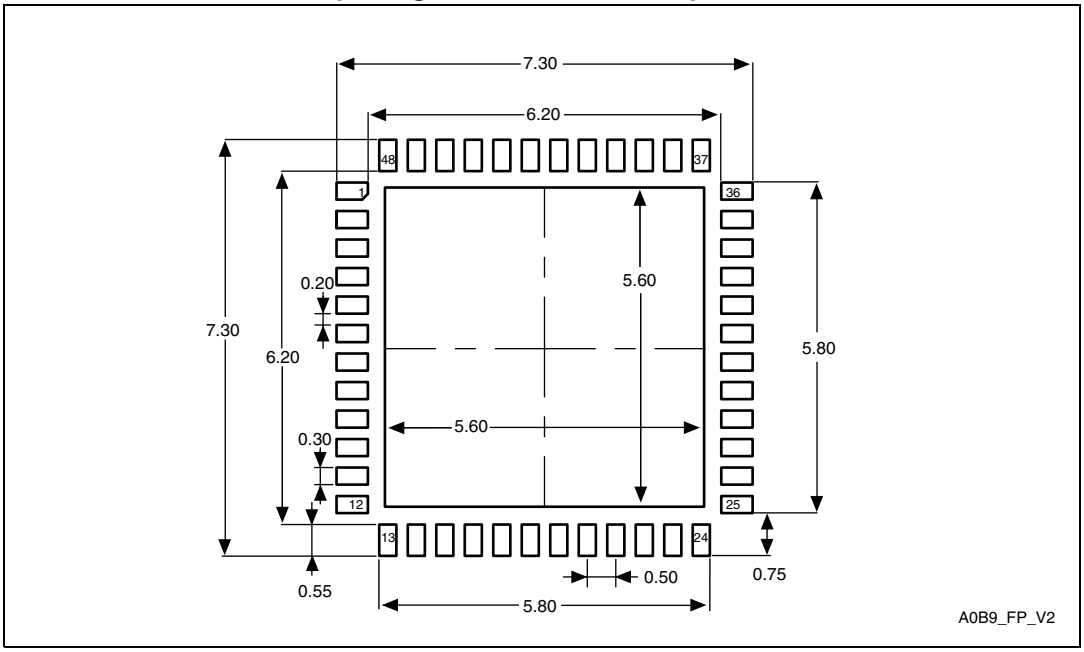

1. Dimensions are expressed in millimeters.

**Table 63. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| D | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| E | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| D2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| E2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| T | - | 0.152 | - | - | 0.0060 | - |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

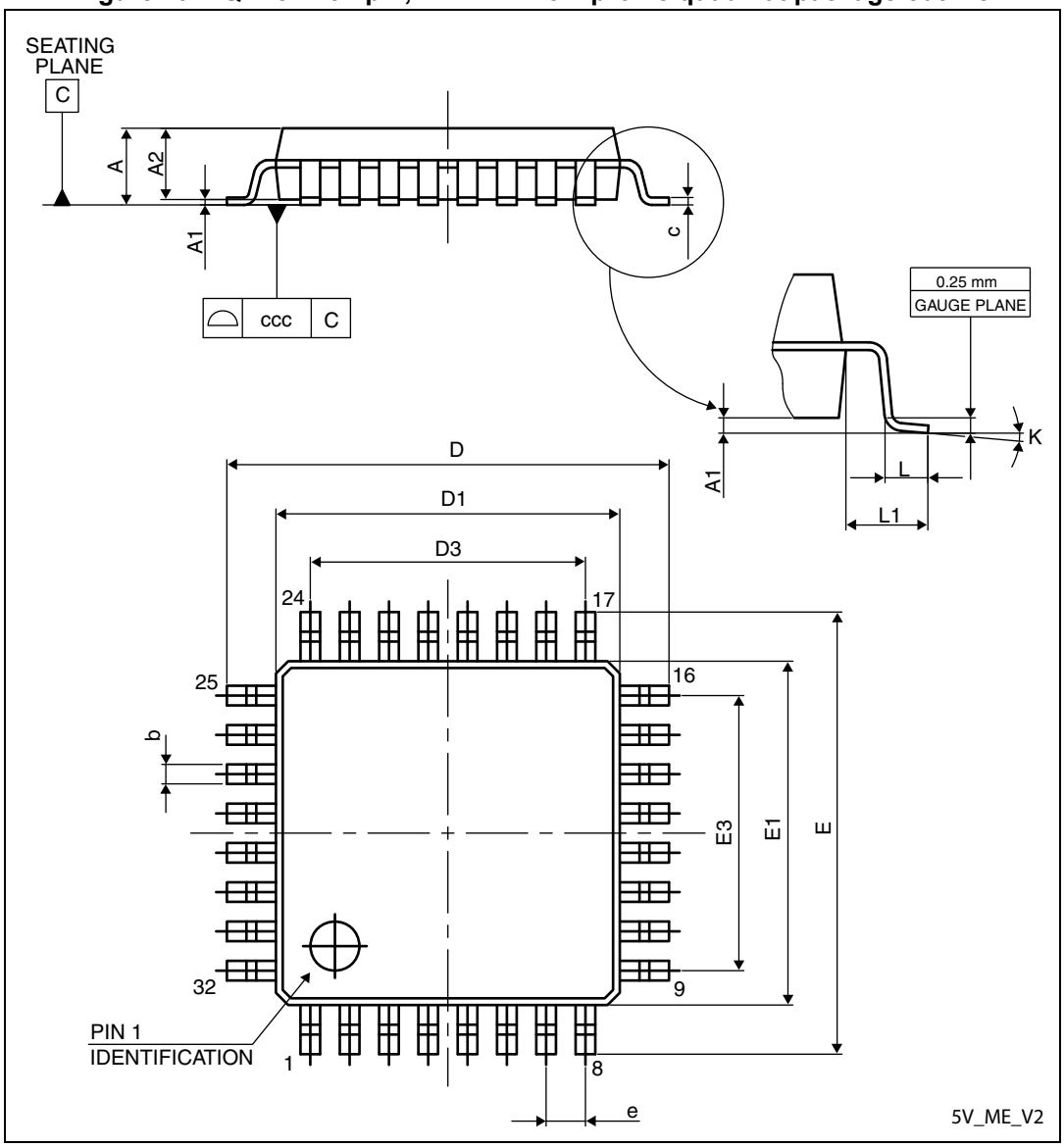
**Figure 47. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

## 10.4 LQFP32 package information

**Figure 49. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline**

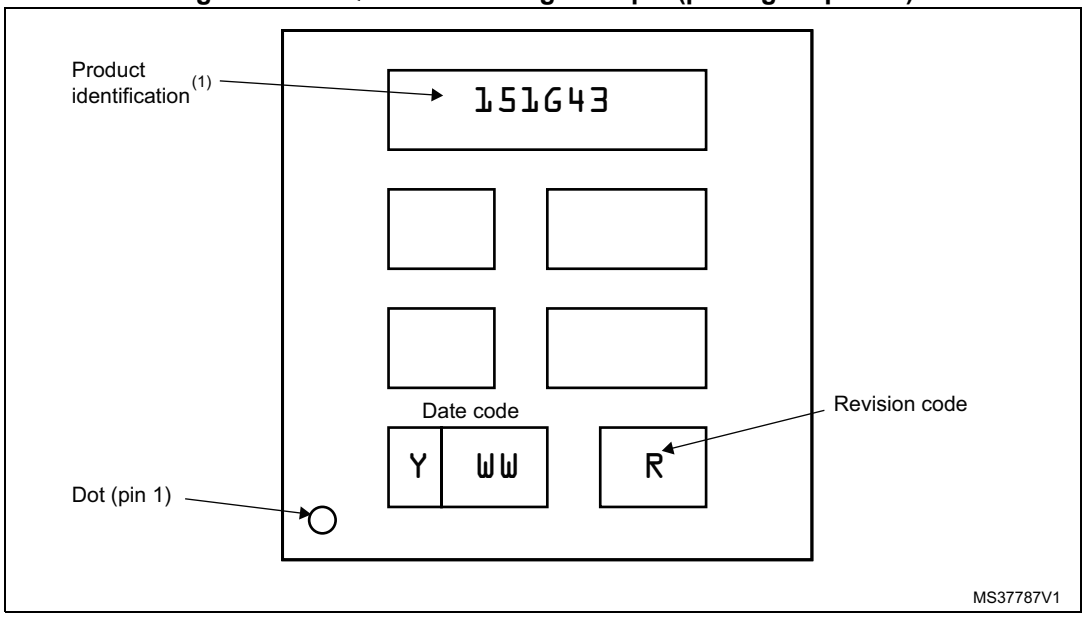



1. Drawing is not to scale.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 57. UFQFPN28 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

**Table 69. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 23-Jul-2010 | 5 | Modified *Introduction* and *Description.*<br>Modified *Table: Legend/abbreviation for table 5* and *Table: Medium density STM8L15x pin description* (for PA0, PA1, PB0 and PB4 and for reset states in the floating input column)<br>Modified *Figure: Low density STM8L151xx device block diagram, Figure: Low density STM8L15x clock tree diagram*, *Figure: Low power modes* and *Figure : Low power real-time clock.*<br>Modified CLK_PCKENR2 and CLK_HSICALR reset values in *Table: General hardware register map.*<br>Modified notes below *Figure: Memory map.*<br>Modified PA_CR1 reset value.<br>Modified reset values for Px_IDR registers.<br>Modified *Table: Voltage characteristics* and *Table: Current characteristics.*<br>Modified $V_{IH}$ in *Table: I/O static characteristics.*<br>Modified *Table: Total current consumption in Wait mode.*<br>Modified *Figure Typical application with I2C bus and timing diagram 1).*<br>Modified $I_L$ value in *Figure: Typical connection diagram using the ADC1.*<br>Modified $R_H$ and $R_L$ in *Table: LCD characteristics.*<br>Added graphs in *Section: Electrical parameters.*<br>Modified note 3 below *Table: Reference voltage characteristics.*<br>Modified note 1 below *Table: TS characteristics.*<br>Changed $V_{ESD(CDM)}$ value in *Table: ESD absolute maximum ratings.*<br>Updated notes for UFQFPN32 and UFQFPN48 packages. |
| 11-Mar-2011 | 6 | Modified note on true open drain I/Os and I/O level columns in *Table: Medium density STM8L15x pin description.*<br>Remapping option removed for USART1_TX, USART1_RX, and USART1_CK on PC2, PC3 and PC4 in *Table: Medium density STM8L15x pin description.*<br>Modified IDWDG_KR reset value in *Table: General hardware register map.*<br>Replaced VREF_OUT with VREFINT and TIMx_TRIG with TIMx_ETR.<br>Added *Table: Factory conversion registers.* Modified reset values for TIM1_DCR1, IWDG_KR, RTC_DR1, RTC_DR2, RTC_SPRERH, RTC_SPRERL, RTC_APRER, RTC_WUTRH, and RTC_WUTRL in *Table: General hardware register map.*<br>Added notes to certain values in *Section: Embedded reference voltage* and *Section: Temperature sensor.* |

**Table 69. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 10-Feb-2012 | 8 | *Features:* replaced "'Dynamic consumption' with 'Consumption'.<br>*Table: Medium density STM8L15x pin description*: updated OD column of NRST/PA1 pin.<br>*Table: Interrupt mapping:* removed tamper 1, tamper 2 and tamper 3.<br>*Figure: UFQFPN48 package outline:* replaced.<br>*Table: UFQFPN48 package mechanical data:* updated title.<br>*Figure: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5):* removed the line over A1.<br>*Figure: UFQFPN28 package outline:* replaced to improve readability of UFQFPN28 package dimensions A, L, and L1.<br>*Figure: Recommended UFQFPN28 footprint (dimensions in mm)*: updated title.<br>*Figure: WLCSP28 package outline:* updated title.<br>*Table: WLCSP28 package mechanical data:* updated title. |
| 02-Mar-2012 | 9 | Updated *Table: UFQFPN48 package mechanical data.*<br>Updated *Figure: UFQFPN28 package outline, Figure: Recommended UFQFPN28 footprint (dimensions in mm)* and *Table: UFQFPN28 package mechanical data.*<br>*Table: WLCSP28 package mechanical data:* Min and Max values removed for e1, e2, e3, e4, F and G dimensions. |
| 30-Mar-2012 | 10 | *Figure: SPI1 timing diagram - master mode(1):* changed SCK signals to 'output' instead of 'input'.<br>*Figure: Medium density STM8L15x ordering information scheme*: added 'Tape & reel' to package section. |
| 26-Apr-2012 | 11 | Updated *Table: WLCSP28 package mechanical data.* |
| 12-Nov-2013 | 12 | Updated *Table: WLCSP28 package mechanical data.*<br>Updated *Table: Medium-density STM8L15x pin description.*<br>Updated *Table 2: Medium density STM8L15x low power device features and peripheral counts*.<br>Added *Figure: Recommended LQFP48 footprint* and *Figure: Recommended LQFP32 footprint.* |
| 12-Aug-2013 | 13 | Changed the default setting value of OPT5 to 0x00 in *Table: Option byte addresses*.<br>Added tTEMP 'BOR detector enabled' and 'disabled' characteristics in *Table: Embedded reset and power control block characteristics*.<br>Updated E2, D2 and ddd in *Table: UFQFPN48 package mechanical data* |

**Table 69. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 21-Apr-2015 | 14 | Added:<br>– *Figure 45: LQFP48 marking example (package top view)*,<br>– *Figure 48: UFQFPN48 marking example (package top view)*,<br>– *Figure 51: LQFP32 marking example (package top view)*,<br>– *Figure 54: UFQFPN32 marking example (package top view)*,<br>– *Figure 57: UFQFPN28 marking example (package top view)*,<br>– *Figure 59: WLCSP28 marking example (package top view)*. |
| 07-Apr-2017 | 15 | Changed symbol $V_{125}$ to $V_{90}$ in *Table 47: TS characteristics* and updated related Min/Typ/Max values. Updated *Section 9.2: Absolute maximum ratings*. Updated table notes for *Table 30*, *Table 31*, *Table 32*, *Table 33*, *Table 34*, *Table 36*, *Table 38*, *Table 42*, *Table 43*, *Table 46*, *Table 47*, *Table 48*, *Table 49*, *Table 53*, *Table 57*, and *Table 60*. Updated device marking paragraphs in *Section 10.2*, *Section 10.3*, *Section 10.4*, *Section 10.5*, *Section 10.6*, and *Section 10.7*. |