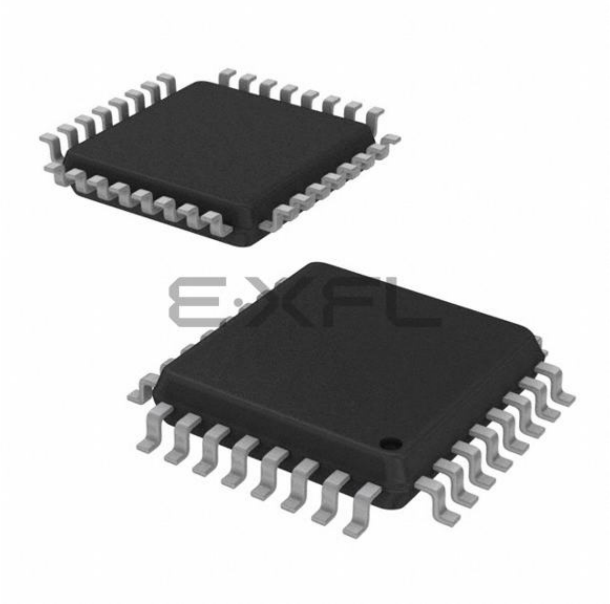

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l152k4t6

Contents

List of figures

1 Introduction

This document describes the features, pinout, mechanical data and ordering information of the medium-density STM8L151x4/6 and STM8L152x4/6 devices (STM8L151Cx/Kx/Gx, STM8L152Cx/Kx microcontrollers with a 16-Kbyte or 32-Kbyte Flash memory density). These devices are referred to as medium-density devices in the STM8L15x and STM8L16x reference manual (RM0031) and in the STM8L Flash programming manual (PM0054).

For more details on the whole STMicroelectronics ultra-low-power family please refer to *Section 2.2: Ultra-low-power continuum on page 13*.

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

The medium-density devices provide the following benefits:

- Integrated system
  - Up to 32 Kbyte of medium-density embedded Flash program memory
  - 1 Kbyte of data EEPROM
  - Internal high speed and low-power low speed RC
  - Embedded reset
- Ultra-low power consumption
  - 195 µA/MHz + 440 µA (consumption)
  - 0.9 µA with LSI in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low power wait mode and Low power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals
  - Wide choice of development tools

All devices offer 12-bit ADC, DAC, two comparators, Real-time clock three 16-bit timers, one 8-bit timer as well as standard communication interface such as SPI, I2C and USART. A 4x28-segment LCD is available on the medium-density STM8L152xx line. *Table 2: Medium-density STM8L151x4/6 and STM8L152x4/6 low-power device features and peripheral counts* and *Section 3: Functional overview* give an overview of the complete range of peripherals proposed in this family.

Figure 1 on page 14 shows the general block diagram of the device family.

3.4 Clock management

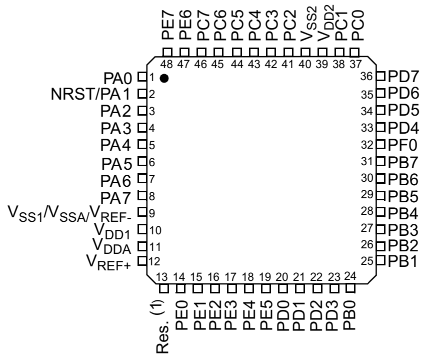
The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources can be used to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 kHz Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC and LCD clock sources:** the above four sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

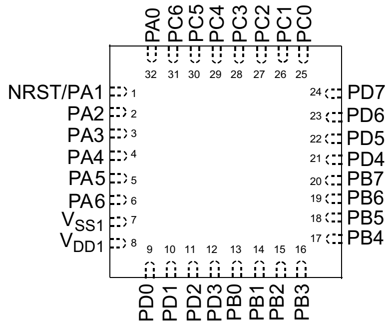
4 Pinout and pin description

Figure 3. STM8L151C4, STM8L151C6 48-pin pinout (without LCD)



1. Reserved. Must be tied to V_{DD}.

Figure 4. STM8L151K4, STM8L151K6 32-pin package pinout (without LCD)



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.

Figure 5. STM8L151Gx UFQFPN28 package pinout

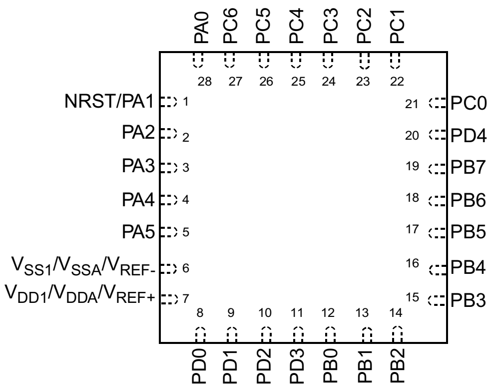


Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
30	-	-	-	PB6/[*SPI1_MOSI*][4]/ LCD_SEG16[2]/ ADC1_IN12/COMP1_INP	I/O	TT[3]	**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out/slave in]*/ LCD segment 16 / ADC1_IN12 / Comparator 1 positive input
-	19	18	F1	PB6/*[SPI1_MOSI]*[4]/ LCD_SEG16[2]/ ADC1_IN12/COMP1_INP/ DAC_OUT	I/O	TT[3]	**X**	X	X	HS	X	X	**Port B6**	*[SPI1 master out]*/ slave in / LCD segment 16 / ADC1_IN12 / DAC output / Comparator 1 positive input
31	20	19	E1	PB7/*[SPI1_MISO]*[4]/ LCD_SEG17[2]/ ADC1_IN11/COMP1_INP	I/O	TT[3]	**X**	X	X	HS	X	X	**Port B7**	*[SPI1 master in- slave out]* / LCD segment 17 / ADC1_IN11 / Comparator 1 positive input
37	25	21	B1	PC0[5]/I2C1_SDA	I/O	FT	**X**		X		T[7]		**Port C0**	I2C1 data
38	26	22	A1	PC1[5]/I2C1_SCL	I/O	FT	**X**		X		T[7]		**Port C1**	I2C1 clock
41	27	23	B2	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREFINT	I/O	TT[3]	**X**	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6 / Comparator 1 positive input / Internal voltage reference output
42	28	24	A2	PC3/USART1_TX/ LCD_SEG23[2]/ ADC1_IN5/COMP1_INP/ COMP2_INM	I/O	TT[3]	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5 / Comparator 1 positive input / Comparator 2 negative input
43	29	25	C2	PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24[2]/ ADC1_IN4/COMP2_INM/ COMP1_INP	I/O	TT[3]	**X**	X	X	HS	X	X	**Port C4**	USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input

have a fixed value: 0x3.

4. Refer to *Table 9* for an overview of hardware register mapping, to *Table 8* for details on I/O port hardware registers, and to *Table 10* for information on CPU/SWIM/debug module controller registers.

Table 6. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	2 Kbyte	0x00 0000	0x00 07FF
Flash program memory	16 Kbyte	0x00 8000	0x00 BFFF
	32 Kbyte	0x00 8000	0x00 FFFF

5.2 Register map

Table 7. Factory conversion registers

Address	Block	Register label	Register name	Reset status
0x00 4910	-	VREFINT_Factory_CONV(1)	Internal reference voltage factory conversion	0xXX
0x00 4911	-	TS_Factory_CONV_V90(2)	Temperature sensor output voltage	0xXX

1. The VREFINT_Factory_CONV byte represents the 8 LSB of the result of the VREFINT 12-bit ADC conversion performed in factory. The MSB have a fixed value: 0x6.

2. The TS_Factory_CONV_V90 byte represents the 8 LSB of the result of the V90 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x3.

Table 8. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x01
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 501E to 0x00 5049	Reserved area (28 bytes)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52D2	TIM1	TIM1_DCR2	TIM1 DMA1 control register 2	0x00
0x00 52D3		TIM1_DMA1R	TIM1 DMA1 address for burst mode	0x00
0x00 52D4 to 0x00 52DF	Reserved area (12 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 bytes)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5300 to 0x00 533F	Reserved area (64 bytes)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00

9.3.2 Embedded reset and power control block characteristics

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	BOR detector enabled	0(1)	-	∞(1)	µs/V
	V_{DD} fall time rate	BOR detector enabled	20(1)	-	∞(1)	
t_{TEMP}	Reset release delay	V_{DD} rising BOR detector enabled	-	3	-	ms
		V_{DD} rising BOR detector disabled	-	1	-	
V_{PDR}	Power-down reset threshold	Falling edge	1.30(2)	1.50	1.65	V
V_{BOR0}	Brown-out reset threshold 0 (BOR_TH[2:0]=000)	Falling edge	1.67	1.70	1.74	V
		Rising edge	1.69	1.75	1.80	
V_{BOR1}	Brown-out reset threshold 1 (BOR_TH[2:0]=001)	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.04	2.07	
V_{BOR2}	Brown-out reset threshold 2 (BOR_TH[2:0]=010)	Falling edge	2.22	2.3	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3 (BOR_TH[2:0]=011)	Falling edge	2.45	2.55	2.60	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4 (BOR_TH[2:0]=100)	Falling edge	2.68	2.80	2.85	
		Rising edge	2.78	2.90	2.95	
V_{PVD0}	PVD threshold 0	Falling edge	1.80	1.84	1.88	V
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.2	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	
		Rising edge	3.08	3.15	3.20	

In the following table, data is based on characterization results, unless otherwise specified.

Table 22. Total current consumption and timing in Low power run mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions[1]			Typ	Max	Unit
$I_{DD(LPR)}$	Supply current in Low power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.1	5.4	µA
				T_A = 55 °C	5.7	6	
				T_A = 85 °C	6.8	7.5	
				T_A = 105 °C	9.2	10.4	
				T_A = 125 °C	13.4	16.6	
			with TIM2 active[2]	T_A = -40 °C to 25 °C	5.4	5.7	
				T_A = 55 °C	6.0	6.3	
				T_A = 85 °C	7.2	7.8	
				T_A = 105 °C	9.4	10.7	
				T_A = 125 °C	13.8	17	
		LSE [3] external clock (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.25	5.6	
				T_A = 55 °C	5.67	6.1	
				T_A = 85 °C	5.85	6.3	
				T_A = 105 °C	7.11	7.6	
				T_A = 125 °C	9.84	12	
			with TIM2 active [2]	T_A = -40 °C to 25 °C	5.59	6	
				T_A = 55 °C	6.10	6.4	
				T_A = 85 °C	6.30	7	
				T_A = 105 °C	7.55	8.4	
				T_A = 125 °C	10.1	15	

1. No floating I/Os
2. Timer 2 clock enabled and counter running
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*

HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Motional resistance (see crystal specification), L_m: Motional inductance (see crystal specification),
C_m: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification),
C_{L1}=C_{L2}=C: Grounded external capacitance
g_m >> g_{mcrit}

LSE crystal/ceramic resonator oscillator

The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 32. LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	ΔV = 200 mV	-	1.2	-	MΩ
C(1)	Recommended load capacitance (2)	-	-	8	-	pF
$I_{DD(LSE)}$	LSE oscillator power consumption	-	-	-	1.4(3)	µA
		V_{DD} = 1.8 V	-	450	-	nA
		V_{DD} = 3 V	-	600	-	
		V_{DD} = 3.6 V	-	750	-	
g_m	Oscillator transconductance	-	3(3)	-	-	µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	s

1. C=C_{L1}=C_{L2} is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details.
3. Data guaranteed by design.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

NRST pin

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage (1)	I_{OL} = 2 mA for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA for V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis(3)	-	10%V_{DD} (2)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor (1)	-	30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse (3)	-	-	-	50	ns
$V_{NF(NRST)}$	NRST input not filtered pulse (3)	-	300	-	-	

1. Data based on characterization results.
2. 200 mV min.
3. Data guaranteed by design.

Figure 31. Typical NRST pull-up resistance R_{PU} vs V_{DD}

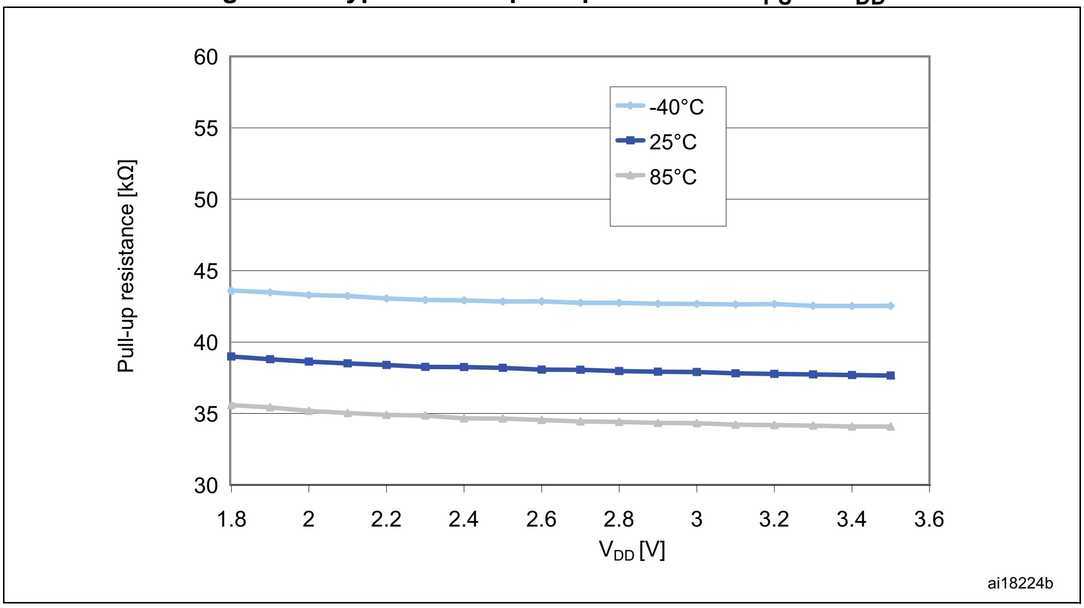
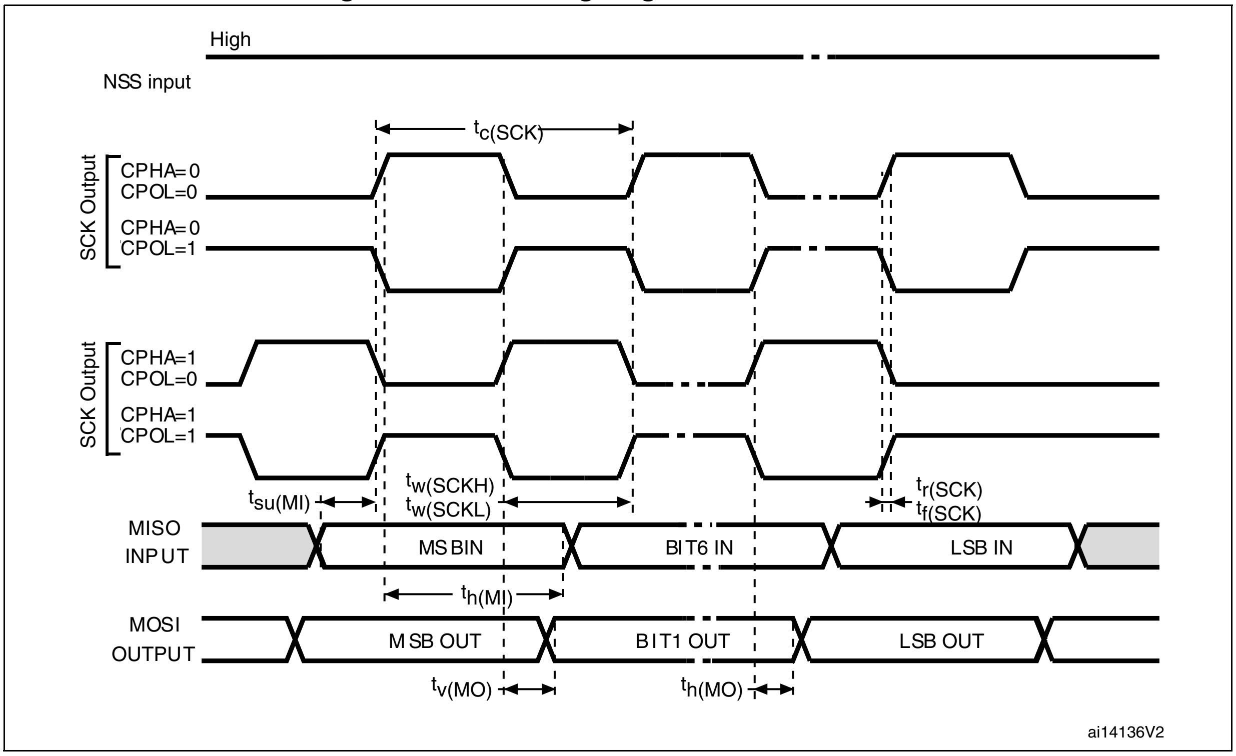


Figure 36. SPI1 timing diagram - master mode(1)

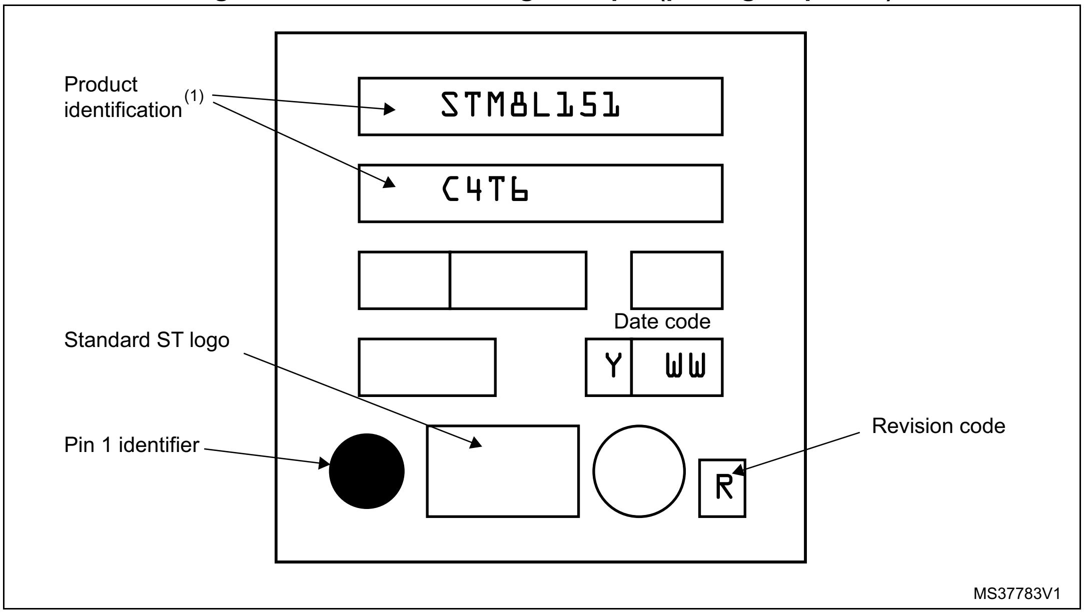


1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 45. LQFP48 marking example (package top view)

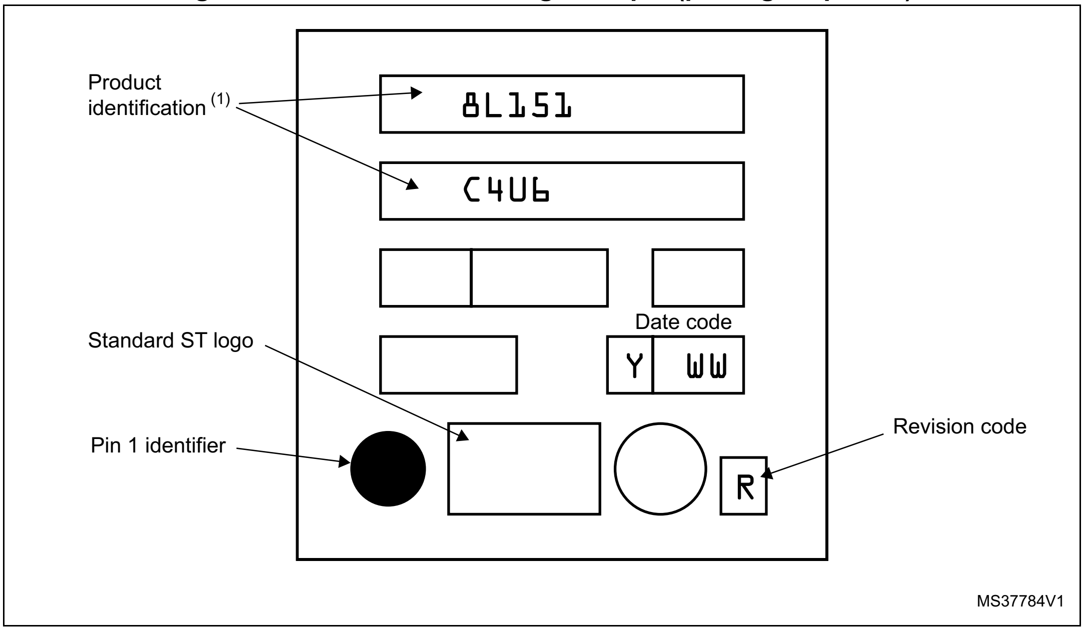


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 48. UFQFPN48 marking example (package top view)

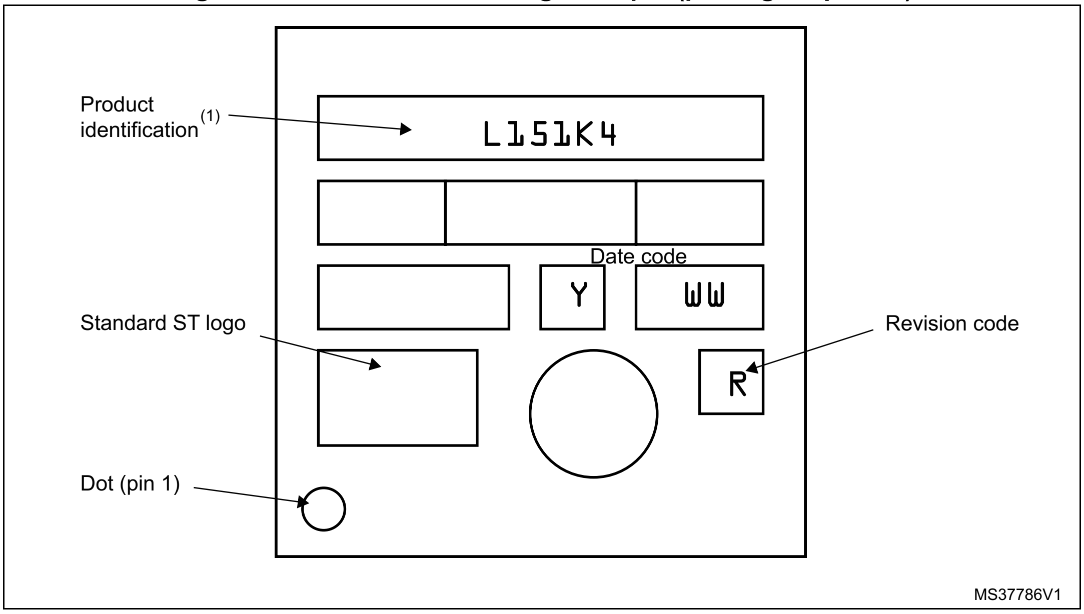


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 54. UFQFPN32 marking example (package top view)

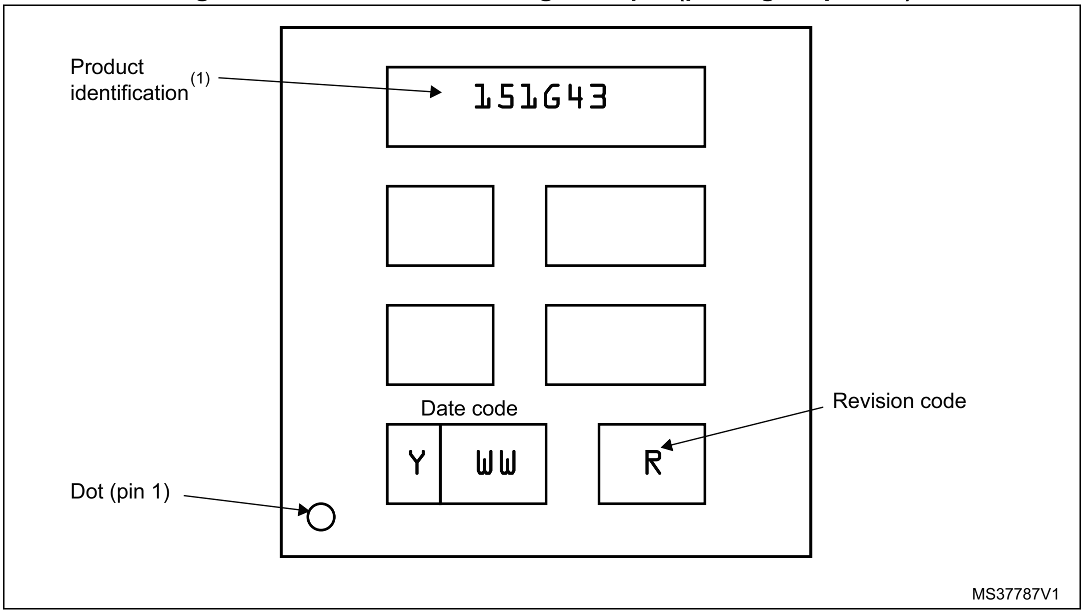


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 57. UFQFPN28 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 67. WLCSP28 - 28-pin, 1.703 x 2.841 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.540	0.570	0.600	0.0213	0.0224	0.0236
A1	-	0.190	-	-	0.0075	-
A2	-	0.380	-	-	0.0150	-
b(2)	0.240	0.270	0.300	0.0094	0.0106	0.0118
D	1.668	1.703	1.738	0.0657	0.0670	0.0684
E	2.806	2.841	2.876	0.1105	0.1119	0.1132
e	-	0.400	-	-	0.0157	-
e1	-	1.200	-	-	0.0472	-
e2	-	2.400	-	-	0.0945	-
F	-	0.251	-	-	0.0099	-
G	-	0.222	-	-	0.0087	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.