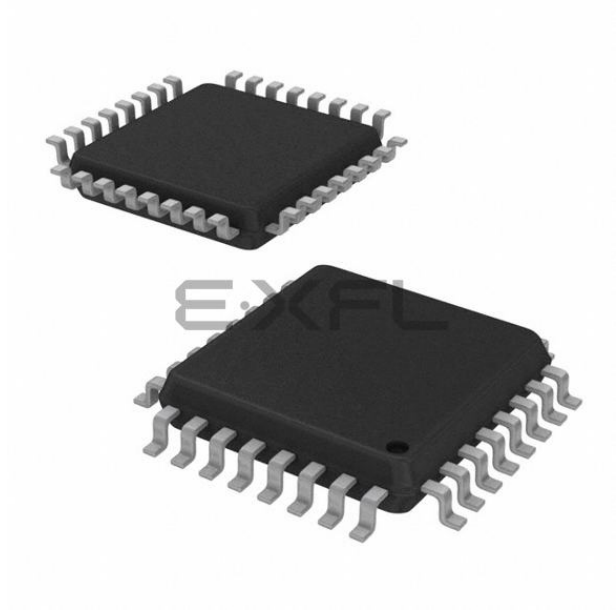

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l152k6t3

List of tables

3.2 Central processing unit STM8

3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The medium-density STM8L151x4/6 and STM8L152x4/6 feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1}; V_{DD1} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD1} pins, the corresponding ground pin is V_{SS1}.
- $V_{SSA;}$ V_{DDA} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{SS2}; V_{DD2} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for I/Os. V_{DD2} and V_{SS2} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{REF+}; V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.
- V_{REF+} (for DAC): external voltage reference for DAC must be provided externally through V_{REF+}.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min value at power down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains under reset when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The medium-density STM8L151x4/6 and STM8L152x4/6 embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

Table 4. Legend/abbreviation for table 5

Type	I= input, O = output, S = power supply	
Level	FT	Five-volt tolerant
	TT	3.6 V tolerant
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
2	1	1	C3	NRST/PA1(1)	I/O			**X**		HS		X	**Reset**	PA1
3	2	2	B4	PA2/OSC_IN/ *[USART1_TX]*(4)/ *[SPI1_MISO]* (4)	I/O		**X**	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out] /*
4	3	3	C4	PA3/OSC_OUT/*[USART1_RX]*(4)/*[SPI1_MOSI]*(4)	I/O		**X**	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/*
5	-	-	-	PA4/TIM2_BKIN/ LCD_COM0(2)/ADC1_IN2/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input / LCD COM 0 / ADC1 input 2 / Comparator 1 positive input
-	4	4	D3	PA4/TIM2_BKIN/ *[TIM2_ETR]*(4)/ LCD_COM0(2)/ ADC1_IN2/COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input / *[Timer 2 - external trigger]* / LCD_COM 0 / ADC1 input 2 / Comparator 1 positive input
6	-	-	-	PA5/TIM3_BKIN/ LCD_COM1(2)/ADC1_IN1/ COMP1_INP	I/O	TT (3)	**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input / LCD_COM 1 / ADC1 input 1/ Comparator 1 positive input

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5200	SPI1	SPI1_CR1	SPI1 control register 1	0x00
0x00 5201		SPI1_CR2	SPI1 control register 2	0x00
0x00 5202		SPI1_ICR	SPI1 interrupt control register	0x00
0x00 5203		SPI1_SR	SPI1 status register	0x02
0x00 5204		SPI1_DR	SPI1 data register	0x00
0x00 5205		SPI1_CRCPR	SPI1 CRC polynomial register	0x07
0x00 5206		SPI1_RXCRCR	SPI1 Rx CRC register	0x00
0x00 5207		SPI1_TXCRCR	SPI1 Tx CRC register	0x00
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C1	I2C1_CR1	I2C1 control register 1	0x00
0x00 5211		I2C1_CR2	I2C1 control register 2	0x00
0x00 5212		I2C1_FREQR	I2C1 frequency register	0x00
0x00 5213		I2C1_OARL	I2C1 own address register low	0x00
0x00 5214		I2C1_OARH	I2C1 own address register high	0x00
0x00 5215		Reserved (1 byte)		
0x00 5216		I2C1_DR	I2C1 data register	0x00
0x00 5217		I2C1_SR1	I2C1 status register 1	0x00
0x00 5218		I2C1_SR2	I2C1 status register 2	0x00
0x00 5219		I2C1_SR3	I2C1 status register 3	0x0x
0x00 521A		I2C1_ITR	I2C1 interrupt control register	0x00
0x00 521B		I2C1_CCRL	I2C1 clock control register low	0x00
0x00 521C		I2C1_CCRH	I2C1 clock control register high	0x00
0x00 521D		I2C1_TRISER	I2C1 TRISE register	0x02
0x00 521E		I2C1_PECR	I2C1 packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 534E	ADC1	ADC1_TRIGR1	ADC1 trigger disable 1	0x00
0x00 534F		ADC1_TRIGR2	ADC1 trigger disable 2	0x00
0x00 5350		ADC1_TRIGR3	ADC1 trigger disable 3	0x00
0x00 5351		ADC1_TRIGR4	ADC1 trigger disable 4	0x00
0x00 5352 to 0x00 537F	Reserved area (46 bytes)			
0x00 5380	DAC	DAC_CR1	DAC control register 1	0x00
0x00 5381		DAC_CR2	DAC control register 2	0x00
0x00 5382 to 0x00 5383		Reserved area (2 bytes)		
0x00 5384		DAC_SWTRIGR	DAC software trigger register	0x00
0x00 5385		DAC_SR	DAC status register	0x00
0x00 5386 to 0x00 5387		Reserved area (2 bytes)		
0x00 5388		DAC_RDHRH	DAC right aligned data holding register high	0x00
0x00 5389		DAC_RDHRL	DAC right aligned data holding register low	0x00
0x00 538A to 0x00 538B		Reserved area (2 bytes)		
0x00 538C		DAC_LDHRH	DAC left aligned data holding register high	0x00
0x00 538D		DAC_LDHRL	DAC left aligned data holding register low	0x00
0x00 538E to 0x00 538F		Reserved area (2 bytes)		
0x00 5390		DAC_DHR8	DAC 8-bit data holding register	0x00
0x00 5391 to 0x00 53AB		Reserved area (27 bytes)		
0x00 53AC		DAC_DORH	DAC data output register high	0x00
0x00 53AD		DAC_DORL	DAC data output register low	0x00
0x00 53AE to 0x00 53FF	Reserved area (82 bytes)			

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option bytes can also be modified 'on the fly' by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 12. Option byte addresses

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved										0x00
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x00
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

Table 20. Total current consumption in Run mode

Symbol	Parameter	Conditions(1)			Typ	Max				Unit
						55 °C	85 °C(2)	105°C(3)	125 °C(4)	
$I_{DD(RUN)}$	Supply current in run mode(5)	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)(6)	f_{CPU} = 125 kHz	0.39	0.47	0.49	0.52	0.55	mA
				f_{CPU} = 1 MHz	0.48	0.56	0.58	0.61	0.65	
				f_{CPU} = 4 MHz	0.75	0.84	0.86	0.91	0.99	
				f_{CPU} = 8 MHz	1.10	1.20	1.25	1.31	1.40	
				f_{CPU} = 16 MHz	1.85	1.93	2.12(8)	2.29(8)	2.36(8)	
			HSE external clock ($f_{CPU}=f_{HSE}$)(7)	f_{CPU} = 125 kHz	0.05	0.06	0.09	0.11	0.12	
				f_{CPU} = 1 MHz	0.18	0.19	0.20	0.22	0.23	
				f_{CPU} = 4 MHz	0.55	0.62	0.64	0.71	0.77	
				f_{CPU} = 8 MHz	0.99	1.20	1.21	1.22	1.24	
				f_{CPU} = 16 MHz	1.90	2.22	2.23(8)	2.24(8)	2.28(8)	
			LSI RC osc. (typ. 38 kHz)	$f_{CPU} = f_{LSI}$	0.040	0.045	0.046	0.048	0.050	
			LSE external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.035	0.040	0.048(8)	0.050	0.062	
$I_{DD(RUN)}$	Supply current in Run mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI RC osc.(9)	f_{CPU} = 125 kHz	0.43	0.55	0.56	0.58	0.62	mA
				f_{CPU} = 1 MHz	0.60	0.77	0.80	0.82	0.87	
				f_{CPU} = 4 MHz	1.11	1.34	1.37	1.39	1.43	
				f_{CPU} = 8 MHz	1.90	2.20	2.23	2.31	2.40	
				f_{CPU} = 16 MHz	3.8	4.60	4.75	4.87	4.88	
			HSE external clock ($f_{CPU}=f_{HSE}$) (7)	f_{CPU} = 125 kHz	0.30	0.36	0.39	0.44	0.47	
				f_{CPU} = 1 MHz	0.40	0.50	0.52	0.55	0.56	
				f_{CPU} = 4 MHz	1.15	1.31	1.40	1.45	1.48	
				f_{CPU} = 8 MHz	2.17	2.33	2.44	2.56	2.77	
				f_{CPU} = 16 MHz	4.0	4.46	4.52	4.59	4.77	
			LSI RC osc.	$f_{CPU} = f_{LSI}$	0.110	0.123	0.130	0.140	0.150	
			LSE ext. clock (32.768 kHz)(10)	$f_{CPU} = f_{LSE}$	0.100	0.101	0.104	0.119	0.122	

1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU}=f_{SYSCLK}$
2. For devices with suffix 6
3. For devices with suffix 7
4. For devices with suffix 3

In the following table, data is based on characterization results, unless otherwise specified.

Table 21. Total current consumption in Wait mode

Symbol	Parameter	Conditions(1)			Typ	Max				Unit
						55°C	85 °C(2)	105 °C (3)	125 °C (4)	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from RAM with Flash in I_{DDQ} mode(5), V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.33	0.39	0.41	0.43	0.45	mA
				f_{CPU} = 1 MHz	0.35	0.41	0.44	0.45	0.48	
				f_{CPU} = 4 MHz	0.42	0.51	0.52	0.54	0.58	
				f_{CPU} = 8 MHz	0.52	0.57	0.58	0.59	0.62	
				f_{CPU} = 16 MHz	0.68	0.76	0.79	0.82 (7)	0.85 (7)	
			HSE external clock (f_{CPU}=f_{HSE}) (6)	f_{CPU} = 125 kHz	0.032	0.056	0.068	0.072	0.093	
				f_{CPU} = 1 MHz	0.078	0.121	0.144	0.163	0.197	
				f_{CPU} = 4 MHz	0.218	0.26	0.30	0.36	0.40	
				f_{CPU} = 8 MHz	0.40	0.52	0.57	0.62	0.66	
				f_{CPU} = 16 MHz	0.760	1.01	1.05	1.09 (7)	1.16 (7)	
			LSI	f_{CPU} = f_{LSI}	0.035	0.044	0.046	0.049	0.054	
			LSE(8) external clock (32.768 kHz)	f_{CPU} = f_{LSE}	0.032	0.036	0.038	0.044	0.051	

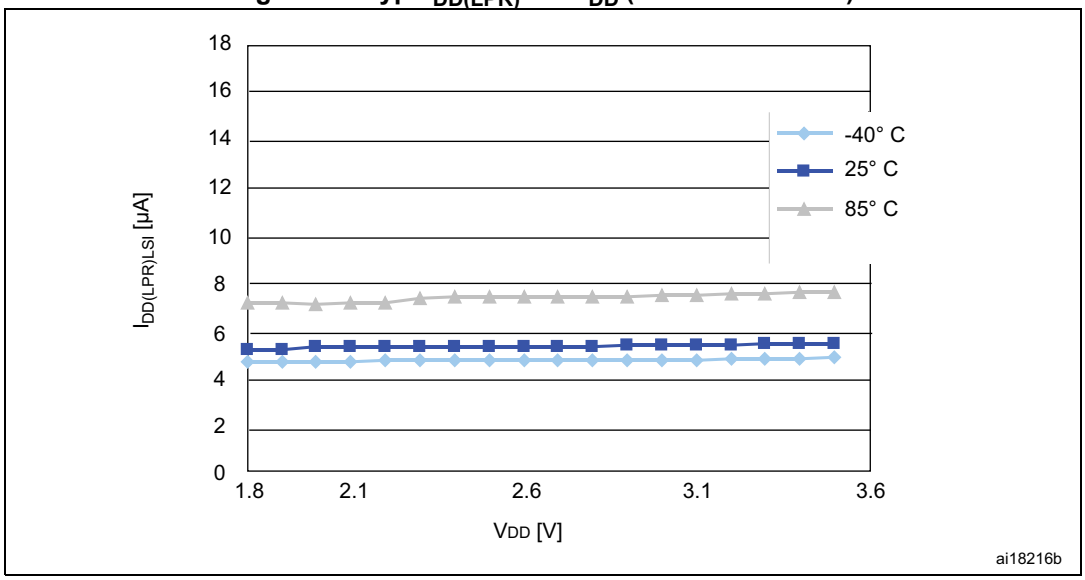
In the following table, data is based on characterization results, unless otherwise specified.

Table 22. Total current consumption and timing in Low power run mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions[1]			Typ	Max	Unit
$I_{DD(LPR)}$	Supply current in Low power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.1	5.4	µA
				T_A = 55 °C	5.7	6	
				T_A = 85 °C	6.8	7.5	
				T_A = 105 °C	9.2	10.4	
				T_A = 125 °C	13.4	16.6	
			with TIM2 active[2]	T_A = -40 °C to 25 °C	5.4	5.7	
				T_A = 55 °C	6.0	6.3	
				T_A = 85 °C	7.2	7.8	
				T_A = 105 °C	9.4	10.7	
				T_A = 125 °C	13.8	17	
		LSE [3] external clock (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.25	5.6	
				T_A = 55 °C	5.67	6.1	
				T_A = 85 °C	5.85	6.3	
				T_A = 105 °C	7.11	7.6	
				T_A = 125 °C	9.84	12	
			with TIM2 active [2]	T_A = -40 °C to 25 °C	5.59	6	
				T_A = 55 °C	6.10	6.4	
				T_A = 85 °C	6.30	7	
				T_A = 105 °C	7.55	8.4	
				T_A = 125 °C	10.1	15	

1. No floating I/Os
2. Timer 2 clock enabled and counter running
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*

Figure 15. Typ. $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source)



In the following table, data is based on characterization results, unless otherwise specified.

Table 23. Total current consumption in Low power wait mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions(1)			Typ	Max	Unit
$I_{DD(LPW)}$	Supply current in Low power wait mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	3	3.3	µA
				T_A = 55 °C	3.3	3.6	
				T_A = 85 °C	4.4	5	
				T_A = 105 °C	6.7	8	
				T_A = 125 °C	11	14	
			with TIM2 active(2)	T_A = -40 °C to 25 °C	3.4	3.7	
				T_A = 55 °C	3.7	4	
				T_A = 85 °C	4.8	5.4	
				T_A = 105 °C	7	8.3	
				T_A = 125 °C	11.3	14.5	
		LSE external clock(3) (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	2.35	2.7	
				T_A = 55 °C	2.42	2.82	
				T_A = 85 °C	3.10	3.71	
				T_A = 105 °C	4.36	5.7	
				T_A = 125 °C	7.20	11	
			with TIM2 active (2)	T_A = -40 °C to 25 °C	2.46	2.75	
				T_A = 55 °C	2.50	2.81	
				T_A = 85 °C	3.16	3.82	
				T_A = 105 °C	4.51	5.9	
				T_A = 125 °C	7.28	11	

1. No floating I/Os.
2. Timer 2 clock enabled and counter is running.
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*.

NRST pin

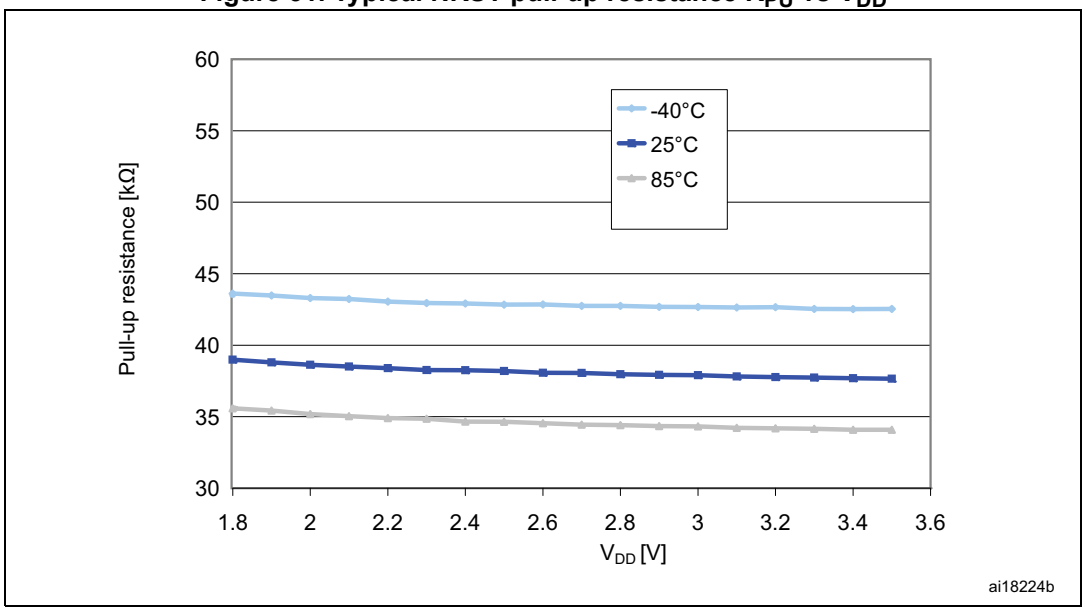
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. $\overline{\text{NRST}}$ pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage (1)	I_{OL} = 2 mA for 2.7 V ≤V_{DD} ≤3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA for V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis(3)	-	10%V_{DD} (2)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor (1)	-	30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse (3)	-	-	-	50	ns
$V_{NF(NRST)}$	NRST input not filtered pulse (3)	-	300	-	-	

1. Data based on characterization results.
2. 200 mV min.
3. Data guaranteed by design.

Figure 31. Typical NRST pull-up resistance R_{PU} vs V_{DD}



9.3.8 Communication interfaces

SPI1 - Serial peripheral interface

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, f_{SYSCLK} frequency and V_{DD} supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 43. SPI1 characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI1 clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI1 clock rise and fall time	Capacitive load: C = 30 pF	-	30	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x $1/f_{SYSCLK}$	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	80	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz	105	145	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	30	-	
		Slave mode	3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	15	-	
		Slave mode	0	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x $1/f_{SYSCLK}$	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	30	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	60	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	20	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	1	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

9.3.10 Embedded reference voltage

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 46. Reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	µA
$T_{S\_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(2)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202(3)	1.224	1.242(3)	V
I_{LPBUF}(2)	Internal reference voltage low power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(2)	Buffer output current(4)	-	-	-	1	µA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(2)	Internal reference voltage buffer startup time once enabled (1)	-	-	-	10	µs
$ACC_{VREFINT}$	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte(5)	-	-	-	± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	-40 °C ≤T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤T_A ≤ 50 °C	-	-	20	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours	-	-	-	TBD	ppm

1. Defined when ADC output reaches its final value ±1/2LSB
2. Data guaranteed by design.
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guaranty less than 1% V_{REFOUT} deviation.
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

Table 53. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time	V_{AIN} on PF0 fast channel V_{DDA} < 2.4 V	0.43(4)(5)	-	-	µs
		V_{AIN} on PF0 fast channel 2.4 V ≤V_{DDA}≤ 3.6 V	0.22(4)(5)	-	-	µs
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(4)(5)	-	-	µs
		V_{AIN} on slow channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.41(4)(5)	-	-	µs
t_{conv}	12-bit conversion time	-	12 + t_S			$1/f_{ADC}$
		16 MHz	1(4)			µs
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	µs
t_{IDLE}(6)	Time before a new conversion	T_A = +25 °C	-	-	1(7)	s
		T_A = +70 °C	-	-	20(7)	ms
		T_A = +125 °C	-	-	2(7)	ms
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 46*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} or V_{DDA} must be tied to ground.
3. Guaranteed by design.
4. Minimum sampling and conversion time is reached for maximum Rext = 0.5 kΩ
5. Value obtained for continuous conversion on fast channel.
6. The time between 2 conversions, or between ADC ON and the first conversion must be lower than t_{IDLE}.
7. The t_{IDLE} maximum value is ∞on the “Z” revision code of the device.

Table 62. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

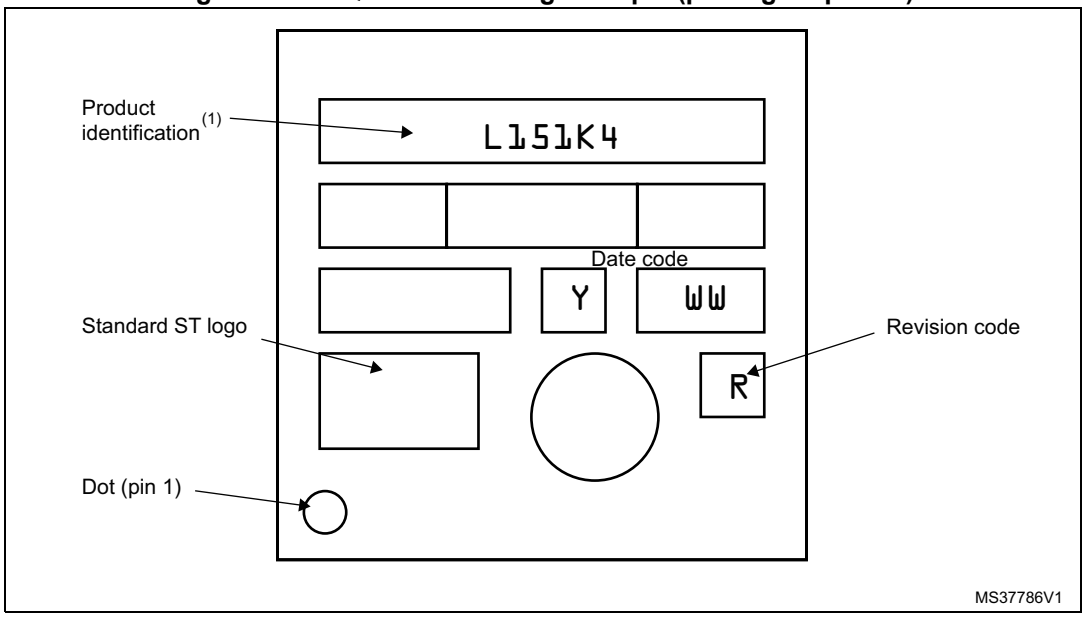
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

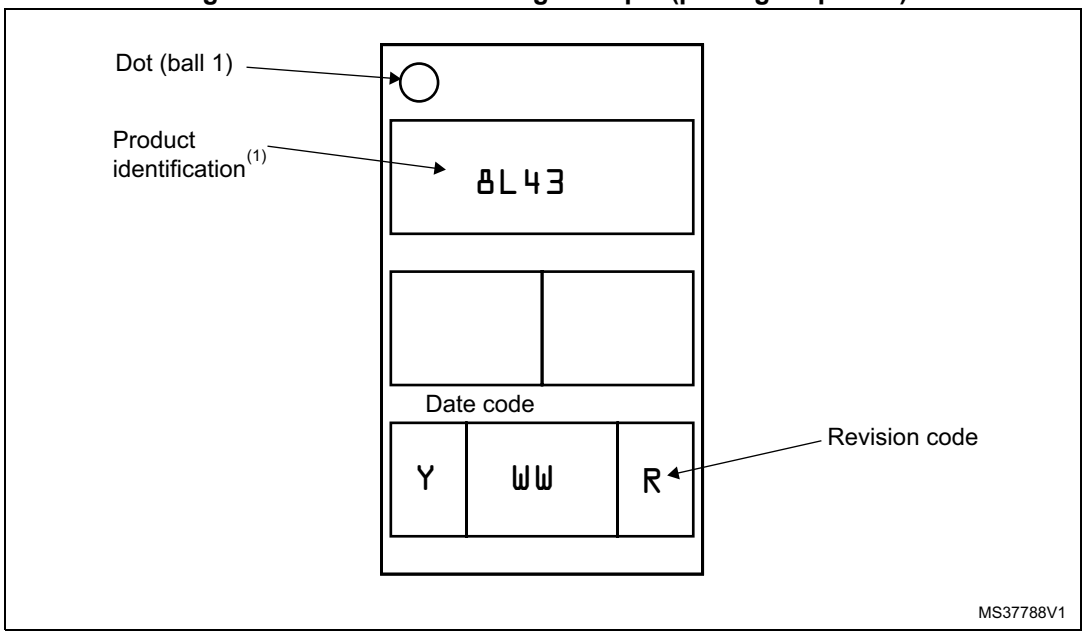
The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 54. UFQFPN32 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Figure 59. WLCSP28 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.