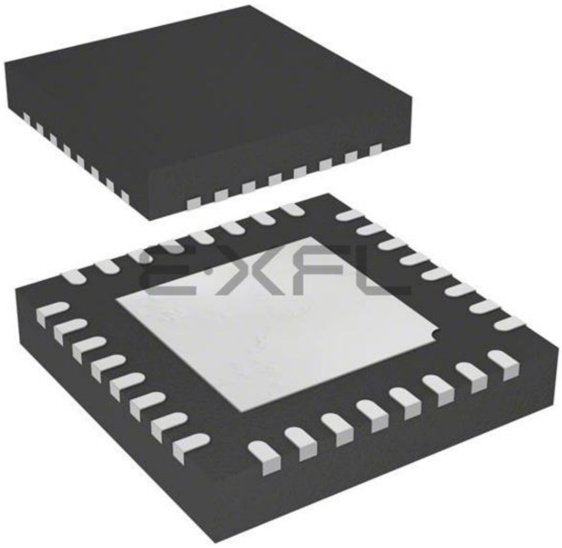

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l152k6u6

2 Description

The medium-density STM8L151x4/6 and STM8L152x4/6 devices are members of the STM8L ultra-low-power 8-bit family. The medium-density STM8L15x family operates from 1.8 V to 3.6 V (down to 1.65 V at power down) and is available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

The medium-density STM8L15x ultra-low-power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive In-Application debugging and ultra-fast Flash programming.

All medium-density STM8L15x microcontrollers feature embedded data EEPROM and low-power, low-voltage, single-supply program Flash memory.

They incorporate an extensive range of enhanced I/Os and peripherals.

The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

Six different packages are proposed from 28 to 48 pins. Depending on the device chosen, different sets of peripherals are included.

All STM8L ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

2.1 Device overview

Table 2. Medium-density STM8L151x4/6 and STM8L152x4/6 low-power device features and peripheral counts

Features		STM8L151Gx		STM8L15xKx		STM8L15xCx	
Flash (Kbyte)		16	32	16	32	16	32
Data EEPROM (Kbyte)		1					
RAM (Kbyte)		2					
LCD		No		4x17 (1)		4x28 (1)	
Timers	Basic	1 (8-bit)					
	General purpose	2 (16-bit)					
	Advanced control	1 (16-bit)					
Communication interfaces	SPI	1					
	I2C	1					
	USART	1					
GPIOs		26(3)		30 (2)(3) or 29 (1)(3)		41(3)	
12-bit synchronized ADC (number of channels)		1 (18)		1 (22 (2) or 21 (1))		1 (25)	
12-Bit DAC (number of channels)		1 (1)					
Comparators COMP1/COMP2		2					
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator					
CPU frequency		16 MHz					
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power down)					
Operating temperature		-40 to +85 °C/ -40 to +105 °C / -40 to +125 °C					
Packages		UFQFPN28 (4x4; 0.6 mm thickness) WLCSP28		LQFP32(7x7) UFQFPN32 (5x5; 0.6 mm thickness)		LQFP48 UFQFPN48 (4x4; 0.6 mm thickness)	

1. STM8L152xx versions only
2. STM8L151xx versions only
3. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

IWDG: Independent watchdog
LCD: Liquid crystal display
POR/PDR: Power on reset / power down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

3.1 Low-power modes

The medium-density STM8L151x4/6 and STM8L152x4/6 devices support five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: The CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt, event or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode). Wait consumption: refer to *Table 21*.
- **Low power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power run mode consumption: refer to *Table 22*.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power wait mode consumption: refer to *Table 23*.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset. Active-halt consumption: refer to *Table 24* and *Table 25*.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs. Halt consumption: refer to *Table 26*.

3.19 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The single-wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

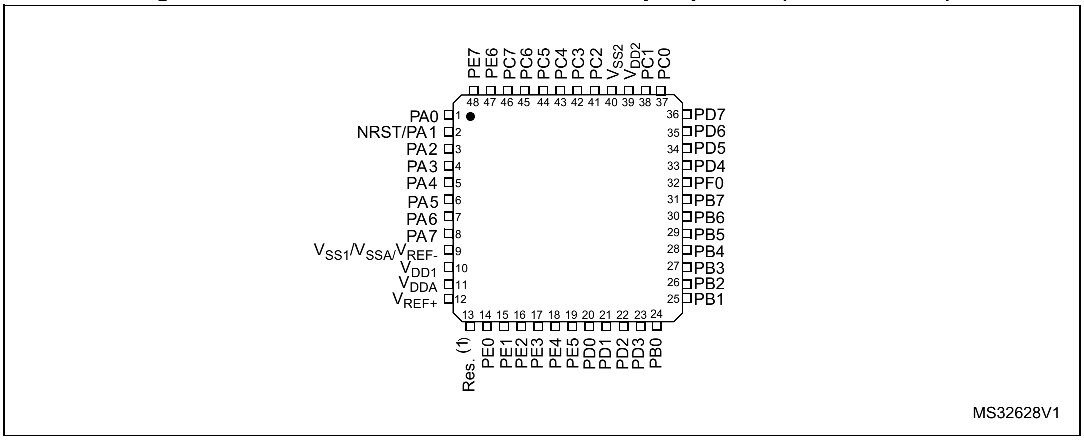
The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1 interface. The reference document for the bootloader is *UM0560: STM8 bootloader user manual*.

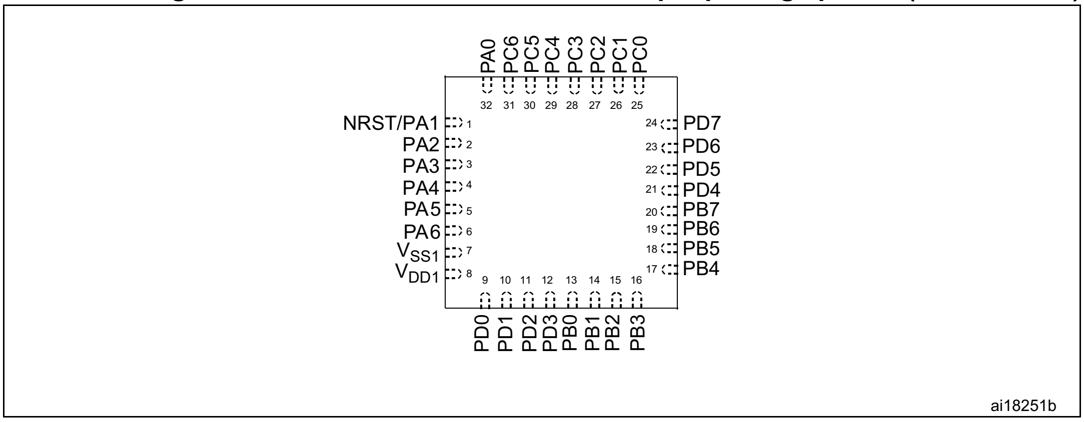
4 Pinout and pin description

Figure 3. STM8L151C4, STM8L151C6 48-pin pinout (without LCD)



1. Reserved. Must be tied to V_{DD}.

Figure 4. STM8L151K4, STM8L151K6 32-pin package pinout (without LCD)



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.

Figure 5. STM8L151Gx UFQFPN28 package pinout

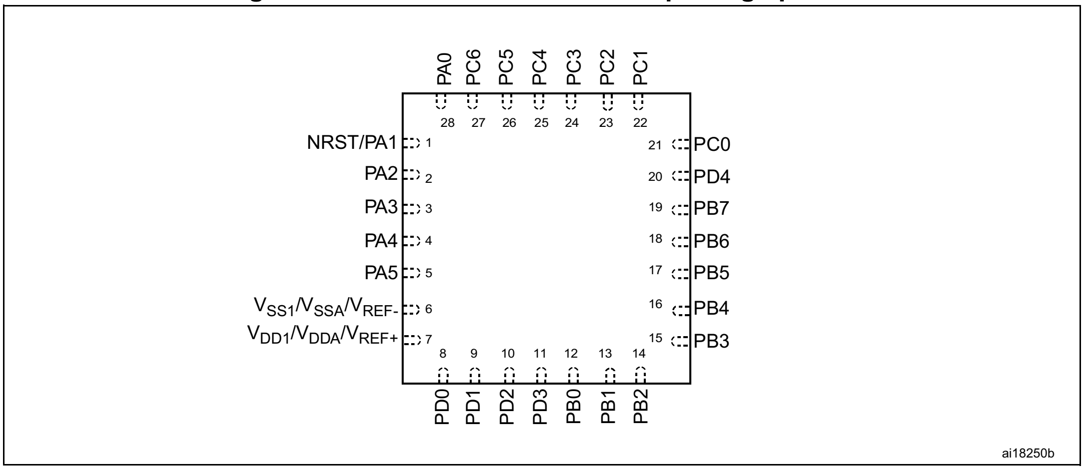


Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_DIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00
0x00 50C2		CLK_ICKR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x80
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0bxxxx0000
0x00 50CA		CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0xxx
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11100x

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5200	SPI1	SPI1_CR1	SPI1 control register 1	0x00
0x00 5201		SPI1_CR2	SPI1 control register 2	0x00
0x00 5202		SPI1_ICR	SPI1 interrupt control register	0x00
0x00 5203		SPI1_SR	SPI1 status register	0x02
0x00 5204		SPI1_DR	SPI1 data register	0x00
0x00 5205		SPI1_CRCPR	SPI1 CRC polynomial register	0x07
0x00 5206		SPI1_RXCRCR	SPI1 Rx CRC register	0x00
0x00 5207		SPI1_TXCRCR	SPI1 Tx CRC register	0x00
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C1	I2C1_CR1	I2C1 control register 1	0x00
0x00 5211		I2C1_CR2	I2C1 control register 2	0x00
0x00 5212		I2C1_FREQR	I2C1 frequency register	0x00
0x00 5213		I2C1_OARL	I2C1 own address register low	0x00
0x00 5214		I2C1_OARH	I2C1 own address register high	0x00
0x00 5215		Reserved (1 byte)		
0x00 5216		I2C1_DR	I2C1 data register	0x00
0x00 5217		I2C1_SR1	I2C1 status register 1	0x00
0x00 5218		I2C1_SR2	I2C1 status register 2	0x00
0x00 5219		I2C1_SR3	I2C1 status register 3	0x0x
0x00 521A		I2C1_ITR	I2C1 interrupt control register	0x00
0x00 521B		I2C1_CCRL	I2C1 clock control register low	0x00
0x00 521C		I2C1_CCRH	I2C1 clock control register high	0x00
0x00 521D		I2C1_TRISER	I2C1 TRISE register	0x02
0x00 521E		I2C1_PECR	I2C1 packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	USART1	USART1_SR	USART1 status register	0xC0
0x00 5231		USART1_DR	USART1 data register	undefined
0x00 5232		USART1_BRR1	USART1 baud rate register 1	0x00
0x00 5233		USART1_BRR2	USART1 baud rate register 2	0x00
0x00 5234		USART1_CR1	USART1 control register 1	0x00
0x00 5235		USART1_CR2	USART1 control register 2	0x00
0x00 5236		USART1_CR3	USART1 control register 3	0x00
0x00 5237		USART1_CR4	USART1 control register 4	0x00
0x00 5238		USART1_CR5	USART1 control register 5	0x00
0x00 5239		USART1_GTR	USART1 guard time register	0x00
0x00 523A		USART1_PSCR	USART1 prescaler register	0x00
0x00 523B to 0x00 524F	Reserved area (21 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52B0	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 52B1		TIM1_CR2	TIM1 control register 2	0x00
0x00 52B2		TIM1_SMCR	TIM1 Slave mode control register	0x00
0x00 52B3		TIM1_ETR	TIM1 external trigger register	0x00
0x00 52B4		TIM1_DER	TIM1 DMA1 request enable register	0x00
0x00 52B5		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 52B6		TIM1_SR1	TIM1 status register 1	0x00
0x00 52B7		TIM1_SR2	TIM1 status register 2	0x00
0x00 52B8		TIM1_EGR	TIM1 event generation register	0x00
0x00 52B9		TIM1_CCMR1	TIM1 Capture/Compare mode register 1	0x00
0x00 52BA		TIM1_CCMR2	TIM1 Capture/Compare mode register 2	0x00
0x00 52BB		TIM1_CCMR3	TIM1 Capture/Compare mode register 3	0x00
0x00 52BC		TIM1_CCMR4	TIM1 Capture/Compare mode register 4	0x00
0x00 52BD		TIM1_CCER1	TIM1 Capture/Compare enable register 1	0x00
0x00 52BE		TIM1_CCER2	TIM1 Capture/Compare enable register 2	0x00
0x00 52BF		TIM1_CNTRH	TIM1 counter high	0x00
0x00 52C0		TIM1_CNTRL	TIM1 counter low	0x00
0x00 52C1		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 52C2		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 52C3		TIM1_ARRH	TIM1 Auto-reload register high	0xFF
0x00 52C4		TIM1_ARRL	TIM1 Auto-reload register low	0xFF
0x00 52C5		TIM1_RCR	TIM1 Repetition counter register	0x00
0x00 52C6		TIM1_CCR1H	TIM1 Capture/Compare register 1 high	0x00
0x00 52C7		TIM1_CCR1L	TIM1 Capture/Compare register 1 low	0x00
0x00 52C8		TIM1_CCR2H	TIM1 Capture/Compare register 2 high	0x00
0x00 52C9		TIM1_CCR2L	TIM1 Capture/Compare register 2 low	0x00
0x00 52CA		TIM1_CCR3H	TIM1 Capture/Compare register 3 high	0x00
0x00 52CB		TIM1_CCR3L	TIM1 Capture/Compare register 3 low	0x00
0x00 52CC		TIM1_CCR4H	TIM1 Capture/Compare register 4 high	0x00
0x00 52CD		TIM1_CCR4L	TIM1 Capture/Compare register 4 low	0x00
0x00 52CE		TIM1_BKR	TIM1 break register	0x00
0x00 52CF		TIM1_DTR	TIM1 dead-time register	0x00
0x00 52D0		TIM1_OISR	TIM1 output idle state register	0x00
0x00 52D1		TIM1_DCR1	DMA1 control register 1	0x00

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	- 5 / +0	mA
	Injected current on five-volt tolerant (FT) pins (PA7 and PE0) (1)	- 5 / +0	
	Injected current on 3.6 V tolerant (TT) pins (1)	- 5 / +0	
	Injected current on any other pin (2)	- 5 / +5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) (3)	± 25	

1. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15.* for maximum allowed input voltage values.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15.* for maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

Table 28. Current consumption under external reset

Symbol	Parameter	Conditions		Typ	Unit
$I_{DD(RST)}$	Supply current under external reset (1)	All pins are externally tied to V_{DD}	V_{DD} = 1.8 V	48	µA
			V_{DD} = 3 V	76	
			V_{DD} = 3.6 V	91	

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset.

9.3.4 Clock and timing characteristics

HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 29. HSE external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency(1)	-	1	-	16	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7 x V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	0.3 x V_{DD}	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	2.6	-	pF
I_{LEAK_HSE}	OSC_IN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-	-	±1	µA

1. Data guaranteed by design.

LSE external clock (LSEBYP=1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 30. LSE external clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency(1)	-	32.768	-	kHz
V_{LSEH}(2)	OSC32_IN input pin high level voltage	0.7 x V_{DD}	-	V_{DD}	V
V_{LSEL}(2)	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 x V_{DD}	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	0.6	-	pF
I_{LEAK_LSE}	OSC32_IN input leakage current	-	-	±1	µA

1. Data guaranteed by design.
2. Data based on characterization results.

HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Motional resistance (see crystal specification), L_m: Motional inductance (see crystal specification),
C_m: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification),
C_{L1}=C_{L2}=C: Grounded external capacitance
$g_m >> g_{mcrit}$

LSE crystal/ceramic resonator oscillator

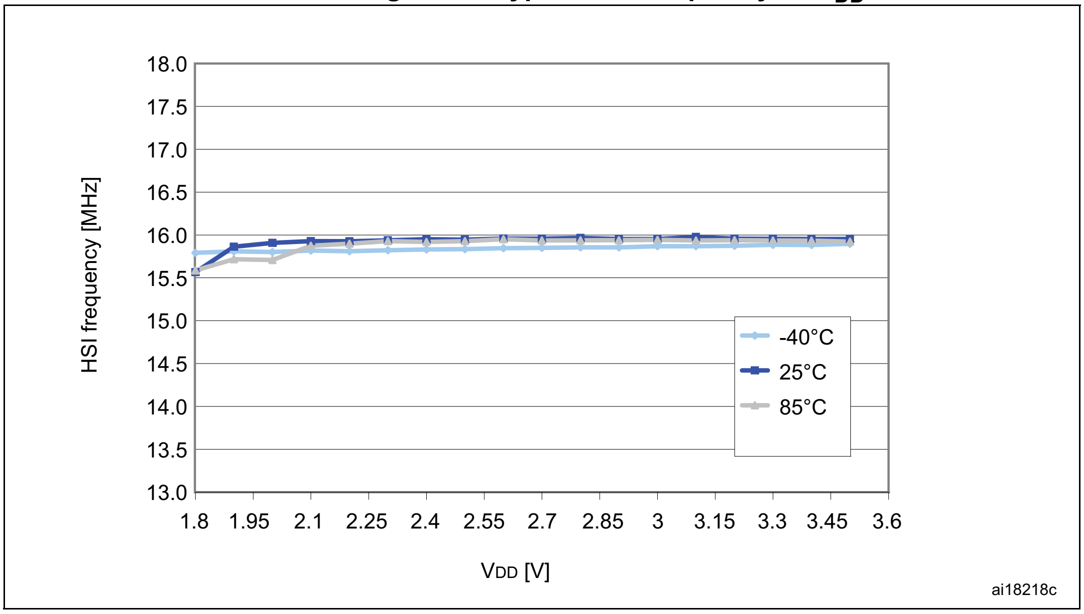
The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 32. LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	ΔV = 200 mV	-	1.2	-	MΩ
C(1)	Recommended load capacitance (2)	-	-	8	-	pF
$I_{DD(LSE)}$	LSE oscillator power consumption	-	-	-	1.4(3)	µA
		V_{DD} = 1.8 V	-	450	-	nA
		V_{DD} = 3 V	-	600	-	
		V_{DD} = 3.6 V	-	750	-	
g_m	Oscillator transconductance	-	3(3)	-	-	µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	s

1. C=C_{L1}=C_{L2} is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details.
3. Data guaranteed by design.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 19. Typical HSI frequency vs V_{DD}



Low speed internal RC oscillator (LSI)

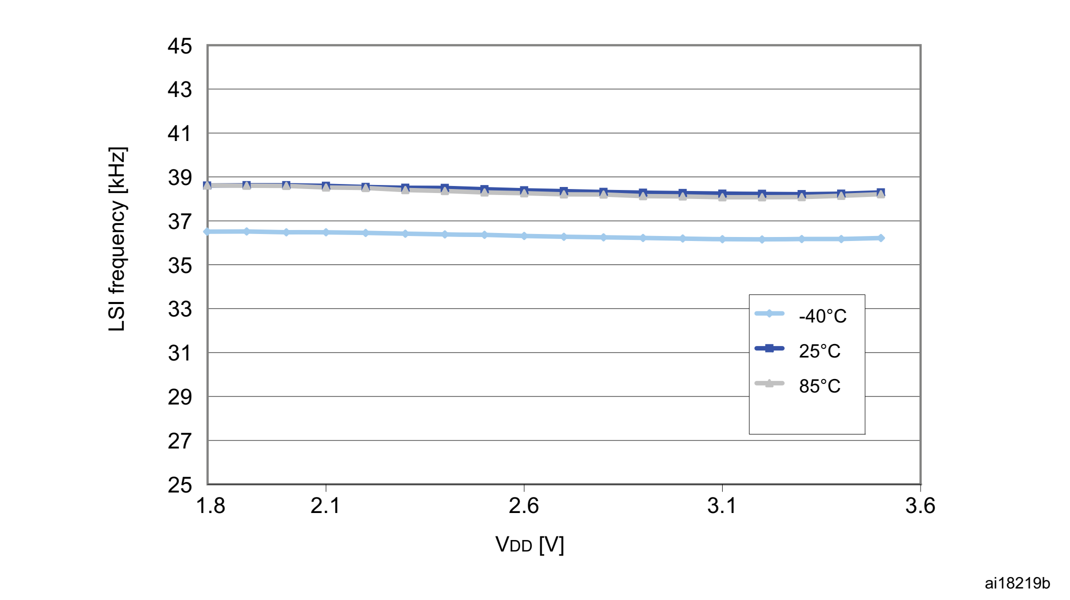
In the following table, data is based on characterization results, not tested in production.

Table 34. LSI oscillator characteristics

Symbol	Parameter (1)	Conditions(1)	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	200(2)	µs
$I_{DD(LSI)}$	LSI oscillator frequency drift(3)	$0\ °C \leq T_A \leq 85\ °C$	-12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

Figure 20. Typical LSI frequency vs. V_{DD}



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
High sink	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	V
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	V
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	V
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	V

1. The I_{IO} current sink must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 40. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

1. The I_{IO} current sink must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 41. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

1. The I_{IO} current sink must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

9.3.11 Temperature sensor

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 47. TS characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{90}(1)	Sensor reference voltage at 90°C ±5 °C,	0.580	0.597	0.614	V
T_L	V_{SENSOR} linearity with temperature	-	±1	±2	°C
Avg_slope (2)	Average slope	1.59	1.62	1.65	mV/°C
$I_{DD(TEMP)}$(2)	Consumption	-	3.4	6	µA
T_{START}(2)(3)	Temperature sensor startup time	-	-	10	µs
T_{S_TEMP}(2)	ADC sampling time when reading the temperature sensor	10	-	-	µs

1. Tested in production at V_{DD} = 3 V ±10 mV. The 8 LSB of the V_{90} ADC conversion result are stored in the TS_Factory_CONV_V90 byte.
2. Data guaranteed by design.
3. Defined for ADC output reaching its final value ±1/2LSB.

9.3.12 Comparator characteristics

In the following table, data is guaranteed by design, not tested in production, unless otherwise specified.

Table 48. Comparator 1 characteristics

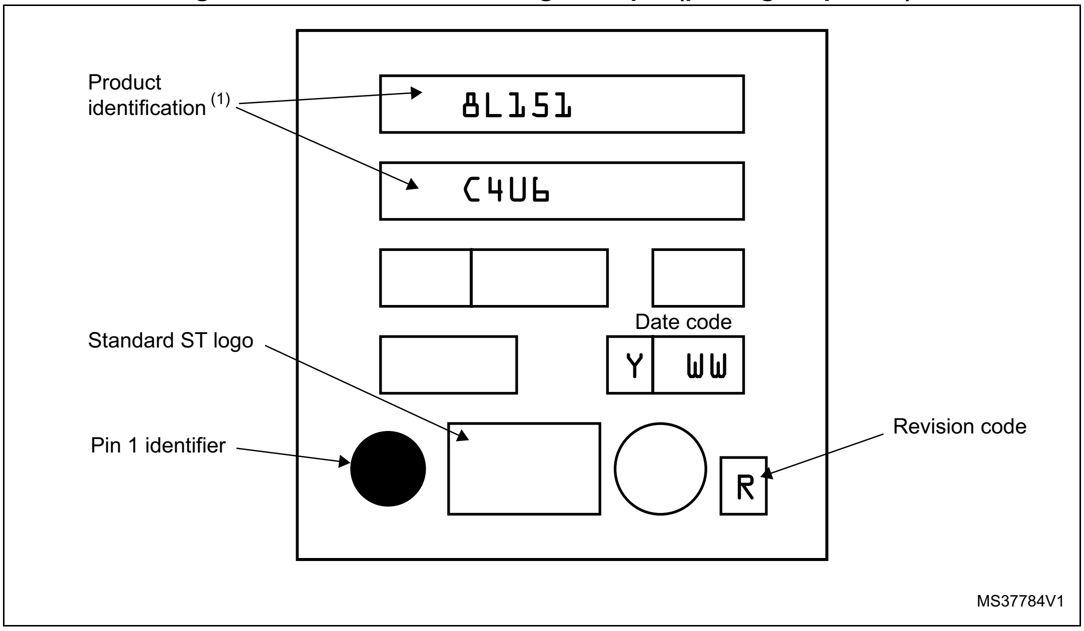
Symbol	Parameter	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	1.65	-	3.6	V
T_A	Temperature range	-40	-	125	°C
R_{400K}	R_{400K} value	300	400	500	kΩ
R_{10K}	R_{10K} value	7.5	10	12.5	
V_{IN}	Comparator 1 input voltage range	0.6	-	V_{DDA}	V
V_{REFINT}	Internal reference voltage(2)	1.202	1.224	1.242	
t_{START}	Comparator startup time	-	7	10	µs
t_d	Propagation delay(3)	-	3	10	
V_{offset}	Comparator offset error	-	±3	±10	mV
I_{COMP1}	Current consumption(4)	-	160	260	nA

1. Based on characterization.
2. Tested in production at V_{DD} = 3 V ±10 mV.
3. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
4. Comparator consumption only. Internal reference voltage not included.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 48. UFQFPN48 marking example (package top view)

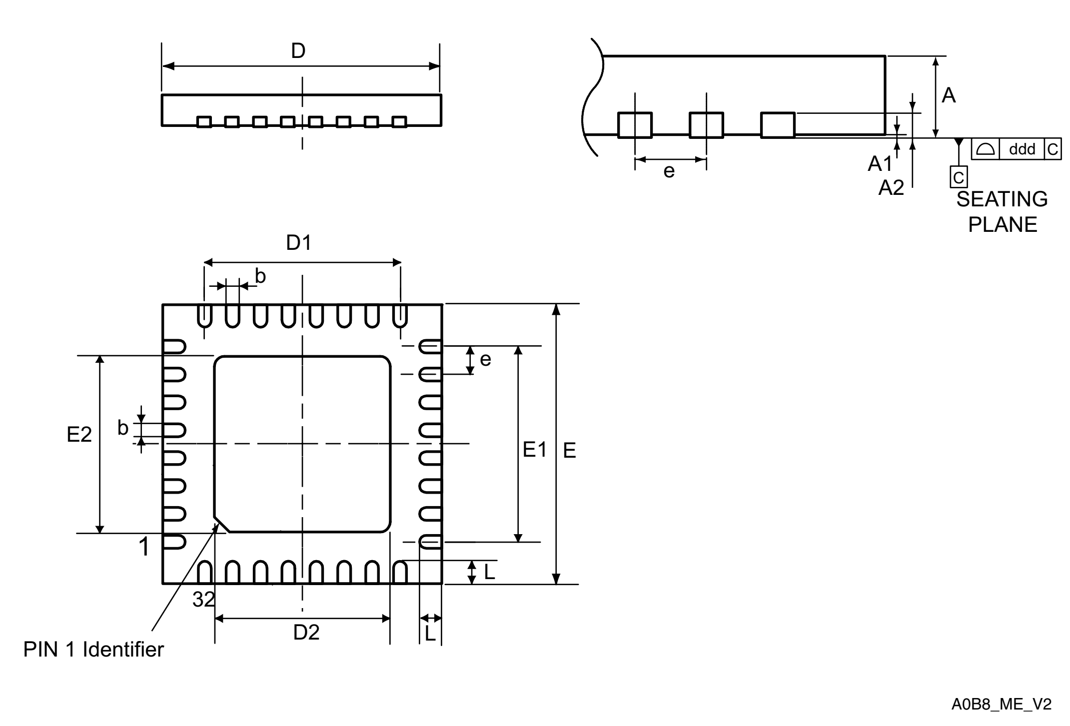


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Samples to run qualification activity.

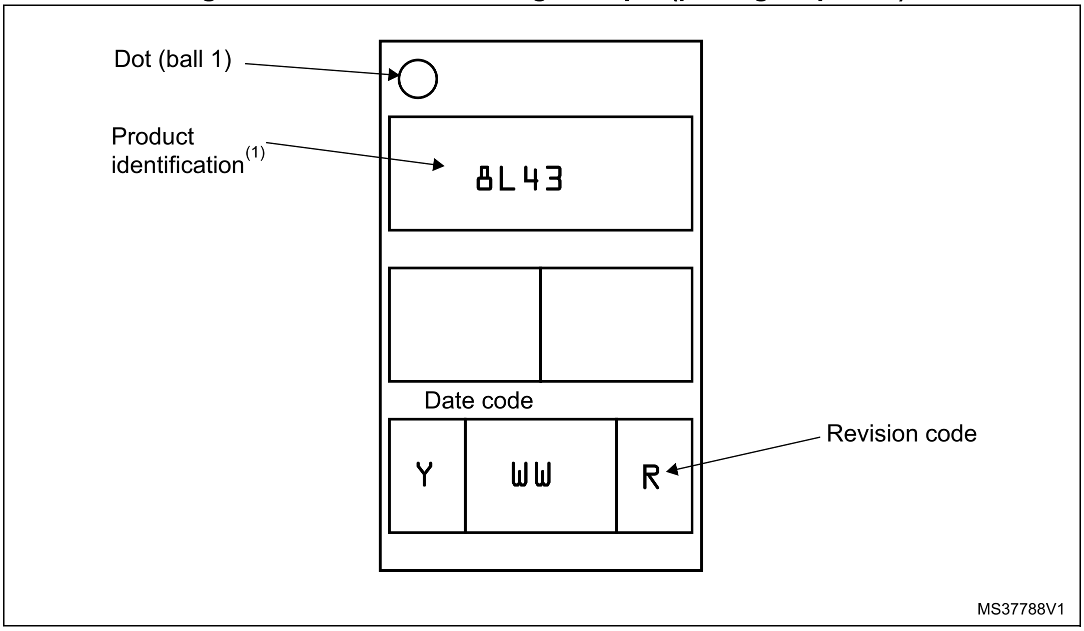
10.5 UFQFPN32 package information

Figure 52. UFQFPN32 - 32-pin, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.

Figure 59. WLCSP28 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 69. Document revision history (continued)

Date	Revision	Changes
23-Jul-2010	5	Modified *Introduction* and *Description.* Modified *Table: Legend/abbreviation for table 5* and *Table: Medium density STM8L15x pin description* (for PA0, PA1, PB0 and PB4 and for reset states in the floating input column) Modified *Figure: Low density STM8L151xx device block diagram, Figure: Low density STM8L15x clock tree diagram*, *Figure: Low power modes* and *Figure : Low power real-time clock.* Modified CLK_PCKENR2 and CLK_HSICALR reset values in *Table: General hardware register map.* Modified notes below *Figure: Memory map.* Modified PA_CR1 reset value. Modified reset values for Px_IDR registers. Modified *Table: Voltage characteristics* and *Table: Current characteristics.* Modified V_{IH} in *Table: I/O static characteristics.* Modified *Table: Total current consumption in Wait mode.* Modified *Figure Typical application with I2C bus and timing diagram 1).* Modified I_L value in *Figure: Typical connection diagram using the ADC1.* Modified R_H and R_L in *Table: LCD characteristics.* Added graphs in *Section: Electrical parameters.* Modified note 3 below *Table: Reference voltage characteristics.* Modified note 1 below *Table: TS characteristics.* Changed $V_{ESD(CDM)}$ value in *Table: ESD absolute maximum ratings.* Updated notes for UFQFPN32 and UFQFPN48 packages.
11-Mar-2011	6	Modified note on true open drain I/Os and I/O level columns in *Table: Medium density STM8L15x pin description.* Remapping option removed for USART1_TX, USART1_RX, and USART1_CK on PC2, PC3 and PC4 in *Table: Medium density STM8L15x pin description.* Modified IDWDG_KR reset value in *Table: General hardware register map.* Replaced VREF_OUT with VREFINT and TIMx_TRIG with TIMx_ETR. Added *Table: Factory conversion registers.* Modified reset values for TIM1_DCR1, IWDG_KR, RTC_DR1, RTC_DR2, RTC_SPRERH, RTC_SPRERL, RTC_APRER, RTC_WUTRH, and RTC_WUTRL in *Table: General hardware register map.* Added notes to certain values in *Section: Embedded reference voltage* and *Section: Temperature sensor.*