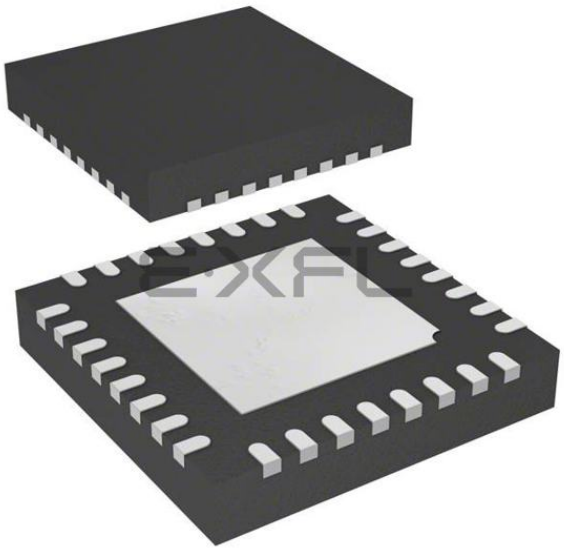


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l152k6u6tr

List of figures

3.6 LCD (Liquid crystal display)

The liquid crystal display drives up to 4 common terminals and up to 28 segment terminals to drive up to 112 pixels.

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4 duty supported.
- Static 1/2, 1/3 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 4 pixels which can programmed to blink.
- The LCD controller can operate in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The medium-density STM8L151x4/6 and STM8L152x4/6 devices have the following main features:

- Up to 2 Kbyte of RAM
- The non-volatile memory is divided into three arrays:
  - Up to 32 Kbyte of medium-density embedded Flash program memory
  - 1 Kbyte of data EEPROM
  - Option bytes.

The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC, I2C1, SPI1, USART1, the four Timers.

3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 25 channels (including 1 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 µs with f_{SYSCLK}= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.10 Digital-to-analog converter (DAC)

- 12-bit DAC with output buffer
- Synchronized update capability using TIM4
- DMA capability
- External triggers for conversion
- Input reference voltage V_{REF+} for better resolution

Note: DAC can be served by DMA1.

3.11 Ultra-low-power comparators

The medium-density STM8L151x4/6 and STM8L152x4/6 embed two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage or internal reference voltage sub multiple (1/4, 1/2, 3/4)

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC and the internal reference voltage V_{REFINT}. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (*Section 3.13: Touch sensing*).

3.13 Touch sensing

Medium-density STM8L151x4/6 and STM8L152x4/6 devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (example, glass, plastic). The capacitive variation introduced by a finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. In medium-density STM8L151x4/6

and STM8L152x4/6 devices, the acquisition sequence is managed by software and it involves analog I/O groups and the routing interface.

Reliable touch sensing solutions can be quickly and easily implemented using the free STM8 Touch Sensing Library.

3.14 Timers

Medium-density STM8L151x4/6 and STM8L152x4/6devices contain one advanced control timer (TIM1), two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 3 compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	up/down	Any integer from 1 to 65536	Yes	3 + 1	3
TIM2			Any power of 2 from 1 to 128		2	None
TIM3						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

3.14.1 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 3 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- 1 additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

3.19 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

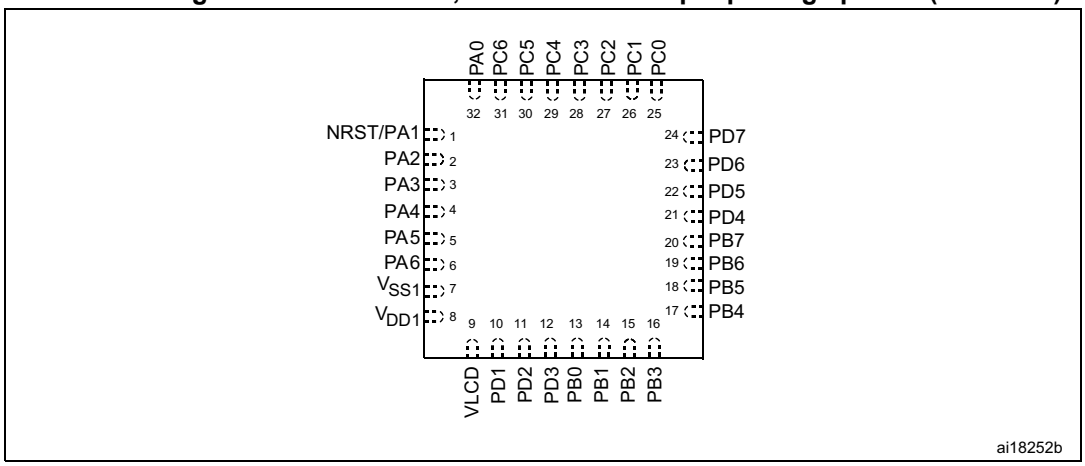
The single-wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1 interface. The reference document for the bootloader is *UM0560: STM8 bootloader user manual*.

Figure 8. STM8L152K4, STM8L152K6 32-pin package pinout (with LCD)



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.

Table 5. Medium-density STM8L151x4/6, STM8L152x4/6 pin description (continued)

Pin number				Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48/UFQFPN48	LQFP32/UFQFPN32	UFQFPN28	WLCSP28				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	8	7	G4	$V_{DD1}/V_{DDA}/V_{REF+}$	S	-	-	-	-	-	-	-	Digital power supply / Analog supply voltage / ADC1 positive voltage reference	
9	7	6	F4	$V_{SS1}/V_{SSA}/V_{REF-}$	S	-	-	-	-	-	-	-	I/O ground / Analog ground voltage / ADC1 negative voltage reference	
39	-	-	-	V_{DD2}	S	-	-	-	-	-	-	-	IOs supply voltage	
40	-	-	-	V_{SS2}	S	-	-	-	-	-	-	-	IOs ground voltage	
1	32	28	A4	PA0(9)/*[USART1_CK]*(4)/ SWIM/BEEP/IR_TIM (10)	I/O		X	**X**(9)	X	HS (10)	X	X	**Port A0**	*[USART1 synchronous clock]*(4) / SWIM input and output / Beep output / Infrared Timer output

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15x and STM8L16x reference manual (RM0031).
2. Available on STM8L152xx devices only.
3. In the 3.6 V tolerant I/Os, protection diode to V_{DD} is not implemented.
4. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
5. In the 5 V tolerant I/Os, protection diode to V_{DD} is not implemented.
6. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
7. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
8. Available on STM8L151xx devices only.
9. The PA0 pin is in input pull-up during the reset phase and after reset release.
10. High Sink LED driver capability available on PA0.

Note: The slope control of all GPIO pins, except true open drain pins, can be programmed. By default, the slope control is limited to 2 MHz.

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_DIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00
0x00 50C2		CLK_ICKR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x80
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0bxxxx0000
0x00 50CA		CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0xxx
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11100x

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50D0 to 0x00 50D2	Reserved area (3 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 bytes)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to 0x00 513F	Reserved area (76 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5140	RTC	RTC_TR1	Time register 1	0x00
0x00 5141		RTC_TR2	Time register 2	0x00
0x00 5142		RTC_TR3	Time register 3	0x00
0x00 5143		Reserved area (1 byte)		
0x00 5144		RTC_DR1	Date register 1	0x01
0x00 5145		RTC_DR2	Date register 2	0x21
0x00 5146		RTC_DR3	Date register 3	0x00
0x00 5147		Reserved area (1 byte)		
0x00 5148		RTC_CR1	Control register 1	0x00
0x00 5149		RTC_CR2	Control register 2	0x00
0x00 514A		RTC_CR3	Control register 3	0x00
0x00 514B		Reserved area (1 byte)		
0x00 514C		RTC_ISR1	Initialization and status register 1	0x00
0x00 514D		RTC_ISR2	Initialization and Status register 2	0x00
0x00 514E 0x00 514F		Reserved area (2 bytes)		
0x00 5150		RTC_SPRERH(1)	Synchronous prescaler register high	0x00(1)
0x00 5151		RTC_SPRERL(1)	Synchronous prescaler register low	0xFF(1)
0x00 5152		RTC_APRER(1)	Asynchronous prescaler register	0x7F(1)
0x00 5153		Reserved area (1 byte)		
0x00 5154		RTC_WUTRH(1)	Wakeup timer register high	0xFF(1)
0x00 5155		RTC_WUTRL(1)	Wakeup timer register low	0xFF(1)
0x00 5156 to 0x00 5158		Reserved area (3 bytes)		
0x00 5159		RTC_WPR	Write protection register	0x00
0x00 515A 0x00 515B		Reserved area (2 bytes)		
0x00 515C		RTC_ALRMAR1	Alarm A register 1	0x00
0x00 515D		RTC_ALRMAR2	Alarm A register 2	0x00
0x00 515E		RTC_ALRMAR3	Alarm A register 3	0x00
0x00 515F		RTC_ALRMAR4	Alarm A register 4	0x00
0x00 5160 to 0x00 51FF	Reserved area (160 bytes)			

Table 24. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions (1)			Typ	Max	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSE external clock (32.768 kHz) (6)	LCD OFF(7)	T_A = -40 °C to 25 °C	0.5	1.2	µA
				T_A = 55 °C	0.62	1.4	
				T_A = 85 °C	0.88	2.1	
				T_A = 105 °C	2.1	4.85	
				T_A = 125 °C	4.8	11	
			LCD ON (static duty/ external V_{LCD}) (3)	T_A = -40 °C to 25 °C	0.85	1.9	
				T_A = 55 °C	0.95	2.2	
				T_A = 85 °C	1.3	3.2	
				T_A = 105 °C	2.3	5.3	
				T_A = 125 °C	5.0	12	
			LCD ON (1/4 duty/ external V_{LCD}) (4)	T_A = -40 °C to 25 °C	1.5	2.5	
				T_A = 55 °C	1.6	3.8	
				T_A = 85 °C	1.8	4.2	
				T_A = 105 °C	2.9	7.0	
				T_A = 125 °C	5.7	14	
			LCD ON (1/4 duty/ internal V_{LCD}) (5)	T_A = -40 °C to 25 °C	3.4	7.6	
				T_A = 55 °C	3.7	8.3	
				T_A = 85 °C	3.9	9.2	
				T_A = 105 °C	5.0	14.5	
				T_A = 125 °C	6.3	15.2	
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode (using HSI)	-		-	2.4	-	mA
$t_{WU\_HSI(AH)}$ (8)(9)	Wakeup time from Active-halt mode to Run mode (using HSI)	-		-	4.7	7	µs
$t_{WU\_LSI(AH)}$ (8) (9)	Wakeup time from Active-halt mode to Run mode (using LSI)	-		-	150	-	µs

1. No floating I/O, unless otherwise specified.
2. RTC enabled. Clock source = LSI
3. RTC enabled, LCD enabled with external V_{LCD} = 3 V, static duty, division ratio = 256, all pixels active, no LCD connected.
4. RTC enabled, LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. LCD enabled with internal LCD booster V_{LCD} = 3 V, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
6. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*.
7. RTC enabled. Clock source = LSE.
8. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.
9. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

Figure 20. Typical LSI frequency vs. V_{DD}

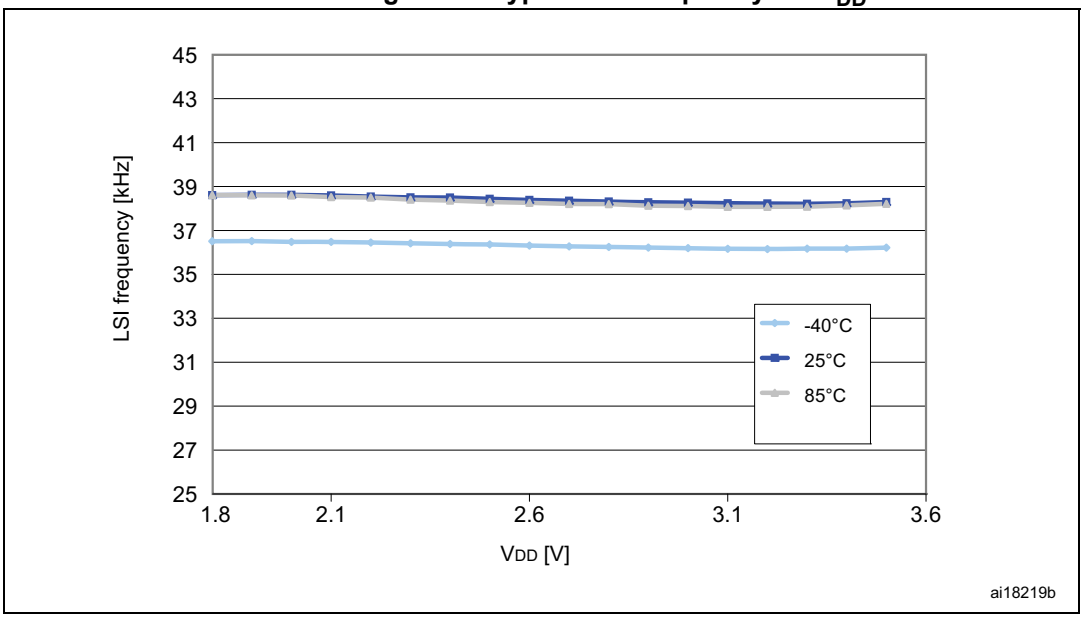


Figure 34. SPI1 timing diagram - slave mode and CPHA=0

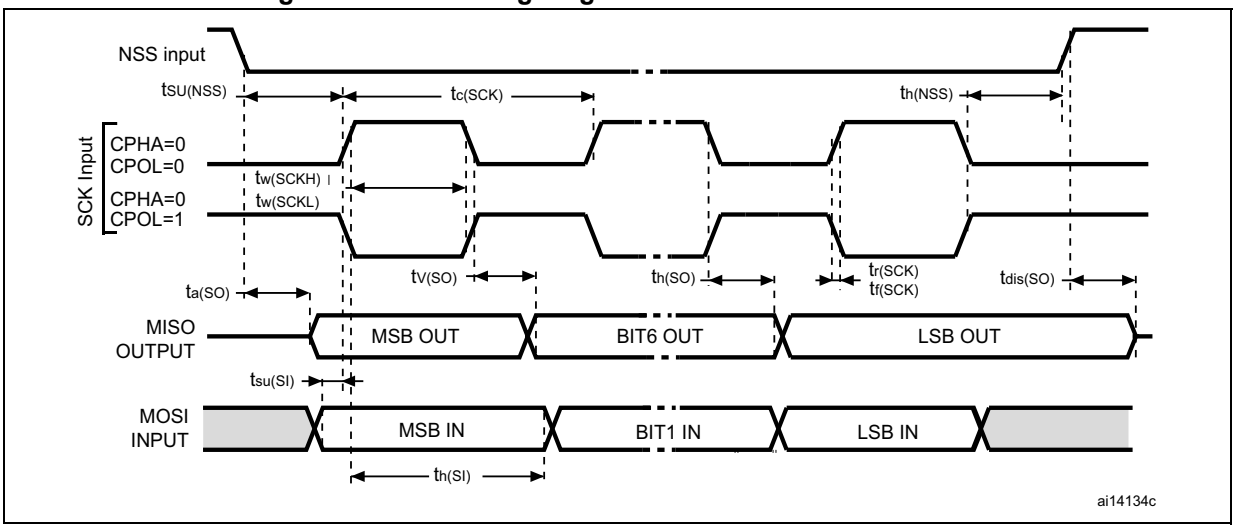
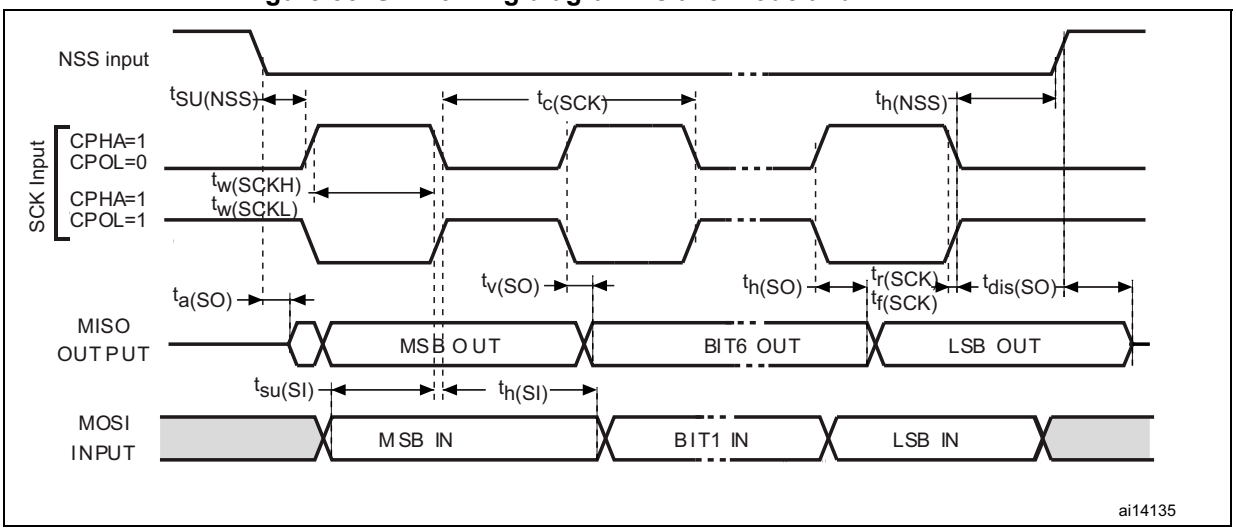


Figure 35. SPI1 timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

9.3.14 12-bit ADC1 characteristics

In the following table, data is guaranteed by design, not tested in production.

Table 53. ADC1 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	2.4 V ≤V_{DDA}≤ 3.6 V	2.4	-	V_{DDA}	V
		1.8 V ≤V_{DDA}≤ 2.4 V	V_{DDA}			V
V_{REF-}	Lower reference voltage	-	V_{SSA}			V
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF+}	Current on the V_{REF+} input pin	-	-	400	700 (peak)(1)	µA
		-	-		450 (average)(1)	µA
V_{AIN}	Conversion voltage range	-	0(2)	-	V_{REF+}	V
T_A	Temperature range	-	-40	-	125	°C
R_{AIN}	External resistance on V_{AIN}	on PF0 fast channel	-	-	50(3)	kΩ
		on all other channels	-	-		
C_{ADC}	Internal sample and hold capacitor	on PF0 fast channel	-	16	-	pF
		on all other channels	-		-	
f_{ADC}	ADC sampling clock frequency	2.4 V≤V_{DDA}≤3.6 V without zooming	0.320	-	16	MHz
		1.8 V≤V_{DDA}≤2.4 V with zooming	0.320	-	8	MHz
f_{CONV}	12-bit conversion rate	V_{AIN} on PF0 fast channel	-	-	1(4)(5)	MHz
		V_{AIN} on all other channels	-	-	760(4)(5)	kHz
f_{TRIG}	External trigger frequency	-	-	-	t_{conv}	$1/f_{ADC}$
t_{LAT}	External trigger latency	-	-	-	3.5	$1/f_{SYSCLK}$

Figure 41. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

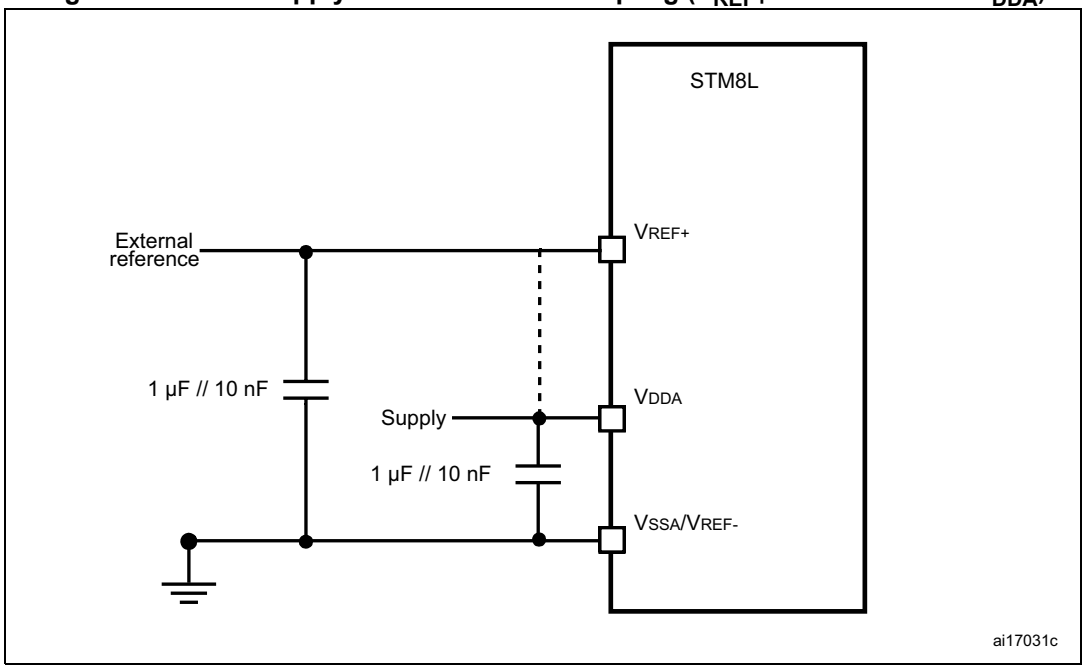
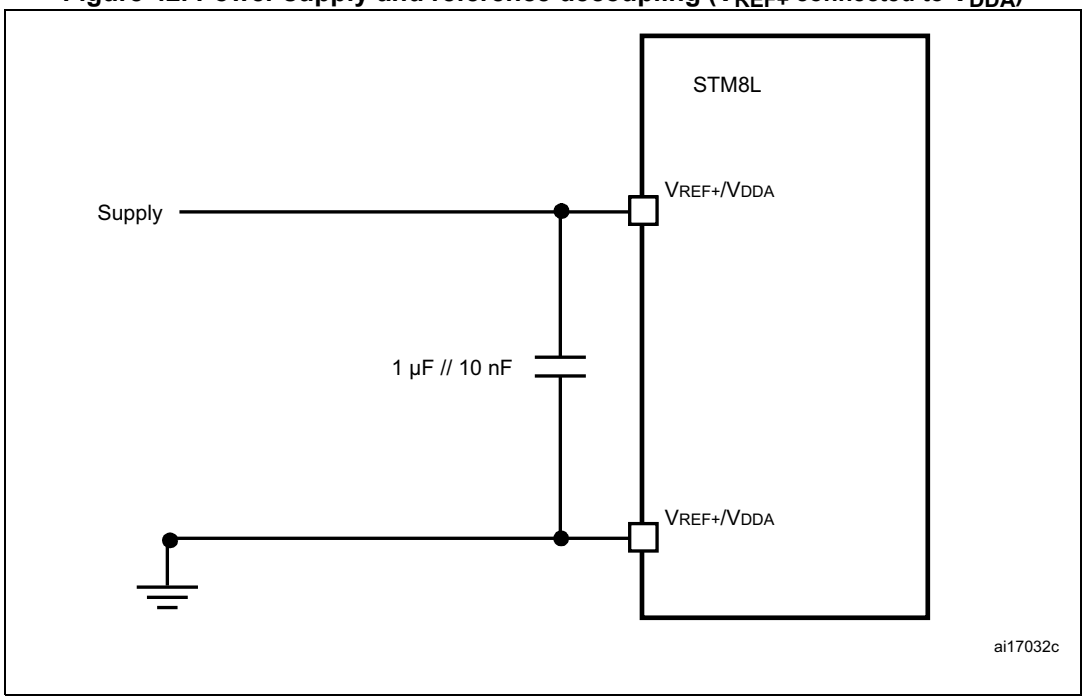


Figure 42. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



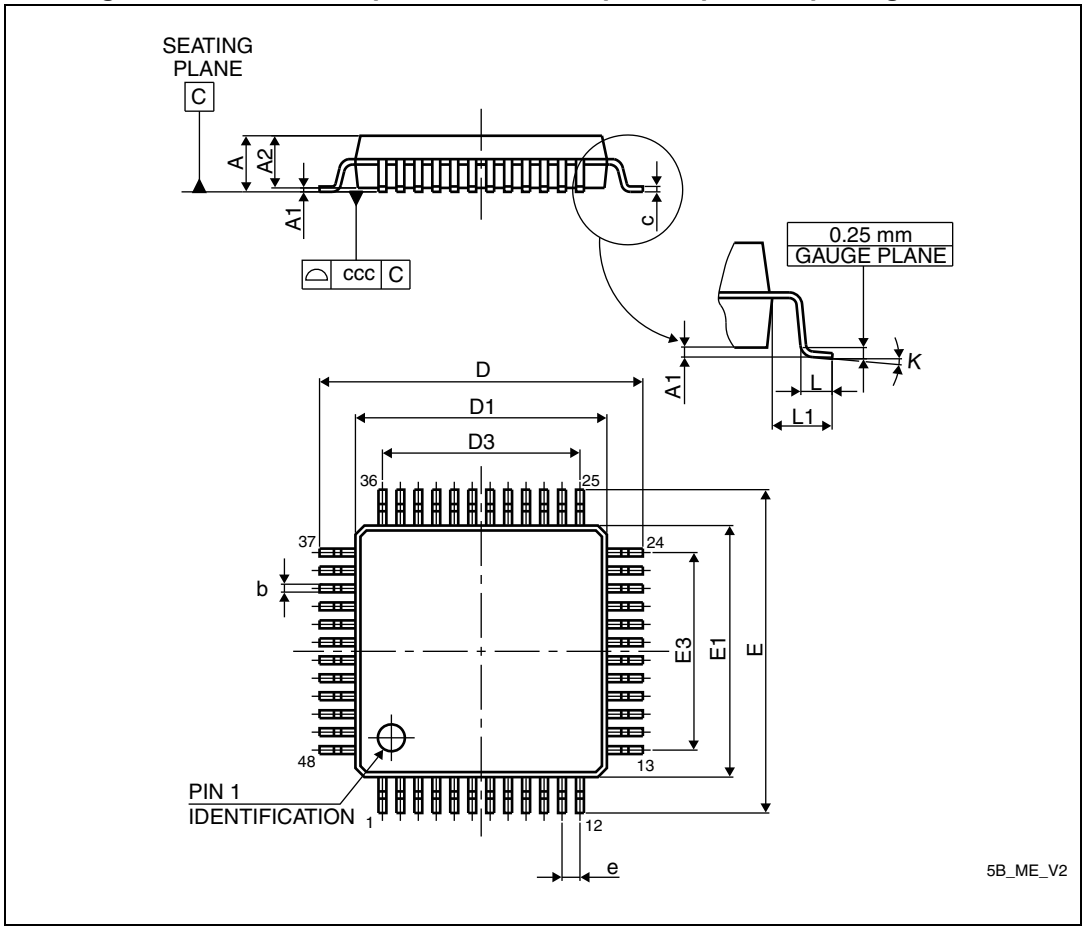
10 Package information

10.1 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

10.2 LQFP48 package information

Figure 43. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



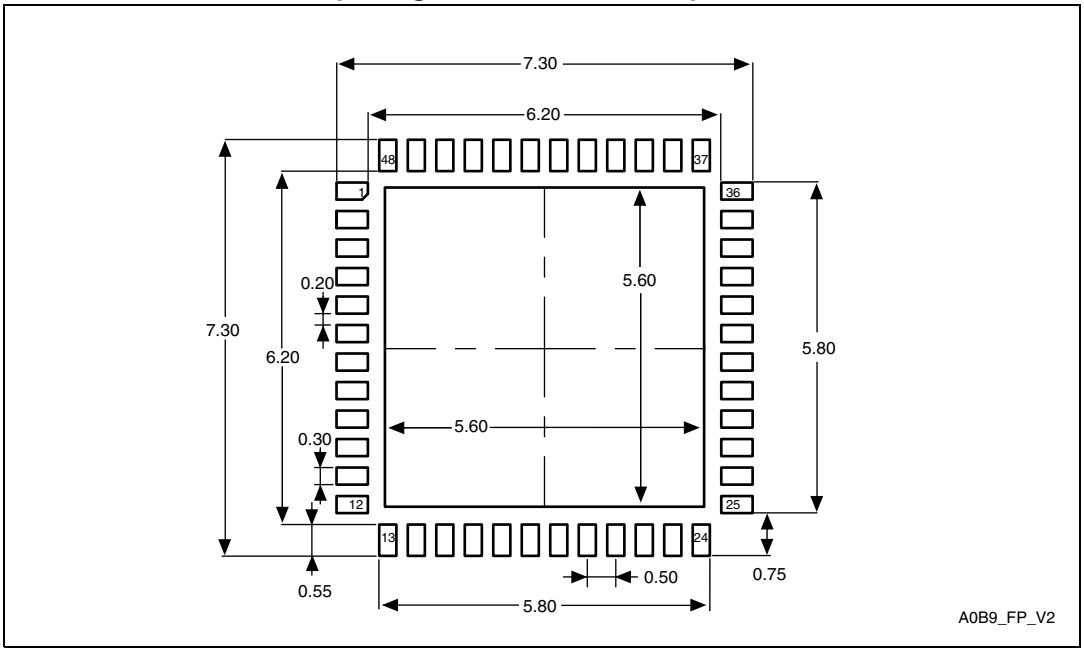
1. Drawing is not to scale.

Table 63. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

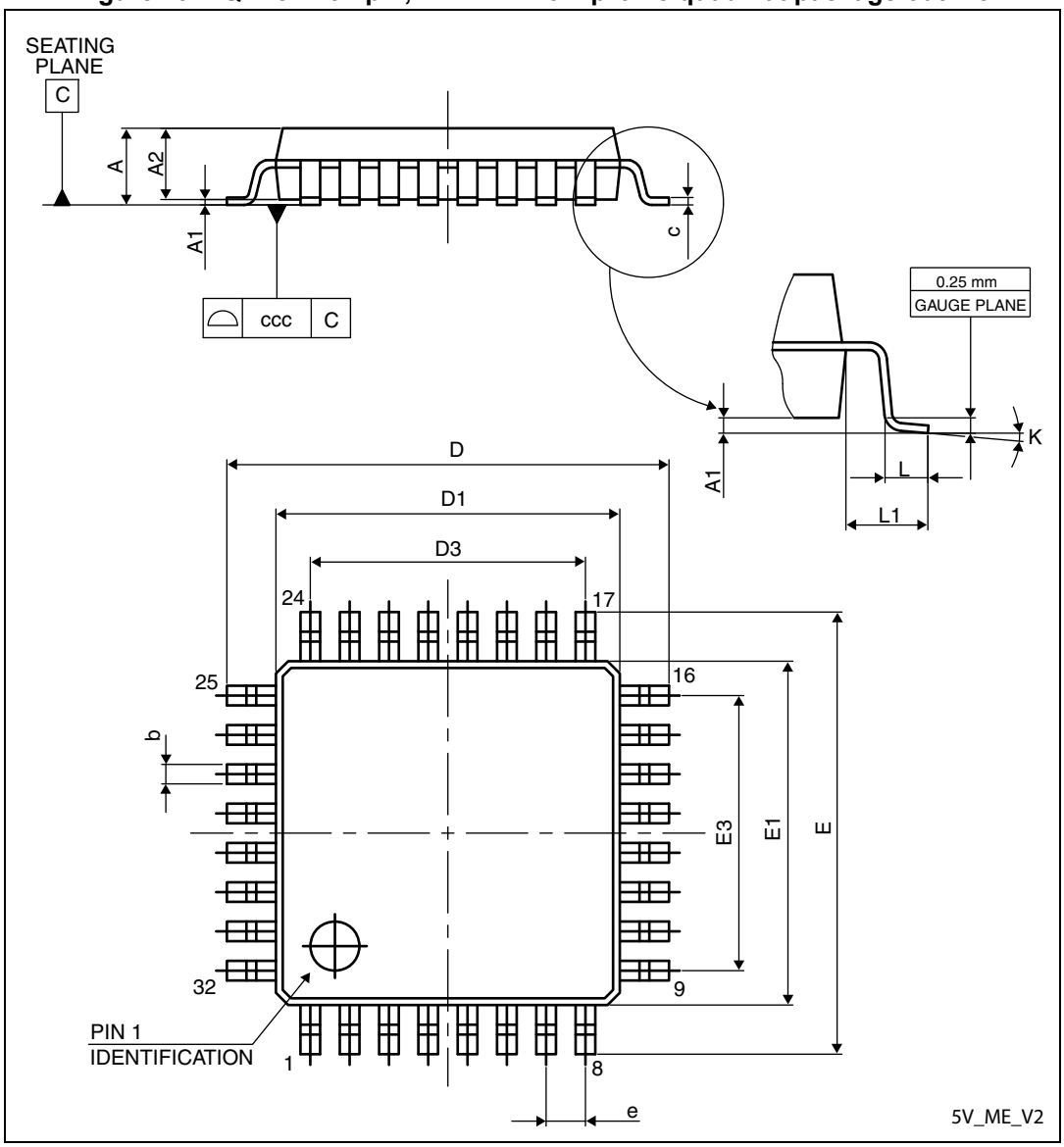
Figure 47. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

10.4 LQFP32 package information

Figure 49. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

10.8 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 18: General operating conditions on page 66*.

The maximum chip-junction temperature, T_{Jmax}, in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 68. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 48- 7 x 7 mm	65	°C/W
Θ_{JA}	Thermal resistance junction-ambient UFQFPN 48- 7 x 7mm	32	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	°C/W
Θ_{JA}	Thermal resistance junction-ambient UFQFPN 32 - 5 x 5 mm	38	°C/W
Θ_{JA}	Thermal resistance junction-ambient UFQFPN28 - 4 x 4 mm	118	°C/W
Θ_{JA}	Thermal resistance junction-ambient WLCSP28	70	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.