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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (9kB)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56301ag100

Signals/Connections 1

The DSP56301 input and output signals are organized into functional groups, as shown in **Table 1-1** and illustrated in **Figure 1-1**. The DSP56301 operates from a 3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 1-1. DSP56301 Functional Signal Groupings

Functional Group		Number of Signals by Package Type		Detailed Description
		TQFP	MAP-BGA	
Power (V_{CC})[1]		25	45	**Table 1-2**
Ground (GND)[1]		26	38	**Table 1-3**
Clock		2	2	**Table 1-4**
PLL		3	3	**Table 1-5**
Address Bus	Port A[2]	24	24	**Table 1-6**
Data Bus		24	24	**Table 1-7**
Bus Control		15	15	**Table 1-8**
Interrupt and Mode Control		5	5	**Table 1-9**
Host Interface (HI32)	Port B[3]	52	52	**Table 1-11**
Enhanced Synchronous Serial Interface (ESSI)	Ports C and D[4]	12	12	**Table 1-12** and **Table 1-13**
Serial Communication Interface (SCI)	Port E[5]	3	3	**Table 1-14**
Timer		3	3	**Table 1-15**
JTAG/OnCE Port		6	6	**Table 1-16**

Notes:
1. The number of available power and ground signals is package-dependent. In the TQFP package specific pins are dedicated internally to device subsystems. In the MAP-BGA package, power and ground connections (except those providing PLL power) connect to internal power and ground planes, respectively.
2. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
3. Port B signals are the HI32 port signals multiplexed with the GPIO signals.
4. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
5. Port E signals are the SCI port signals multiplexed with the GPIO signals.
6. Each device also includes several no connect (NC) pins. The number of NC connections is package-dependent: the TQFP has 9 NCs and the MAP-BGA has 20 NCs. Do not connect any line, component, trace, or via to these pins. See **Chapter 3** for details.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{HTRDY}}$	Input/ Output	Tri-stated	**Host Target Ready** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Target Ready signal.
$\overline{\text{HDBEN}}$	Output		**Host Data Bus Enable** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Bus Enable signal.
PB20	Input or Output		**Port B 20** When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH. This input is 5 V tolerant.
$\overline{\text{HIRDY}}$	Input/ Output	Tri-stated	**Host Initiator Ready** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Initiator Ready signal.
$\overline{\text{HDBDR}}$	Output		**Host Data Bus Direction** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Bus Direction signal.
PB21	Input or Output		**Port B 21** When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH. This input is 5 V tolerant.
$\overline{\text{HDEVSEL}}$	Input/ Output	Tri-stated	**Host Device Select** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Device Select signal.
$\overline{\text{HSAK}}$	Output		**Host Select Acknowledge** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Select Acknowledge signal.
PB22	Input or Output		**Port B 22** When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH. This input is 5 V tolerant.
$\overline{\text{HLOCK}}$	Input	Tri-stated	**Host Lock** When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Lock signal.
$\overline{\text{HBS}}$	Input		**Host Bus Strobe** When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Bus Strobe Schmitt-trigger signal.
PB23	Input or Output		**Port B 23** When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH. This input is 5 V tolerant.

Table 1-13. Enhanced Synchronous Serial Interface 1 (ESSI1) (Continued)

Signal Name	Type	State During Reset	Signal Description
SRD1	Input/Output	Input	**Serial Receive Data** Receives serial data and transfers it to the ESSI receive shift register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4** The default configuration following reset is GPIO. For PD4, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SRD1 through PCR1. This input is 5 V tolerant.
STD1	Input/Output	Input	**Serial Transmit Data** Transmits data from the serial transmit shift register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5** The default configuration following reset is GPIO. For PD5, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal STD1 through PCR1. This input is 5 V tolerant.

1.10 Serial Communication Interface (SCI)

The Serial Communication interface (SCI) provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-14. Serial Communication Interface (SCI)

Signal Name	Type	State During Reset	Signal Description
RXD	Input	Input	**Serial Receive Data** Receives byte-oriented serial data and transfers it to the SCI receive shift register.
PE0	Input or Output		**Port E 0** The default configuration following reset is GPIO. When configured as PE0, signal direction is controlled through the SCI Port Directions Register (PRR). The signal can be configured as an SCI signal RXD through the SCI Port Control Register (PCR). This input is 5 V tolerant.
TXD	Output	Input	**Serial Transmit Data** Transmits data from SCI transmit data register.
PE1	Input or Output		**Port E 1** The default configuration following reset is GPIO. When configured as PE1, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal TXD through the SCI PCR. This input is 5 V tolerant.

Table 1-14. Serial Communication Interface (SCI) (Continued)

Signal Name	Type	State During Reset	Signal Description
SCLK PE2	Input/Output Input or Output	Input	**Serial Clock** Provides the input or output clock used by the transmitter and/or the receiver. **Port E 2** The default configuration following reset is GPIO. For PE2, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal SCLK through the SCI PCR. This input is 5 V tolerant.

1.11 Timers

The DSP56301 has three identical and independent timers. Each can use internal or external clocking, interrupt the DSP56301 after a specified number of events (clocks), or signal an external device after counting a specific number of internal events.

Table 1-15. Triple Timer Signals

Signal Name	Type	State During Reset	Signal Description
TIO0	Input or Output	Input	**Timer 0 Schmitt-Trigger Input/Output** As an external event counter or in Measurement mode, TIO0 is input. In Watchdog, Timer, or Pulse Modulation mode, TIO0 is output. The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 0 Control/Status Register (TCSR0). This input is 5 V tolerant.
TIO1	Input or Output	Input	**Timer 1 Schmitt-Trigger Input/Output** As an external event counter or in Measurement mode, TIO1 is input. In Watchdog, Timer, or Pulse Modulation mode, TIO1 is output. The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 1 Control/Status Register (TCSR1). This input is 5 V tolerant.
TIO2	Input or Output	Input	**Timer 2 Schmitt-Trigger Input/Output** As an external event counter or in Measurement mode, TIO2 is input. In Watchdog, Timer, or Pulse Modulation mode, TIO2 is output. The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 2 Control/Status Register (TCSR2). This input is 5 V tolerant.

Table 2-3. DC Electrical Characteristics[6] (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
Input high voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$ • MOD[1]/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESSI/SCI/Timer/HI32 pins • EXTAL[8]	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 $0.8 \times V_{CC}$	 — — —	 V_{CC} 5.25 V_{CC}	 V V V
Input low voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD[1]/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT • All JTAG/ESSI/SCI/Timer/HI32 pins • EXTAL[8]	 V_{IL} V_{ILP} V_{ILX}	 –0.3 –0.3 –0.3	 — — —	 0.8 0.8 $0.2 \times V_{CC}$	 V V V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage • TTL (I_{OH} = –0.4 mA)[5,7] • CMOS (I_{OH} = –10 µA)[5]	V_{OH}	 2.4 V_{CC} – 0.01	 — —	 — —	 V V
Output low voltage • TTL (I_{OL} = 1.6 mA, open-drain pins I_{OL} = 6.7 mA)[5,7] • CMOS (I_{OL} = 10 µA)[5]	V_{OL}	 — —	 — —	 0.4 0.01	 V V
Internal supply current[2]: • In Normal mode • In Wait mode[3] • In Stop mode[4]	 I_{CCI} I_{CCW} I_{CCS}	 — — —	**80 MHz** / **100 MHz** 102 / 127 6 / 7.5 100 / 100	 — — —	 mA mA µA
PLL supply current		—	1	2.5	mA
Input capacitance[5]	C_{IN}	—	—	10	pF

Notes:
1. Refers to MODA/$\overline{IRQA}$, MODB/$\overline{IRQB}$, MODC/$\overline{IRQC}$, and MODD/$\overline{IRQD}$ pins.
2. **Power Consumption Considerations** on page 4-3 provides a formula to compute the estimated current requirements in Normal mode. To obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC} = 3.0 V at T_J = 100°C.
3. To obtain these results, all inputs must be terminated (that is, not allowed to float).
4. To obtain these results, all inputs that are not disconnected at Stop mode must be terminated (that is, not allowed to float). PLL and XTAL signals are disabled during Stop state.
5. Periodically sampled and not 100 percent tested.
6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
7. This characteristic does not apply to XTAL and PCAP.
8. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than $0.9 \times V_{CC}$ and the maximum V_{ILX} should be no higher than $0.1 \times V_{CC}$.

Table 2-5. Clock Operation

No.	Characteristics	Symbol	80 MHz		100 MHz	
			Min	Max	Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	80.0 MHz	0	100.0 MHz
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_H	 5.84 ns 5.31 ns	 ∞ 157.0 µs	 4.67 ns 4.25 ns	 ∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_L	 5.84 ns 5.31 ns	 ∞ 157.0 µs	 4.67 ns 4.25 ns	 ∞ 157.0 µs
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	 12.50 ns 12.50 ns	 ∞ 273.1 µs	 10.00 ns 10.00 ns	 ∞ 273.1 µs
5	CLKOUT change from EXTAL fall with PLL disabled		4.3 ns	11.0 ns	4.3 ns	11.0 ns
6	a. CLKOUT rising edge from EXTAL rising edge with PLL enabled (MF = 1 or 2 or 4, PDF = 1, Ef > 15 MHz)[3,5] b. CLKOUT falling edge from EXTAL falling edge with PLL enabled (MF ≤ 4, PDF ≠ 1, Ef / PDF > 15 MHz)[3,5]		0.0 ns 0.0 ns	1.8 ns 1.8 ns	0.0 ns 0.0 ns	1.8 ns 1.8 ns
7	Instruction cycle time = $I_{CYC} = T_C$[4] (see **Table 2-4**) (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled	I_{CYC}	 25.0 ns 12.50 ns	 ∞ 8.53 µs	 20.0 ns 10.00 ns	 ∞ 8.53 µs

Notes:
1. Measured at 50 percent of the input transition
2. The maximum value for PLL enabled is given for minimum VCO frequency (see **Table 2-6**) and maximum MF.
3. Periodically sampled and not 100 percent tested
4. The maximum value for PLL enabled is given for minimum VCO frequency and maximum DF.
5. The skew is not guaranteed for any other MF value.
6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

2.5.3 Phase Lock Loop (PLL) Characteristics

Table 2-6. PLL Characteristics

Characteristics	80 MHz		100 MHz		Unit
	Min	Max	Min	Max	
Voltage Controlled Oscillator (VCO) frequency when PLL enabled (MF × E_f × 2/PDF)	30	160	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}) • @ MF ≤ 4 • @ MF > 4	 (MF × 580) – 100 MF × 830	 (MF × 780) – 140 MF × 1470	 (MF × 580) – 100 MF × 830	 (MF × 780) – 140 MF × 1470	 pF pF

Note: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}). The recommended value in pF for C_{PCAP} can be computed from one of the following equations:
(680 × MF) – 120, for MF ≤ 4, or
1100 × MF, for MF > 4.

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
28	DMA Request Rate						
	• Data read from HI32, ESSI, SCI	$6 \times T_C$	—	75.0	—	60.0	ns
	• Data write to HI32, ESSI, SCI	$7 \times T_C$	—	87.5	—	70.0	ns
	• Timer	$2 \times T_C$	—	25.0	—	20.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$3 \times T_C$	—	37.5	—	30.0	ns
29	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory (DMA source) access address out valid	$4.25 \times T_C + 2.0$	55.1	—	44.5	—	ns

Notes:

1. When using fast interrupts and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. This timing depends on several settings:
   • For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure that the oscillator is stable before programs are executed. Resetting the Stop delay (Operating Mode Register Bit 6 = 0) provides the proper delay. While Operating Mode Register Bit 6 = 1 can be set, it is not recommended, and these specifications do not guarantee timings for that case.
   • For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery is minimal (Operating Mode Register Bit 6 setting is ignored).
   • For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time is defined by the PCTL Bit 17 and Operating Mode Register Bit 6 settings.
   • For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery ends when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.
   • PLC value for PLL disable is 0.
   • The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (that is, for 66 MHz it is 4096/66 MHz = 62 µs). During the stabilization period, T_C, T_H, and T_L is not constant, and their width may vary, so timing may vary as well.
3. Periodically sampled and not 100 percent tested.
4. Value depends on clock source:
   • For an external clock generator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.
   • For an internal oscillator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.
   • When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
5. If PLL does not lose lock.
6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100°C, C_L = 50 pF.
7. WS = number of wait states (measured in clock cycles, number of T_C).
8. Use the expression to compute a maximum value.

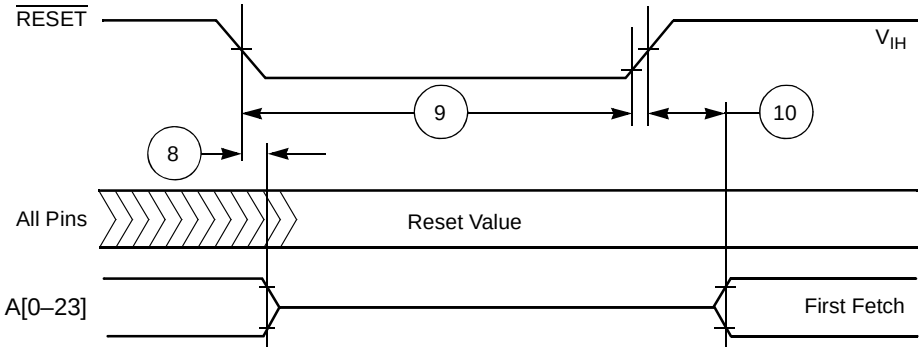


Figure 2-3. Reset Timing

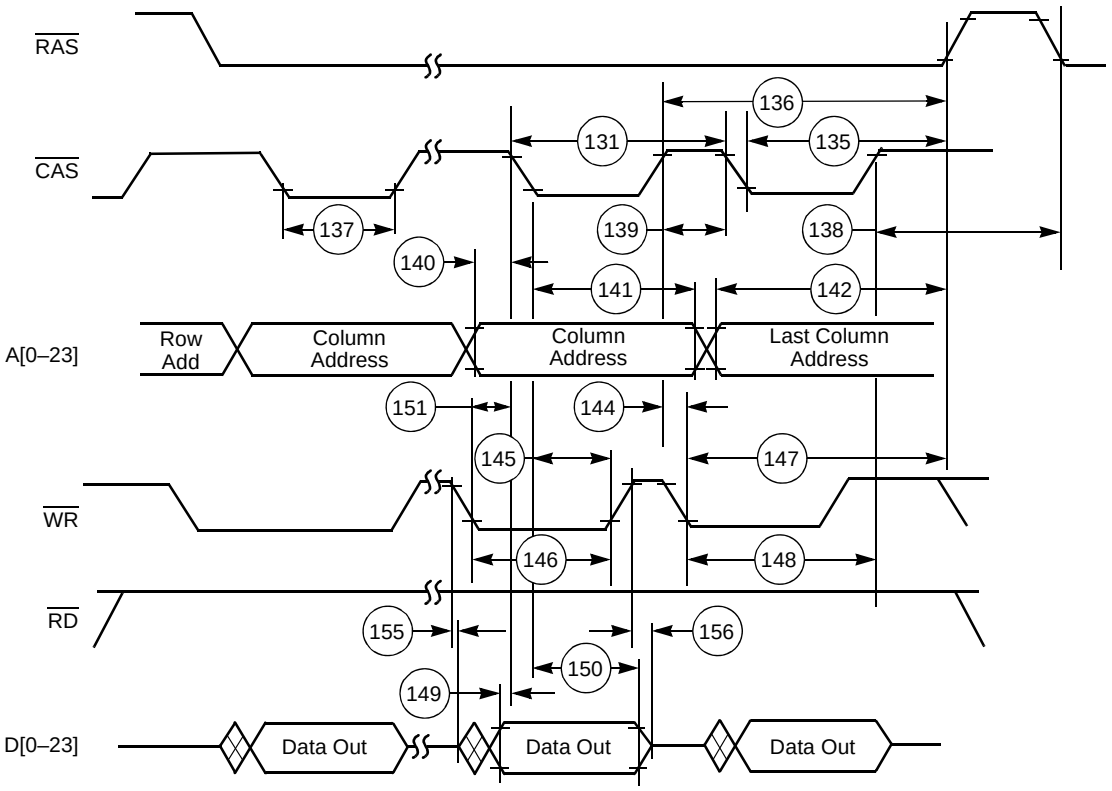


Figure 2-15. DRAM Page Mode Write Accesses

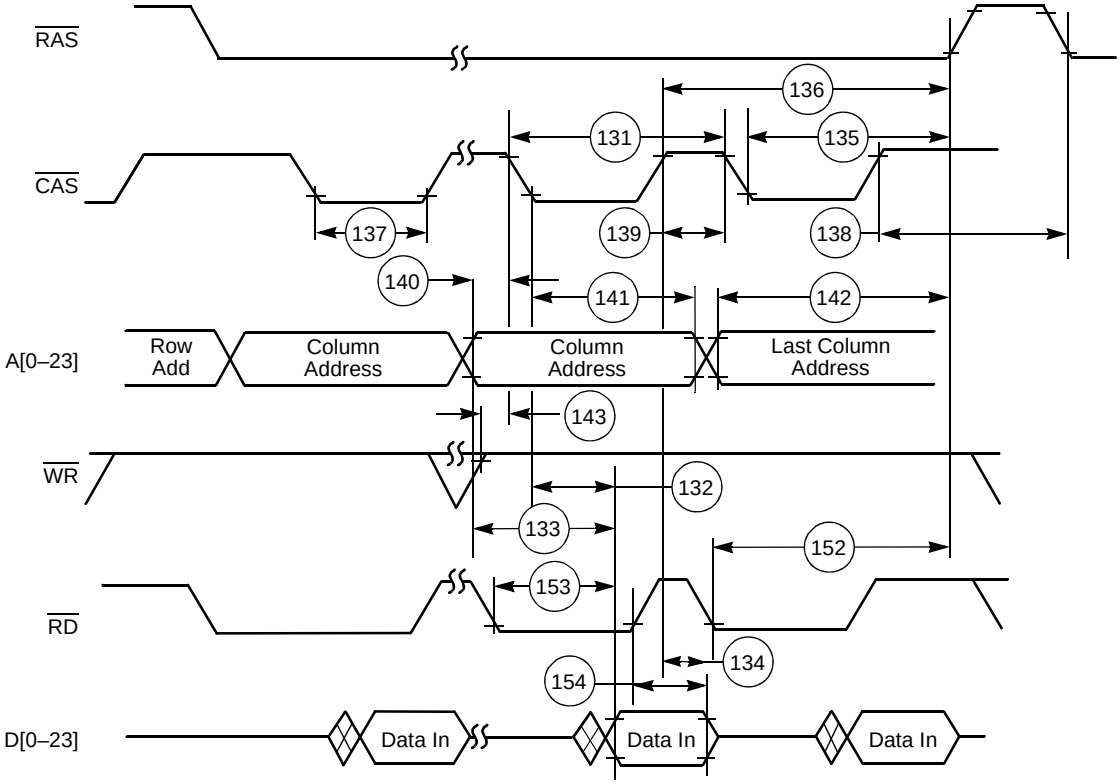


Figure 2-16. DRAM Page Mode Read Accesses

Table 2-13. DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$7.75 \times T_C - 4.0$	92.9	—	73.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$6.5 \times T_C - 4.3$	77.0	—	60.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$2.75 \times T_C - 4.0$	30.4	—	23.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$11.5 \times T_C - 4.0$	139.8	—	111.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	**80 MHz**: $10 \times T_C - 6.5$ **100 MHz**: $10 \times T_C - 7.0$	— —	118.5 —	— —	— 93.0	ns ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	9.1	—	6.0	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for an out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 2-14. DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$16 \times T_C$	200.0	—	160.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	**80 MHz**: $8.25 \times T_C - 6.5$ **100 MHz**: $8.25 \times T_C - 5.7$	— —	96.6 —	— —	— 76.8	ns ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**80 MHz**: $4.75 \times T_C - 6.5$ **100 MHz**: $4.75 \times T_C - 5.7$	— —	52.9 —	— —	— 41.8	ns ns
160	Column address valid to data valid (read)	t_{AA}	**80 MHz**: $5.5 \times T_C - 6.5$ **100 MHz**: $5.5 \times T_C - 5.7$	— —	62.3 —	— —	— 49.3	ns ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}	0.0	0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$8.25 \times T_C - 4.0$	99.1	—	78.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$4.75 \times T_C - 4.0$	55.4	—	43.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$3.5 \times T_C \pm 2$	41.8	45.8	33.0	37.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$2.75 \times T_C \pm 2.0$	32.4	36.4	25.5	29.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$7.75 \times T_C - 4.0$	92.9	—	73.5	—	ns

Table 2-14. DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 6.0$	74.1	—	56.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C - 4.0$	30.4	—	23.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	5.4	—	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$7 \times T_C - 4.0$	83.5	—	66.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$5 \times T_C - 3.8$	58.7	—	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	18.2	—	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RRH}	**80 MHz**: $0.25 \times T_C - 2.6$ **100 MHz**: $0.25 \times T_C - 2.0$	0.5 —	— —	— 0.5	— —	ns ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$6 \times T_C - 4.2$	70.8	—	55.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$9.5 \times T_C - 4.2$	114.6	—	90.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$15.5 \times T_C - 4.5$	189.3	—	150.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$15.75 \times T_C - 4.3$	192.6	—	153.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$14.25 \times T_C - 4.3$	173.8	—	138.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$8.75 \times T_C - 4.0$	105.4	—	83.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$9.5 \times T_C - 4.3$	114.5	—	90.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C - 4.0$	55.4	—	43.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$15.5 \times T_C - 4.0$	189.8	—	151.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	**80 MHz**: $14 \times T_C - 6.5$ **100 MHz**: $14 \times T_C - 5.7$	— —	168.5 —	— —	— 134.3	ns ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	9.1	—	6.0	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for an out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

2.5.5.3 Synchronous Timings (SRAM)

Table 2-15. External Bus Synchronous Timings (SRAM Access)[3]

No.	Characteristics	Expression[1,2]	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
196	CLKOUT high to $\overline{BS}$ assertion	$0.25 \times T_C$ +5.2/–0.5	2.6	8.3	2.0	7.7	ns
197	CLKOUT high to $\overline{BS}$ deassertion	$0.75 \times T_C$ +4.2/–1.0	8.4	13.6	6.5	11.7	ns
198	CLKOUT high to address, and AA valid[4]	$0.25 \times T_C + 2.5$	—	5.6	—	5.0	ns
199	CLKOUT high to address, and AA invalid[4]	$0.25 \times T_C - 0.7$	2.4	—	1.8	—	ns
200	$\overline{TA}$ valid to CLKOUT high (setup time)		5.8	—	4.0	—	ns
201	CLKOUT high to $\overline{TA}$ invalid (hold time)		0.0	—	0.0	—	ns
202	CLKOUT high to data out active	$0.25 \times T_C$	3.1	—	2.5	—	ns
203	CLKOUT high to data out valid	**80 MHz**: $0.25 \times T_C + 4.5$ **100 MHz**: $0.25 \times T_C + 4.0$	— —	7.6 —	— —	— 6.5	ns ns
204	CLKOUT high to data out invalid	$0.25 \times T_C$	3.1	—	2.5	—	ns
205	CLKOUT high to data out high impedance	**80 MHz**: $0.25 \times T_C + 0.5$ **100 MHz**: $0.25 \times T_C$	— —	3.6 —	— —	— 2.5	ns ns
206	Data in valid to CLKOUT high (setup)		5.0	—	4.0	—	ns
207	CLKOUT high to data in invalid (hold)		0.0	—	0.0	—	ns
208	CLKOUT high to $\overline{RD}$ assertion	maximum: $0.75 \times T_C + 2.5$	10.4	 11.9	6.7	 10.0	ns ns
209	CLKOUT high to $\overline{RD}$ deassertion		0.0	4.5	0.0	4.0	ns
210	CLKOUT high to $\overline{WR}$ assertion[2]	$0.5 \times T_C + 4.3$ [WS = 1 or WS ≥ 4] [2 ≤ WS ≤ 3]	7.6 1.3	10.6 4.8	4.5 0.0	9.3 4.3	ns ns
211	CLKOUT high to $\overline{WR}$ deassertion		0.0	4.3	0.0	3.8	ns

Notes:
1. WS is the number of wait states specified in the BCR.
2. If WS > 1, $\overline{WR}$ assertion refers to the next rising edge of CLKOUT.
3. External bus synchronous timings should be used only for reference to the clock and *not* for relative timings.
4. T198 and T199 are valid for Address Trace mode if the ATE bit in the Operating Mode Register is set. Use the status of $\overline{BR}$ (See T212) to determine whether the access referenced by A[0–23] is internal or external in this mode.

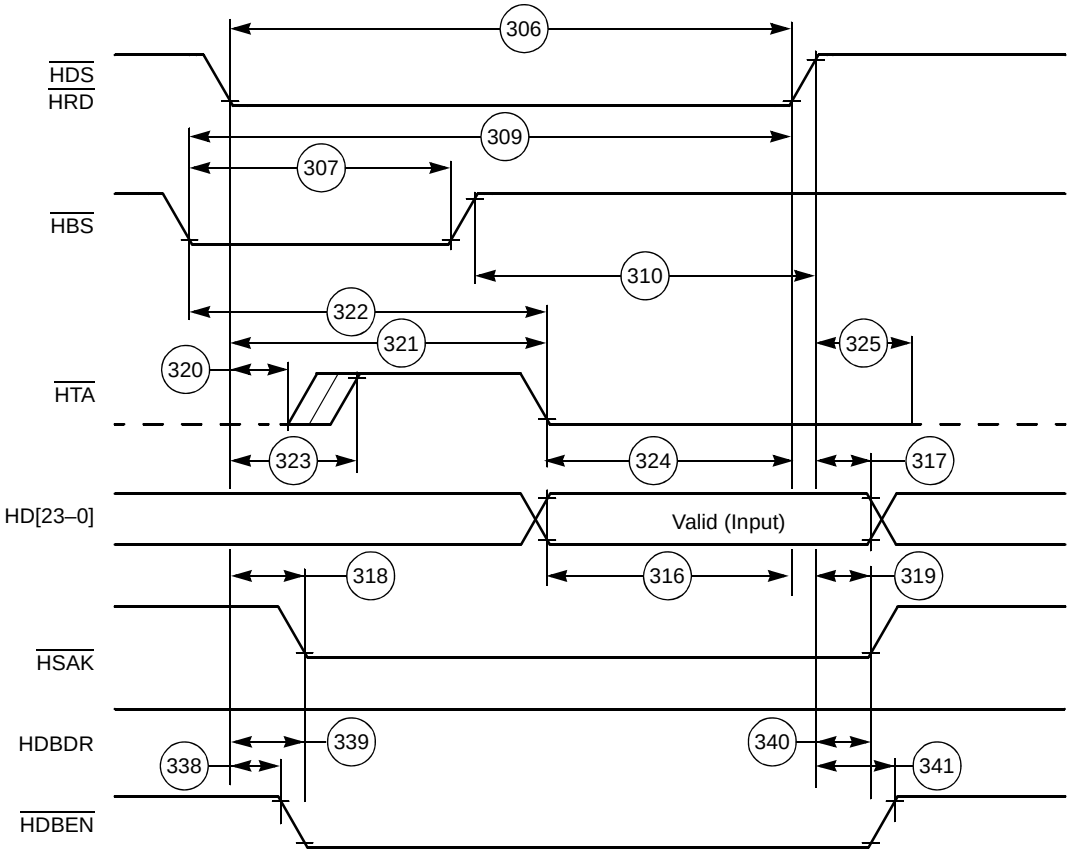


Figure 2-33. Write Timing

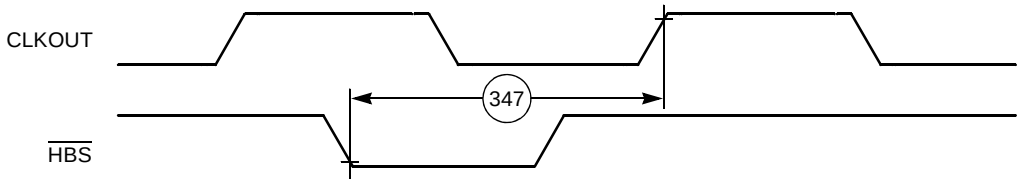


Figure 2-34. $\overline{\text{HBS}}$ Synchronous Timing

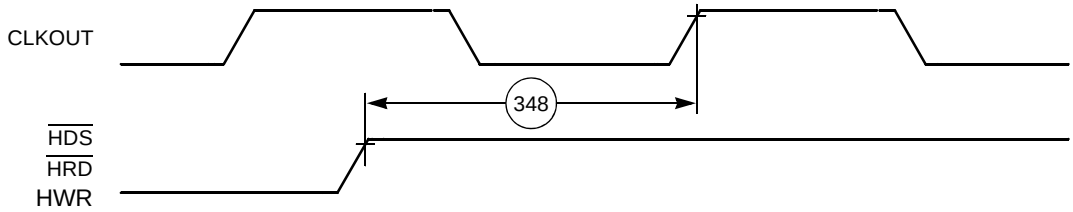
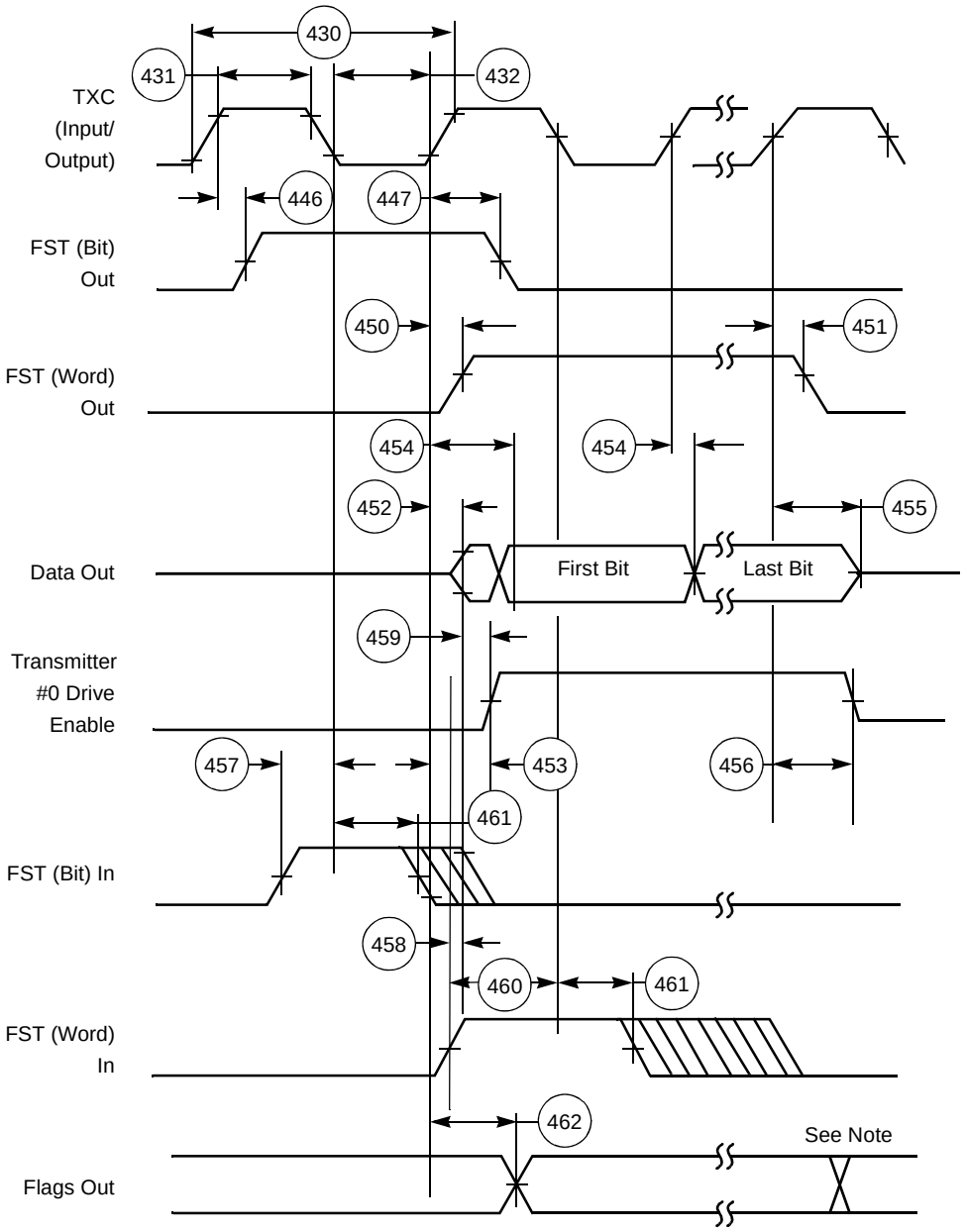


Figure 2-35. Data Strobe Synchronous Timing



Note: In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

Figure 2-40. ESSI Transmitter Timing

Packaging 3

This section provides information on the available packages for the DSP56301, including diagrams of the package pinouts and tables showing how the signals discussed in **Section 1** are allocated for each package. The DSP56301 is available in two package types:

- 208-pin Thin Quad Flat Pack (TQFP)
- 252-pin Molded Array Process-Ball Grid Array (MAP-BGA)

Note: Both packages are available in lead-bearing and lead-free versions. Switching a design from a lead-bearing package device to a lead-free package device may require a change in the board manufacturing process. The lead-free package requires a higher solder flow temperature than the lead-bearing device. Refer to *Lead-Free BGA Solder Joint Assembly Evaluation* (EB635) for manufacturing considerations when incorporating lead-free package devices into a design.

Table 3-2. DSP56301 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND_N	19	HAD14	152	HAEN	149
GND_P	13	HAD15	151	$\overline{HBE0}$	163
GND_Q	27	HAD16	127	$\overline{HBE1}$	150
GND_Q	78	HAD17	126	$\overline{HBE2}$	128
GND_Q	132	HAD18	125	$\overline{HBE3}$	117
GND_Q	183	HAD19	124	$\overline{HBS}$	140
GND_Q	183	HAD2	171	HC0	163
GND_S	180	HAD20	121	HC1	150
GND_S	194	HAD21	120	HC2	128
HA0	163	HAD22	119	HC3	117
HA1	150	HAD23	118	HCLK	148
HA10	164	HAD24	116	HD0	162
HA2	128	HAD25	115	HD1	161
HA3	173	HAD26	114	HD10	125
HA4	172	HAD27	113	HD11	124
HA5	171	HAD28	110	HD12	121
HA6	170	HAD29	109	HD13	120
HA7	167	HAD3	170	HD14	119
HA8	166	HAD30	108	HD15	118
HA9	165	HAD31	107	HD16	116
HAD0	173	HAD4	167	HD17	115
HAD1	172	HAD5	166	HD18	114
HAD10	160	HAD6	165	HD19	113
HAD11	159	HAD7	164	HD2	160
HAD12	154	HAD8	162	HD20	110
HAD13	153	HAD9	161	HD21	109

3.3 MAP-BGA Package Description

Top and bottom views of the MAP-BGA package are shown in **Figure 3-4** and **Figure 3-5** with their pin-outs.

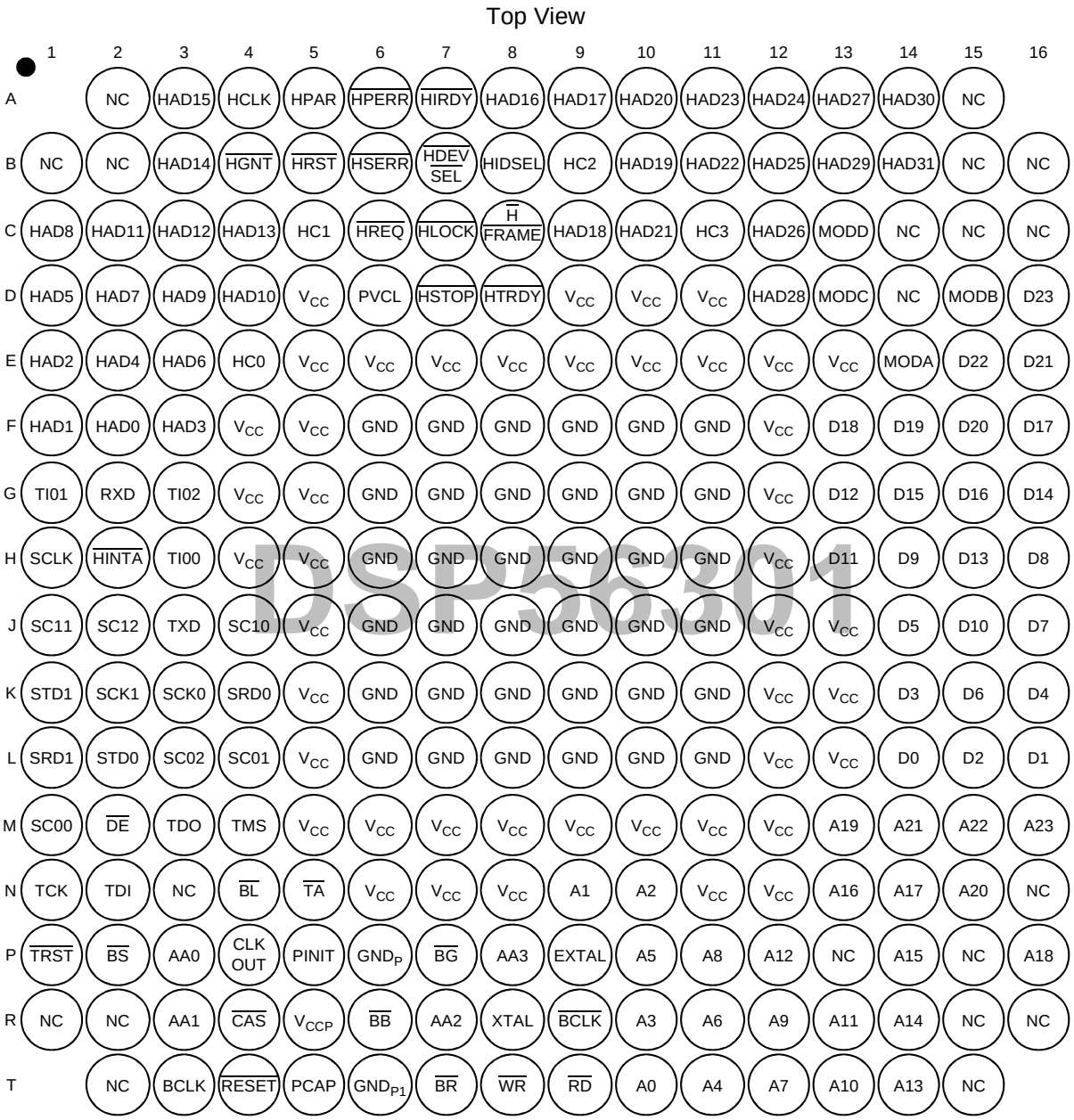


Figure 3-4. DSP56301 Molded Array Process-Ball Grid Array (MAP-BGA), Top View

Table 3-4. DSP56301 MAP-BGA Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	T10	AA2	R7	D22	E15
A1	N9	AA3	P8	D23	D16
A10	T13	$\overline{BB}$	R6	D3	K14
A11	R13	BCLK	T3	D4	K16
A12	P12	$\overline{BCLK}$	R9	D5	J14
A13	T14	$\overline{BG}$	P7	D6	K15
A14	R14	$\overline{BL}$	N4	D7	J16
A15	P14	$\overline{BR}$	T7	D8	H16
A16	N13	$\overline{BS}$	P2	D9	H14
A17	N14	$\overline{CAS}$	R4	$\overline{DE}$	M2
A18	P16	CLKOUT	P4	EXTAL	P9
A19	M13	D0	L14	GND	F10
A2	N10	D1	L16	GND	F11
A20	N15	D10	J15	GND	F6
A21	M14	D11	H13	GND	F7
A22	M15	D12	G13	GND	F8
A23	M16	D13	H15	GND	F9
A3	R10	D14	G16	GND	G10
A4	T11	D15	G14	GND	G11
A5	P10	D16	G15	GND	G6
A6	R11	D17	F16	GND	G7
A7	T12	D18	F13	GND	G8
A8	P11	D19	F14	GND	G9
A9	R12	D2	L15	GND	H10
AA0	P3	D20	F15	GND	H11
AA1	R3	D21	E16	GND	H6

```
M_TSMB1 EQU $FFFFA3; SSI1 Transmit Slot Mask Register B
M_RSMA1 EQU $FFFFA2; SSI1 Receive Slot Mask Register A
M_RSMB1 EQU $FFFFA1; SSI1 Receive Slot Mask Register B

;       SSI Control Register A Bit Flags

M_PM EQU $FF    ; Prescale Modulus Select Mask (PM0-PM7)
M_PSR EQU 11     ; Prescaler Range
M_DC EQU $1F000 ; Frame Rate Divider Control Mask (DC0-DC7)
M_ALC EQU 18   ; Alignment Control (ALC)
M_WL EQU $380000; Word Length Control Mask (WL0-WL7)
M_SSC1 EQU 22  ; Select SC1 as TR #0 drive enable (SSC1)

;       SSI Control Register B Bit Flags

M_OF EQU $3    ; Serial Output Flag Mask
M_OF0 EQU 0    ; Serial Output Flag 0
M_OF1 EQU 1    ; Serial Output Flag 1
M_SCD EQU $1C  ; Serial Control Direction Mask
M_SCD0 EQU 2   ; Serial Control 0 Direction
M_SCD1 EQU 3      ; Serial Control 1 Direction
M_SCD2 EQU 4      ; Serial Control 2 Direction
M_SCKD EQU 5      ; Clock Source Direction
M_SHFD EQU 6      ; Shift Direction
M_FSL EQU $180 ; Frame Sync Length Mask (FSL0-FSL1)
M_FSL0 EQU 7   ; Frame Sync Length 0
M_FSL1 EQU 8   ; Frame Sync Length 1
M_FSR EQU 9    ; Frame Sync Relative Timing
M_FSP EQU 10   ; Frame Sync Polarity
M_CKP EQU 11   ; Clock Polarity
M_SYN EQU 12   ; Sync/Async Control
M_MOD EQU 13   ; SSI Mode Select
M_SSTE EQU $1C000; SSI Transmit enable Mask
M_SSTE2 EQU 14 ; SSI Transmit #2 Enable
M_SSTE1 EQU 15 ; SSI Transmit #1 Enable
M_SSTE0 EQU 16 ; SSI Transmit #0 Enable
M_SSRE EQU 17  ; SSI Receive Enable
M_SSTIE EQU 18 ; SSI Transmit Interrupt Enable
M_SSRIE EQU 19 ; SSI Receive Interrupt Enable
M_STLIE EQU 20 ; SSI Transmit Last Slot Interrupt Enable
M_SRLIE EQU 21 ; SSI Receive Last Slot Interrupt Enable
M_STEIE EQU 22 ; SSI Transmit Error Interrupt Enable
M_SREIE EQU 23 ; SSI Receive Error Interrupt Enable


;       SSI Status Register Bit Flags

M_IF EQU $3     ; Serial Input Flag Mask
M_IF0 EQU 0      ; Serial Input Flag 0
M_IF1 EQU 1      ; Serial Input Flag 1
M_TFS EQU 2      ; Transmit Frame Sync Flag
M_RFS EQU 3      ; Receive Frame Sync Flag
M_TUE EQU 4      ; Transmitter Underrun Error FLag
M_ROE EQU 5      ; Receiver Overrun Error Flag
M_TDE EQU 6      ; Transmit Data Register Empty
M_RDF EQU 7      ; Receive Data Register Full

;       SSI Transmit Slot Mask Register A

M_SSTSA EQU $FFFF  ; SSI Transmit Slot Bits Mask A (TS0-TS15)
```

```
M_TC EQU $F0    ; Timer Control Mask (TC0-TC3)
M_INV EQU 8      ; Inverter Bit
M_TRM EQU 9      ; Timer Restart Mode
M_DIR EQU 11     ; Direction Bit
M_DI EQU 12     ; Data Input
M_DO EQU 13     ; Data Output
M_PCE EQU 15   ; Prescaled Clock Enable
M_TOF EQU 20     ; Timer Overflow Flag
M_TCF EQU 21     ; Timer Compare Flag

;       Timer Prescaler Register Bit Flags

M_PS EQU $600000  ; Prescaler Source Mask
M_PS0 EQU 21
M_PS1 EQU 22

;      Timer Control Bits
M_TC0 EQU 4      ; Timer Control 0
M_TC1 EQU 5      ; Timer Control 1
M_TC2 EQU 6      ; Timer Control 2
M_TC3 EQU 7      ; Timer Control 3


;---------------------------------------------------------------------------
;
;       EQUATES for Direct Memory Access (DMA)
;
;---------------------------------------------------------------------------

;       Register Addresses Of DMA
M_DSTR EQU $FFFFF4; DMA Status Register
M_DOR0 EQU $FFFFF3; DMA Offset Register 0
M_DOR1 EQU $FFFFF2; DMA Offset Register 1
M_DOR2 EQU $FFFFF1; DMA Offset Register 2
M_DOR3 EQU $FFFFF0; DMA Offset Register 3


;       Register Addresses Of DMA0

M_DSR0 EQU $FFFFEF; DMA0 Source Address Register
M_DDR0 EQU $FFFFEE; DMA0 Destination Address Register
M_DCO0 EQU $FFFFED; DMA0 Counter
M_DCR0 EQU $FFFFEC; DMA0 Control Register

;       Register Addresses Of DMA1

M_DSR1 EQU $FFFFEB; DMA1 Source Address Register
M_DDR1 EQU $FFFFEA; DMA1 Destination Address Register
M_DCO1 EQU $FFFFE9; DMA1 Counter
M_DCR1 EQU $FFFFE8; DMA1 Control Register

;       Register Addresses Of DMA2

M_DSR2 EQU $FFFFE7; DMA2 Source Address Register
M_DDR2 EQU $FFFFE6; DMA2 Destination Address Register
M_DCO2 EQU $FFFFE5; DMA2 Counter
M_DCR2 EQU $FFFFE4; DMA2 Control Register

;       Register Addresses Of DMA4
```

```
M_BME EQU 12     ; Mastership Enable
M_BRE EQU 13     ; Refresh Enable
M_BSTR EQU 14     ; Software Triggered Refresh
M_BRF EQU $7F8000; Refresh Rate Bits Mask (BRF0-BRF7)
M_BRP EQU 23     ; Refresh prescaler

;       Address Attribute Registers

M_BAT EQU $3     ; External Access Type and Pin Definition Bits Mask (BAT0-BAT1)
M_BAAP EQU 2      ; Address Attribute Pin Polarity
M_BPEN EQU 3      ; Program Space Enable
M_BXEN EQU 4      ; X Data Space Enable
M_BYEN EQU 5      ; Y Data Space Enable
M_BAM EQU 6      ; Address Muxing
M_BPAC EQU 7   ; Packing Enable
M_BNC EQU $F00   ; Number of Address Bits to Compare Mask (BNC0-BNC3)
M_BAC EQU $FFF000; Address to Compare Bits Mask (BAC0-BAC11)

;       control and status bits in SR

M_CP EQU $c00000 ; mask for CORE-DMA priority bits in SR
M_CA EQU 0       ; Carry
M_V EQU 1       ; Overflow
M_Z EQU 2       ; Zero
M_N EQU 3       ; Negative
M_U EQU 4       ; Unnormalized
M_E EQU 5       ; Extension
M_L EQU 6       ; Limit
M_S EQU 7       ; Scaling Bit
M_I0 EQU 8       ; Interupt Mask Bit 0
M_I1 EQU 9       ; Interupt Mask Bit 1
M_S0 EQU 10      ; Scaling Mode Bit 0
M_S1 EQU 11      ; Scaling Mode Bit 1
M_SC EQU 13      ; Sixteen_Bit Compatibility
M_DM EQU 14      ; Double Precision Multiply
M_LF EQU 15      ; DO-Loop Flag
M_FV EQU 16      ; DO-Forever Flag
M_SA EQU 17      ; Sixteen-Bit Arithmetic
M_CE EQU 19      ; Instruction Cache Enable
M_SM EQU 20      ; Arithmetic Saturation
M_RM EQU 21      ; Rounding Mode
M_CP0 EQU22      ; bit 0 of priority bits in SR
M_CP1 EQU 23      ; bit 1 of priority bits in SR

;       control and status bits in OMR
M_CDP EQU$300  ; mask for CORE-DMA priority bits in OMR
M_MA EQU 0       ; Operating Mode A
M_MB EQU 1       ; Operating Mode B
M_MC EQU 2       ; Operating Mode C
M_MD EQU 3       ; Operating Mode D
M_EBD EQU 4       ; External Bus Disable bit in OMR
M_SD EQU 6       ; Stop Delay
M_CDP0 EQU 8       ; bit 0 of priority bits in OMR
M_CDP1 EQU 9       ; bit 1 of priority bits in OMR
M_BEN EQU 10      ; Burst Enable
M_TAS EQU 11      ; TA Synchronize Select
M_BRT EQU 12      ; Bus Release Timing
M_XYS EQU 16      ; Stack Extension space select bit in OMR.
M_EUN EQU 17      ; Extensed stack UNderflow flag in OMR.
M_EOV EQU 18      ; Extended stack OVerflow flag in OMR.
```