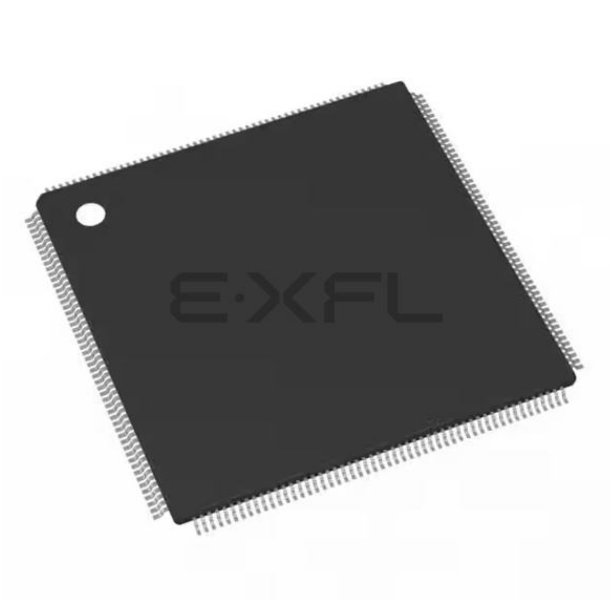

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	80MHz
Non-Volatile Memory	ROM (9kB)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56301ag80

1.5.3 External Bus Control

Table 1-8. External Bus Control Signals

Signal Name	Type	State During Reset	Signal Description
AA0/$\overline{\text{RAS0}}$–AA3/$\overline{\text{RAS3}}$	Output	Tri-stated	**Address Attribute or Row Address Strobe** As AA, these signals function as chip selects or additional address lines. Unlike address lines, however, the AA lines do not hold their state after a read or write operation. As $\overline{\text{RAS}}$, these signals can be used for Dynamic Random Access Memory (DRAM) interface. These signals have programmable polarity.
$\overline{\text{RD}}$	Output	Tri-stated	**Read Enable** When the DSP is the bus master, $\overline{\text{RD}}$ is asserted to read external memory on the data bus (D[0–23]). Otherwise, $\overline{\text{RD}}$ is tri-stated.
$\overline{\text{WR}}$	Output	Tri-stated	**Write Enable** When the DSP is the bus master, $\overline{\text{WR}}$ is asserted to write external memory on the data bus (D[0–23]). Otherwise, $\overline{\text{WR}}$ is tri-stated.
$\overline{\text{TA}}$	Input	Ignored Input	**Transfer Acknowledge** If the DSP56301 is the bus master and there is no external bus activity, or the DSP56301 is not the bus master, the $\overline{\text{TA}}$ input is ignored. The $\overline{\text{TA}}$ input is a Data Transfer Acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2,..., infinity) can be added to the wait states inserted by the BCR by keeping $\overline{\text{TA}}$ deasserted. In typical operation, $\overline{\text{TA}}$ is deasserted at the start of a bus cycle, asserted to enable completion of the bus cycle, and deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{\text{TA}}$ is asserted synchronous to CLKOUT. The number of wait states is determined by the $\overline{\text{TA}}$ input or by the Bus Control Register (BCR), whichever is longer. The BCR can set the minimum number of wait states in external bus cycles. To use the $\overline{\text{TA}}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{\text{TA}}$ deassertion; otherwise improper operation may result. $\overline{\text{TA}}$ can operate synchronously or asynchronously, depending on the setting of the TAS bit in the Operating Mode Register (OMR). $\overline{\text{TA}}$ functionality cannot be used during DRAM-type accesses; otherwise improper operation may result.
$\overline{\text{BR}}$	Output	Output (deasserted)	**Bus Request** Asserted when the DSP requests bus mastership and deasserted when the DSP no longer needs the bus. $\overline{\text{BR}}$ can be asserted or deasserted independently of whether the DSP56301 is a bus master or a bus slave. Bus “parking” allows $\overline{\text{BR}}$ to be deasserted even though the DSP56301 is the bus master (see the description of bus “parking” in the $\overline{\text{BB}}$ signal description). The Bus Request Hole (BRH) bit in the BCR allows $\overline{\text{BR}}$ to be asserted under software control, even though the DSP does not need the bus. $\overline{\text{BR}}$ is typically sent to an external bus arbitrator that controls the priority, parking and tenure of each master on the same external bus. $\overline{\text{BR}}$ is affected only by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{\text{BR}}$ is deasserted and the arbitration is reset to the bus slave state.
$\overline{\text{BG}}$	Input	Ignored Input	**Bus Grant** Must be asserted/deasserted synchronous to CLKOUT for proper operation. An external bus arbitration circuit asserts $\overline{\text{BG}}$ when the DSP56301 becomes the next bus master. When $\overline{\text{BG}}$ is asserted, the DSP56301 must wait until $\overline{\text{BB}}$ is deasserted before taking bus mastership. When $\overline{\text{BG}}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution.

1.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After $\overline{\text{RESET}}$ is deasserted, these inputs are hardware interrupt request lines.

Table 1-9. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
MODA $\overline{\text{IRQA}}$	Input Input	Input	**Mode Select A** Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input $\overline{\text{IRQA}}$ during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted. **External Interrupt Request A** Internally synchronized to CLKOUT. If $\overline{\text{IRQA}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQA}}$ to exit the Wait state. If the processor is in the Stop stand-by state and $\overline{\text{IRQA}}$ is asserted, the processor exits the Stop state. These inputs are 5 V tolerant.
MODB $\overline{\text{IRQB}}$	Input Input	Input	**Mode Select B** Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input $\overline{\text{IRQB}}$ during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted. **External Interrupt Request B** Internally synchronized to CLKOUT. If $\overline{\text{IRQB}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQB}}$ to exit the Wait state. If the processor is in the Stop stand-by state and $\overline{\text{IRQC}}$ is asserted, the processor will exit the Stop state. These inputs are 5 V tolerant.
MODC $\overline{\text{IRQC}}$	Input Input	Input	**Mode Select C** Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input $\overline{\text{IRQC}}$ during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted. **External Interrupt Request C** Internally synchronized to CLKOUT. If $\overline{\text{IRQC}}$ is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting $\overline{\text{IRQC}}$ to exit the Wait state. If the processor is in the Stop stand-by state and $\overline{\text{IRQC}}$ is asserted, the processor exits the Stop state. These inputs are 5 V tolerant.

Table 1-12. Enhanced Synchronous Serial Interface 0 (ESSI0) (Continued)

Signal Name	Type	State During Reset	Signal Description
SCK0 PC3	Input/Output Input or Output	Input	**Serial Clock** Provides the serial bit rate clock for the ESSI interface for both the transmitter and receiver in Synchronous modes, or the transmitter only in Asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6 T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock. **Port C 3** The default configuration following reset is GPIO. For PC3, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SCK0 through PCR0. This input is 5 V tolerant.
SRD0 PC4	Input/Output Input or Output	Input	**Serial Receive Data** Receives serial data and transfers the data to the ESSI receive shift register. SRD0 is an input when data is being received. **Port C 4** The default configuration following reset is GPIO. For PC4, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SRD0 through PCR0. This input is 5 V tolerant.
STD0 PC5	Input/Output Input or Output	Input	**Serial Transmit Data** Transmits data from the serial transmit shift register. STD0 is an output when data is being transmitted. **Port C 5** The default configuration following reset is GPIO. For PC5, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal STD0 through PCR0. This input is 5 V tolerant.

Table 1-13. Enhanced Synchronous Serial Interface 1 (ESSI1) (Continued)

Signal Name	Type	State During Reset	Signal Description
SRD1 PD4	Input/Output Input or Output	Input	**Serial Receive Data** Receives serial data and transfers it to the ESSI receive shift register. SRD1 is an input when data is being received. **Port D 4** The default configuration following reset is GPIO. For PD4, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SRD1 through PCR1. This input is 5 V tolerant.
STD1 PD5	Input/Output Input or Output	Input	**Serial Transmit Data** Transmits data from the serial transmit shift register. STD1 is an output when data is being transmitted. **Port D 5** The default configuration following reset is GPIO. For PD5, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal STD1 through PCR1. This input is 5 V tolerant.

1.10 Serial Communication Interface (SCI)

The Serial Communication interface (SCI) provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-14. Serial Communication Interface (SCI)

Signal Name	Type	State During Reset	Signal Description
RXD PE0	Input Input or Output	Input	**Serial Receive Data** Receives byte-oriented serial data and transfers it to the SCI receive shift register. **Port E 0** The default configuration following reset is GPIO. When configured as PE0, signal direction is controlled through the SCI Port Directions Register (PRR). The signal can be configured as an SCI signal RXD through the SCI Port Control Register (PCR). This input is 5 V tolerant.
TXD PE1	Output Input or Output	Input	**Serial Transmit Data** Transmits data from SCI transmit data register. **Port E 1** The default configuration following reset is GPIO. When configured as PE1, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal TXD through the SCI PCR. This input is 5 V tolerant.

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
21	Delay from $\overline{\text{WR}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1] • DRAM for all WS[7] • SRAM WS = 1 • SRAM WS = 2, 3 • SRAM WS ≥ 4	**80 MHz**: $(WS + 3.5) \times T_C - 12.4$ **100 MHz**: $(WS + 3.5) \times T_C - 10.94$ **80 MHz**: $(WS + 3.5) \times T_C - 12.4$ **100 MHz**: $(WS + 3.5) \times T_C - 10.94$ **80 MHz**: $(WS + 3) \times T_C - 12.4$ **100 MHz**: $(WS + 3) \times T_C - 10.94$ **80 MHz**: $(WS + 2.5) \times T_C - 12.4$ **100 MHz**: $(WS + 2.5) \times T_C - 10.94$	— — — —	Note 8 Note 8 Note 8 Note 8	— — — —	Note 8 Note 8 Note 8 Note 8	ns ns ns ns ns ns ns ns
22	Synchronous interrupt setup time from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to the CLKOUT Transition 2		7.4	T_C	5.9	T_C	ns
23	Synchronous interrupt delay time from the CLKOUT Transition 2 to the first external address output valid caused by the first instruction fetch after coming out of Wait Processing state • Minimum • Maximum	$8.25 \times T_C + 1.0$ $24.75 \times T_C + 5.0$	116.6 —	— 314.4	83.5 —	— 252.5	ns ns
24	Duration for $\overline{\text{IRQA}}$ assertion to recover from Stop state		7.4	—	5.9	—	ns
25	Delay from $\overline{\text{IRQA}}$ assertion to fetch of first instruction (when exiting Stop)[2, 3] • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay)	$PLC \times ET_C \times PDF + (128\ K - PLC/2) \times T_C$ $PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$ $(9.25 \pm 0.5) \times TC$	1.6 290.6 ns 109.4	17.0 15.4 ms 121.9	1.3 232.5 ns 87.5	13.6 12.3 ms 97.5	ms ns
26	Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[2, 3] • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay)	$PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$ $PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$ $5.5 \times T_C$	17.0 15.4 68.8	— — —	13.6 12.3 55.0	— — —	ms ms ns
27	Interrupt Request Rate • HI32, ESSI, SCI, Timer • DMA • $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger) • $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (level trigger)	$12 \times T_C$ $8 \times T_C$ $8 \times T_C$ $12 \times T_C$	— — — —	150.0 100.0 100.0 150.0	— — — —	120.0 80.0 80.0 120.0	ns ns ns ns

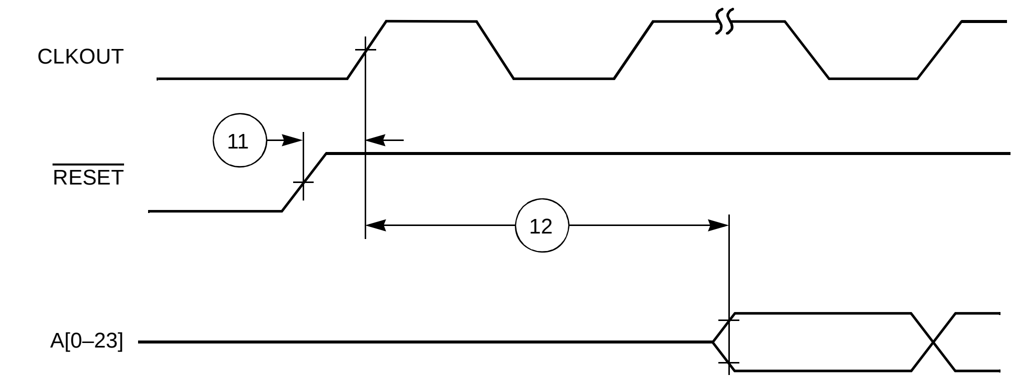
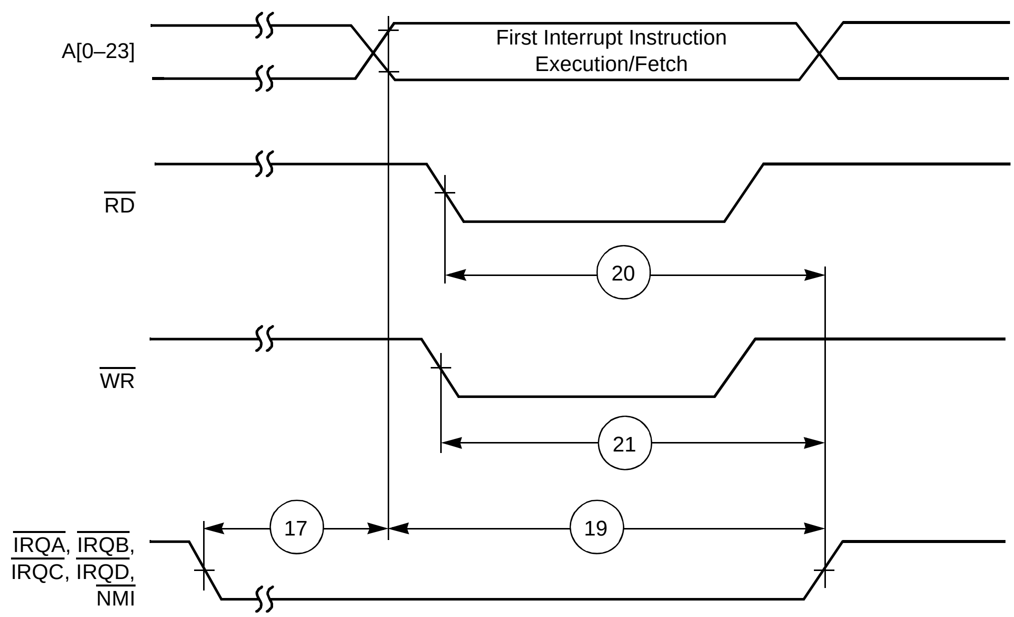
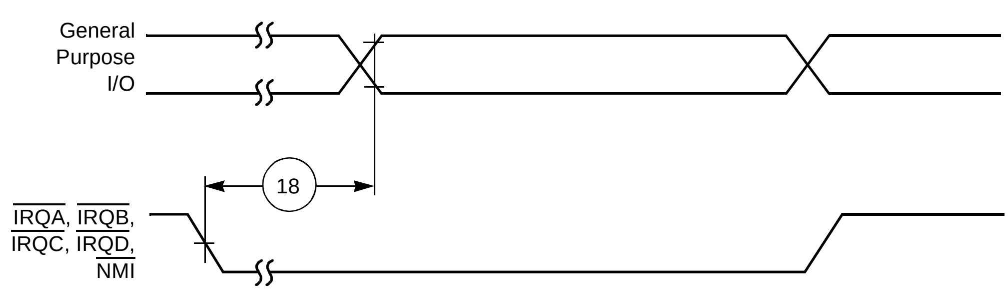


Figure 2-4. Synchronous Reset Timing



a) First Interrupt Instruction Execution



b) General-Purpose I/O

Figure 2-5. External Fast Interrupt Timing

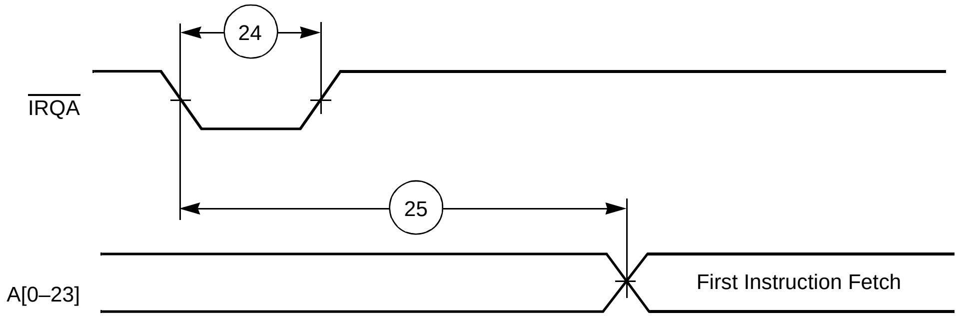


Figure 2-9. Recovery from Stop State Using IRQA

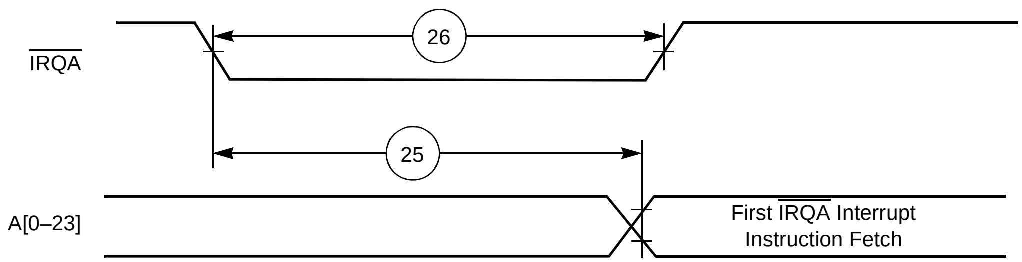


Figure 2-10. Recovery from Stop State Using IRQA Interrupt Service

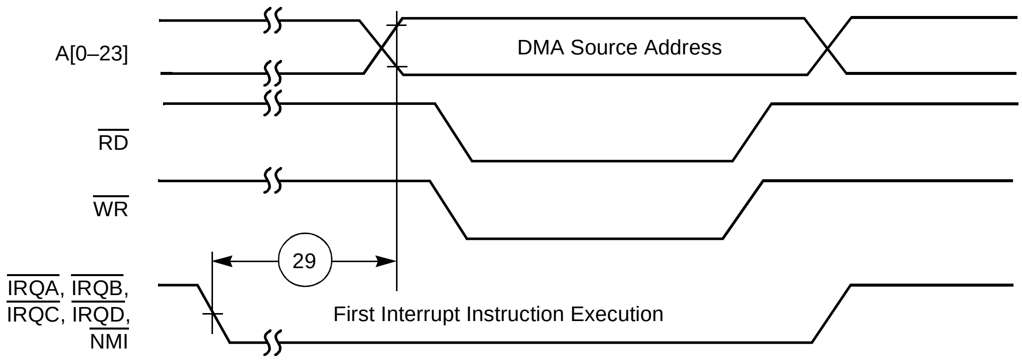


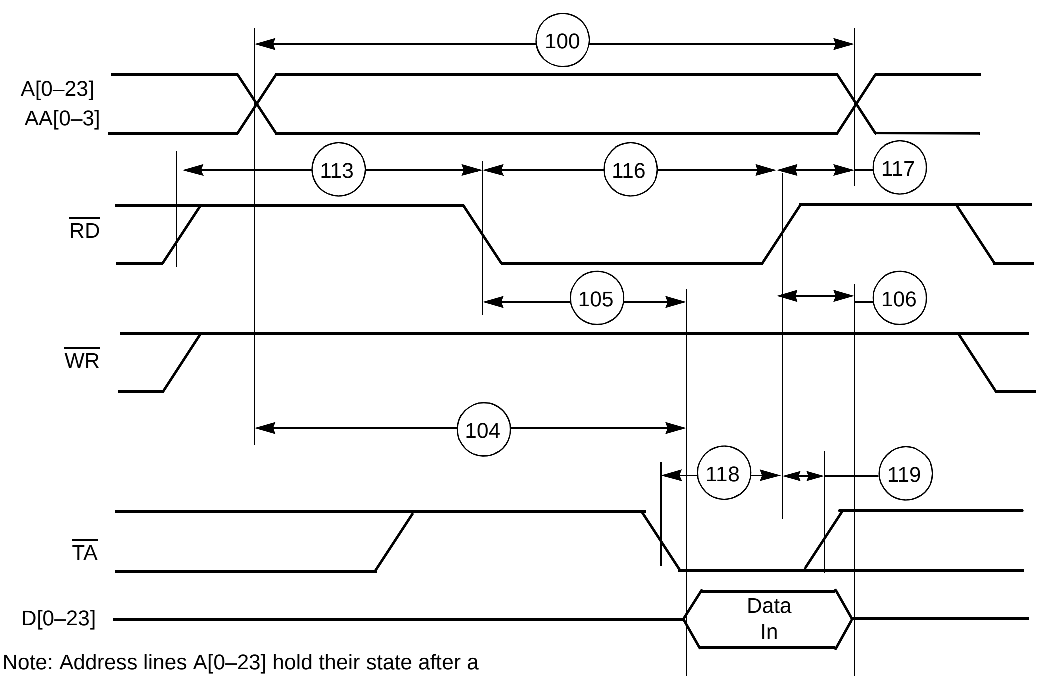
Figure 2-11. External Memory Access (DMA Source) Timing

2.5.5 External Memory Expansion Port (Port A)

Table 2-8. SRAM Read and Write Accesses[3,6] (Continued)

No.	Characteristics	Symbol	Expression[1]	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
115	Address valid to $\overline{RD}$ assertion		$0.5 \times T_C - 4.0$	2.3	—	1.0	—	ns
116	$\overline{RD}$ assertion pulse width		$(WS + 0.25) \times T_C - 4.0$	11.6	—	8.5	—	ns
117	$\overline{RD}$ deassertion to address not valid		$0.25 \times T_C - 2.0$ $[1 \leq WS \leq 3]$ $1.25 \times T_C - 2.0$ $[4 \leq WS \leq 7]$ $2.25 \times T_C - 2.0$ $[WS \geq 8]$	1.1 13.6 26.1	— — —	0.5 10.5 20.5	— — —	ns ns ns
118	$\overline{TA}$ setup before $\overline{RD}$ or $\overline{WR}$ deassertion[4]		$0.25 \times T_C + 2.0$	5.1	—	4.5	—	ns
119	$\overline{TA}$ hold after $\overline{RD}$ or $\overline{WR}$ deassertion			0	—	0	—	ns

Notes:
1. WS is the number of wait states specified in the BCR.
2. Timings 100, 107 are guaranteed by design, not tested.
3. All timings for 100 MHz are measured from 0.5 · Vcc to 0.5 · Vcc
4. Timing 118 is relative to the deassertion edge of $\overline{RD}$ or $\overline{WR}$ even if $\overline{TA}$ remains active.
5. Timings 110, 111, and 112, are not helpful and are not specified for 100 MHz.
6. $V_{CC} = 3.3$ V $\pm$ 0.3 V; $T_J = -40$°C to +100°C, $C_L = 50$ pF



Note: Address lines A[0–23] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-12. SRAM Read Access

Table 2-14. DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
170	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 6.0$	74.1	—	56.5	—	ns
171	Row address valid to $\overline{\text{RAS}}$ assertion	t_{ASR}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
172	$\overline{\text{RAS}}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C - 4.0$	30.4	—	23.5	—	ns
173	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	5.4	—	3.5	—	ns
174	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
175	$\overline{\text{RAS}}$ assertion to column address not valid	t_{AR}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
176	Column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$7 \times T_C - 4.0$	83.5	—	66.0	—	ns
177	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	$5 \times T_C - 3.8$	58.7	—	46.2	—	ns
178	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	18.2	—	13.8	—	ns
179	$\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}$[4] assertion	t_{RRH}	**80 MHz**: $0.25 \times T_C - 2.6$ **100 MHz**: $0.25 \times T_C - 2.0$	0.5 —	— —	— 0.5	— —	ns ns
180	$\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCH}	$6 \times T_C - 4.2$	70.8	—	55.8	—	ns
181	$\overline{\text{RAS}}$ assertion to $\overline{\text{WR}}$ deassertion	t_{WCR}	$9.5 \times T_C - 4.2$	114.6	—	90.8	—	ns
182	$\overline{\text{WR}}$ assertion pulse width	t_{WP}	$15.5 \times T_C - 4.5$	189.3	—	150.5	—	ns
183	$\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RWL}	$15.75 \times T_C - 4.3$	192.6	—	153.2	—	ns
184	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CWL}	$14.25 \times T_C - 4.3$	173.8	—	138.2	—	ns
185	Data valid to $\overline{\text{CAS}}$ assertion (write)	t_{DS}	$8.75 \times T_C - 4.0$	105.4	—	83.5	—	ns
186	$\overline{\text{CAS}}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
187	$\overline{\text{RAS}}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
188	$\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{WCS}	$9.5 \times T_C - 4.3$	114.5	—	90.7	—	ns
189	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns
190	$\overline{\text{RAS}}$ deassertion to $\overline{\text{CAS}}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C - 4.0$	55.4	—	43.5	—	ns
191	$\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{ROH}	$15.5 \times T_C - 4.0$	189.8	—	151.0	—	ns
192	$\overline{\text{RD}}$ assertion to data valid	t_{GA}	**80 MHz**: $14 \times T_C - 6.5$ **100 MHz**: $14 \times T_C - 5.7$	— —	168.5 —	— —	— 134.3	ns ns
193	$\overline{\text{RD}}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{\text{WR}}$ assertion to data active		$0.75 \times T_C - 1.5$	9.1	—	6.0	—	ns
195	$\overline{\text{WR}}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for an out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{\text{RD}}$ deassertion always occurs after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

2.5.5.3 Synchronous Timings (SRAM)

Table 2-15. External Bus Synchronous Timings (SRAM Access)[3]

No.	Characteristics	Expression[1,2]	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
196	CLKOUT high to $\overline{BS}$ assertion	$0.25 \times T_C$ +5.2/–0.5	2.6	8.3	2.0	7.7	ns
197	CLKOUT high to $\overline{BS}$ deassertion	$0.75 \times T_C$ +4.2/–1.0	8.4	13.6	6.5	11.7	ns
198	CLKOUT high to address, and AA valid[4]	$0.25 \times T_C + 2.5$	—	5.6	—	5.0	ns
199	CLKOUT high to address, and AA invalid[4]	$0.25 \times T_C - 0.7$	2.4	—	1.8	—	ns
200	$\overline{TA}$ valid to CLKOUT high (setup time)		5.8	—	4.0	—	ns
201	CLKOUT high to $\overline{TA}$ invalid (hold time)		0.0	—	0.0	—	ns
202	CLKOUT high to data out active	$0.25 \times T_C$	3.1	—	2.5	—	ns
203	CLKOUT high to data out valid	**80 MHz**: $0.25 \times T_C + 4.5$ **100 MHz**: $0.25 \times T_C + 4.0$	— —	7.6 —	— —	— 6.5	ns ns
204	CLKOUT high to data out invalid	$0.25 \times T_C$	3.1	—	2.5	—	ns
205	CLKOUT high to data out high impedance	**80 MHz**: $0.25 \times T_C + 0.5$ **100 MHz**: $0.25 \times T_C$	— —	3.6 —	— —	— 2.5	ns ns
206	Data in valid to CLKOUT high (setup)		5.0	—	4.0	—	ns
207	CLKOUT high to data in invalid (hold)		0.0	—	0.0	—	ns
208	CLKOUT high to $\overline{RD}$ assertion	maximum: $0.75 \times T_C + 2.5$	10.4	 11.9	6.7	 10.0	ns ns
209	CLKOUT high to $\overline{RD}$ deassertion		0.0	4.5	0.0	4.0	ns
210	CLKOUT high to $\overline{WR}$ assertion[2]	$0.5 \times T_C + 4.3$ [WS = 1 or WS $\geq$ 4] [2 $\leq$ WS $\leq$ 3]	7.6 1.3	10.6 4.8	4.5 0.0	9.3 4.3	ns ns
211	CLKOUT high to $\overline{WR}$ deassertion		0.0	4.3	0.0	3.8	ns

Notes:
1. WS is the number of wait states specified in the BCR.
2. If WS > 1, $\overline{WR}$ assertion refers to the next rising edge of CLKOUT.
3. External bus synchronous timings should be used only for reference to the clock and *not* for relative timings.
4. T198 and T199 are valid for Address Trace mode if the ATE bit in the Operating Mode Register is set. Use the status of $\overline{BR}$ (See T212) to determine whether the access referenced by A[0–23] is internal or external in this mode.

2.5.5.4 Arbitration Timings

Table 2-16. Arbitration Bus Timings[1].

No.	Characteristics	Expression[2]	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
212	CLKOUT high to $\overline{\text{BR}}$ assertion/deassertion[3]		1.0	4.5	0.0	4.0	ns
213	$\overline{\text{BG}}$ asserted/deasserted to CLKOUT high (setup)		5.0	—	4.0	—	ns
214	CLKOUT high to $\overline{\text{BG}}$ deasserted/asserted (hold)		0.0	—	0.0	—	ns
215	$\overline{\text{BB}}$ deassertion to CLKOUT high (input setup)		5.0	—	4.0	—	ns
216	CLKOUT high to $\overline{\text{BB}}$ assertion (input hold)		0.0	—	0.0	—	ns
217	CLKOUT high to $\overline{\text{BB}}$ assertion (output)		1.0	4.5	0.0	4.0	ns
218	CLKOUT high to $\overline{\text{BB}}$ deassertion (output)		1.0	4.5	0.0	4.0	ns
219	$\overline{\text{BB}}$ high to $\overline{\text{BB}}$ high impedance (output)		—	5.6	—	4.5	ns
220	CLKOUT high to address and controls active	$0.25 \times T_C$	3.1	—	2.5	—	ns
221	CLKOUT high to address and controls high impedance	$0.75 \times T_C$	—	9.4	—	7.5	ns
222	CLKOUT high to AA active	$0.25 \times T_C$	3.1	—	2.5	—	ns
223	CLKOUT high to AA deassertion	maximum: $0.25 \times T_C + 4.0$	4.1	7.1	2.0	6.5	ns
224	CLKOUT high to AA high impedance	$0.75 \times T_C$	—	9.4	—	7.5	ns

Notes:
1. Synchronous Bus Arbitration is not recommended. Use Asynchronous mode whenever possible.
2. An expression is used to compute the maximum or minimum value listed, as appropriate. For timing 223, the minimum is an absolute value.
3. T212 is valid for Address Trace mode when the ATE bit in the Operating Mode Register is set. $\overline{\text{BR}}$ is deasserted for internal accesses and asserted for external accesses.

Table 2-19. Universal Bus Mode, Synchronous Port A Type Host Timing (Continued)

No.	Characteristic	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
330	$\overline{\text{HIRQ}}$ High Impedance from Data Strobe Assertion (HIRH = 1, HIRD = 0)[1,6]	**80 MHz:** $2.5 \times T_C + 24.7$ **100 MHz:** $2.5 \times T_C + 21.5$	—	55.9	—	46.5	ns ns
331	$\overline{\text{HIRQ}}$ Active from Data Strobe Deassertion (HIRH = 1, HIRD = 0)[1]	$2.5 \times T_C$	31.3	—	25.0	—	ns
332	$\overline{\text{HIRQ}}$ Deasserted Hold from Data Strobe Deassertion[1]	$2.5 \times T_C$	31.3	—	25.0	—	ns
346	HRST Assertion to Host Port Pins High Impedance[2]		—	22.2	—	19.6	ns
347	$\overline{\text{HBS}}$ Assertion to CLKOUT Rising Edge		4.3	—	3.4	—	ns
348	Data Strobe Deassertion to CLKOUT Rising Edge[1]		7.4	—	5.9	—	ns

Notes:
1. The Data Strobe is $\overline{\text{HRD}}$ or $\overline{\text{HWR}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
2. HTA, HDRQ, and HRST may be programmed as active-high or active-low. In the example timing diagrams, HDRQ and HRST are shown as active-high and $\overline{\text{HTA}}$ is shown as active low.
3. The Read Data Strobe is $\overline{\text{HRD}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
4. The Write Data Strobe is $\overline{\text{HWR}}$ in the Dual Data Strobe mode and $\overline{\text{HDS}}$ in the Single Data Strobe mode.
5. $\overline{\text{HTA}}$ requires an external pull-down resistor if programmed as active high (HTAP = 0); or an external pull-up resistor if programmed as active low (HTAP = 1). The resistor value should be consistent with the DC specifications.
6. $\overline{\text{HIRQ}}$ requires an external pull-up resistor if programmed as open drain (HIRD = 0). The resistor value should be consistent with the DC specifications.
7. "LT" is the value of the latency timer register (CLAT) as programmed by the user during self configuration.
8. Values are valid for $V_{CC} = 3.3 \pm 0.3V$

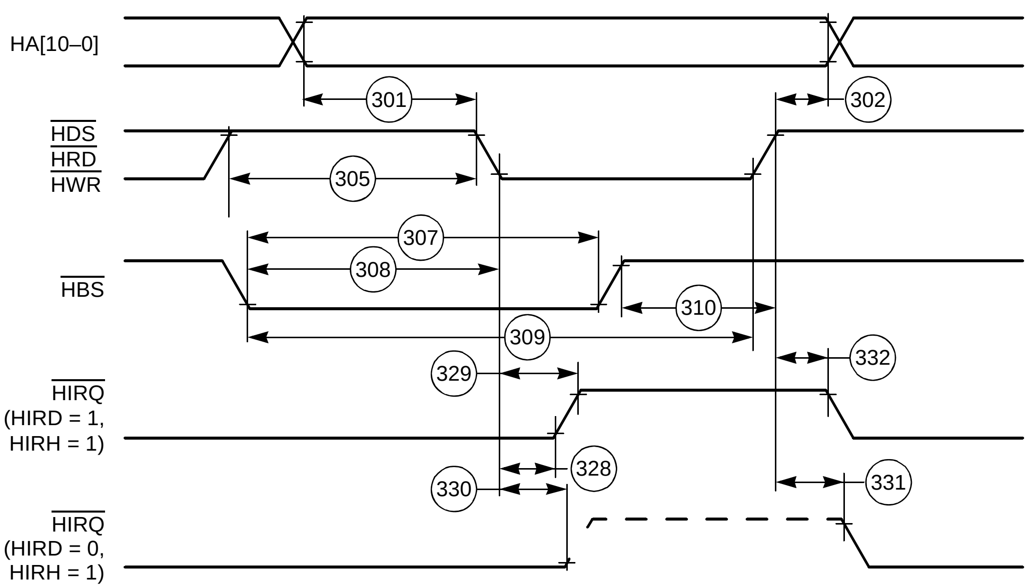


Figure 2-27. Universal Bus Mode I/O Access Timing

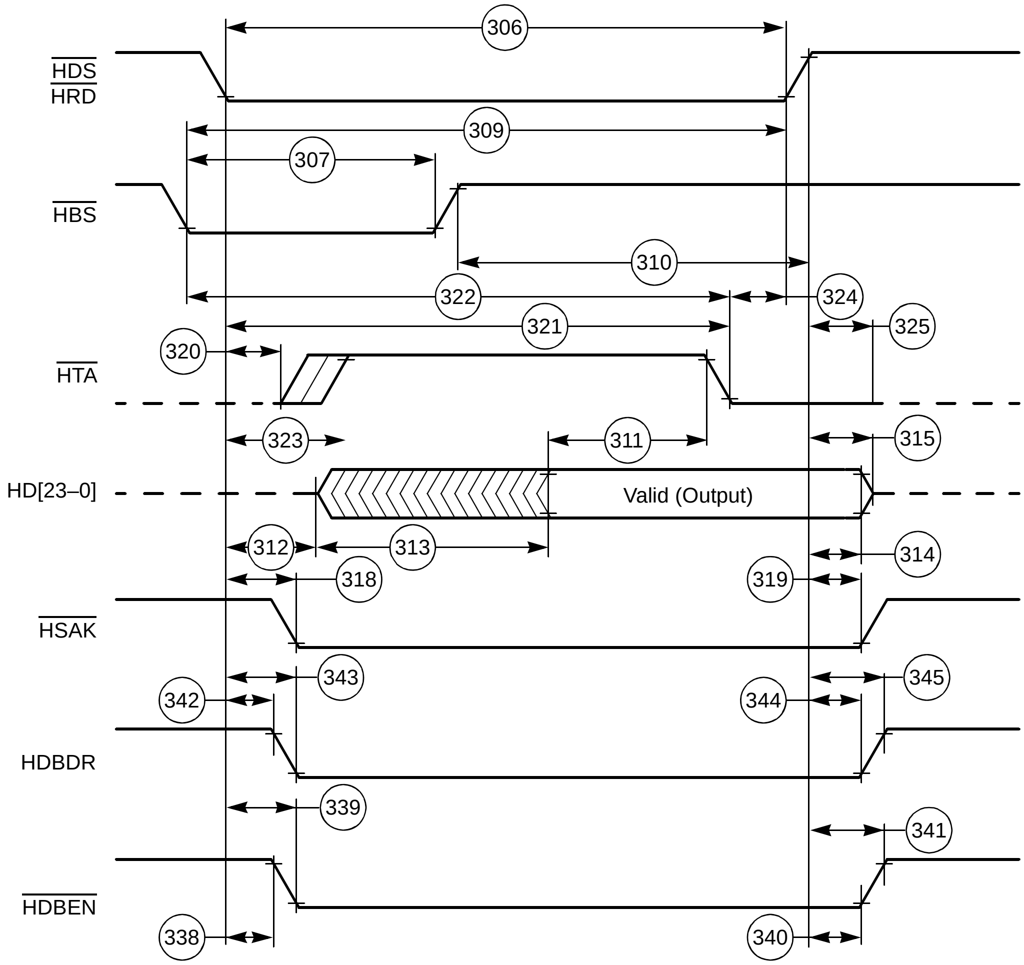


Figure 2-32. Read Timing

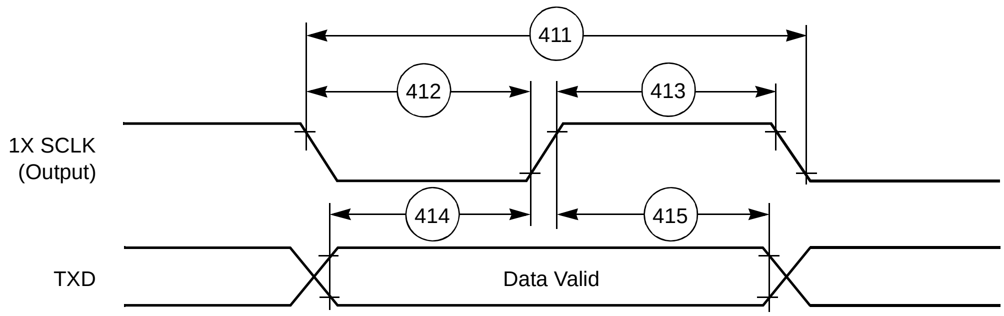


Figure 2-39. SCI Asynchronous Mode Timing

2.5.8 ESSI0/ESSI1 Timing

Table 2-22. ESSI Timings

No.	Characteristics[4, 5, 7]	Symbol	Expression	80 MHz		100 MHz		Condition[6]	Unit
				Min	Max	Min	Max		
430	Clock cycle[1]	t_{SSICC}	$3 \times T_C$ $4 \times T_C$	50.0 37.5	— —	30.0 40.0	— —	x ck i ck	ns
431	Clock high period For internal clock For external clock		 $2 \times T_C - 10.0$ $1.5 \times T_C$	 15.0 18.8	 — —	 10.0 15.0	 — —		 ns ns
432	Clock low period For internal clock For external clock		 $2 \times T_C - 10.0$ $1.5 \times T_C$	 15.0 18.8	 — —	 10.0 15.0	 — —		 ns ns
433	RXC rising edge to FSR out (bl) high			— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bl) low			— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (wr) high[2]			— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
436	RXC rising edge to FSR out (wr) low[2]			— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
437	RXC rising edge to FSR out (wl) high			— —	36.0 21.0	— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (wl) low			— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (SCK in Synchronous mode) falling edge			10.0 19.0	— —	10.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[2]			1.0 23.0	— —	1.0 23.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge			3.5 23.0	— —	3.5 23.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	3.0 0.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge			5.5 19.0	— —	5.5 19.0	— —	x ck i ck s	ns

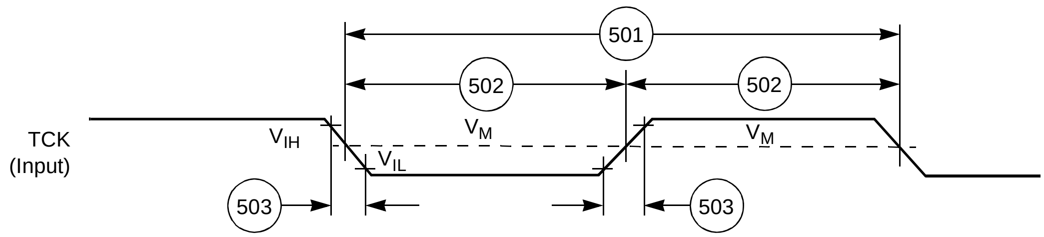


Figure 2-46. Test Clock Input Timing Diagram

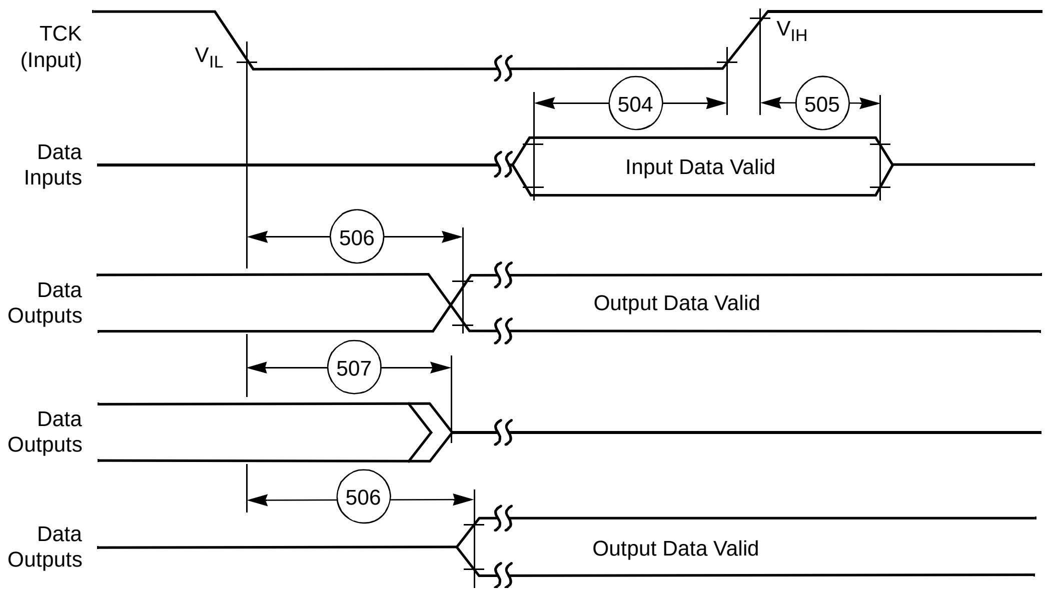


Figure 2-47. Boundary Scan (JTAG) Timing Diagram

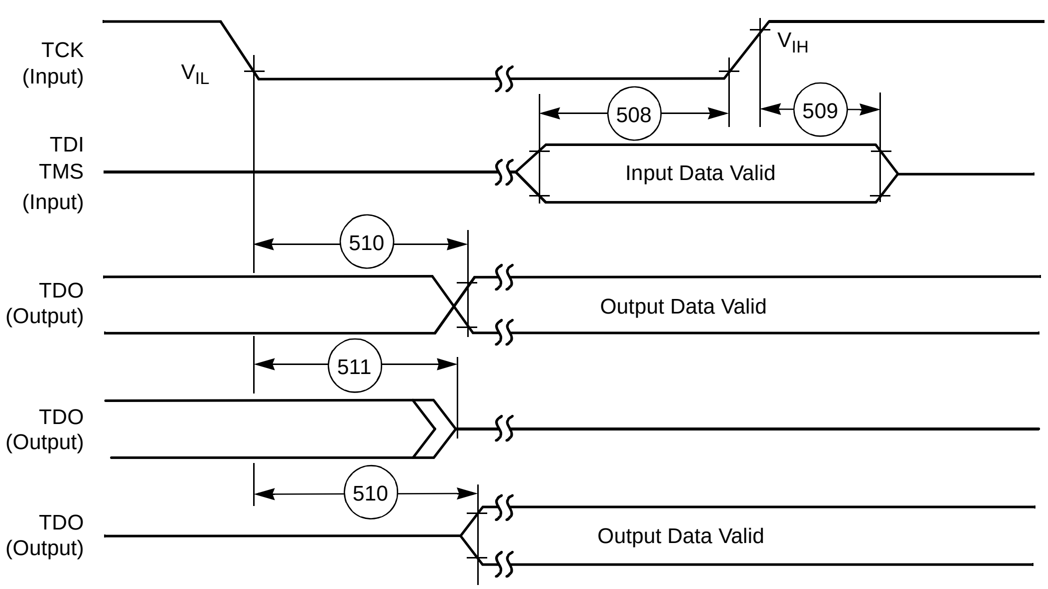
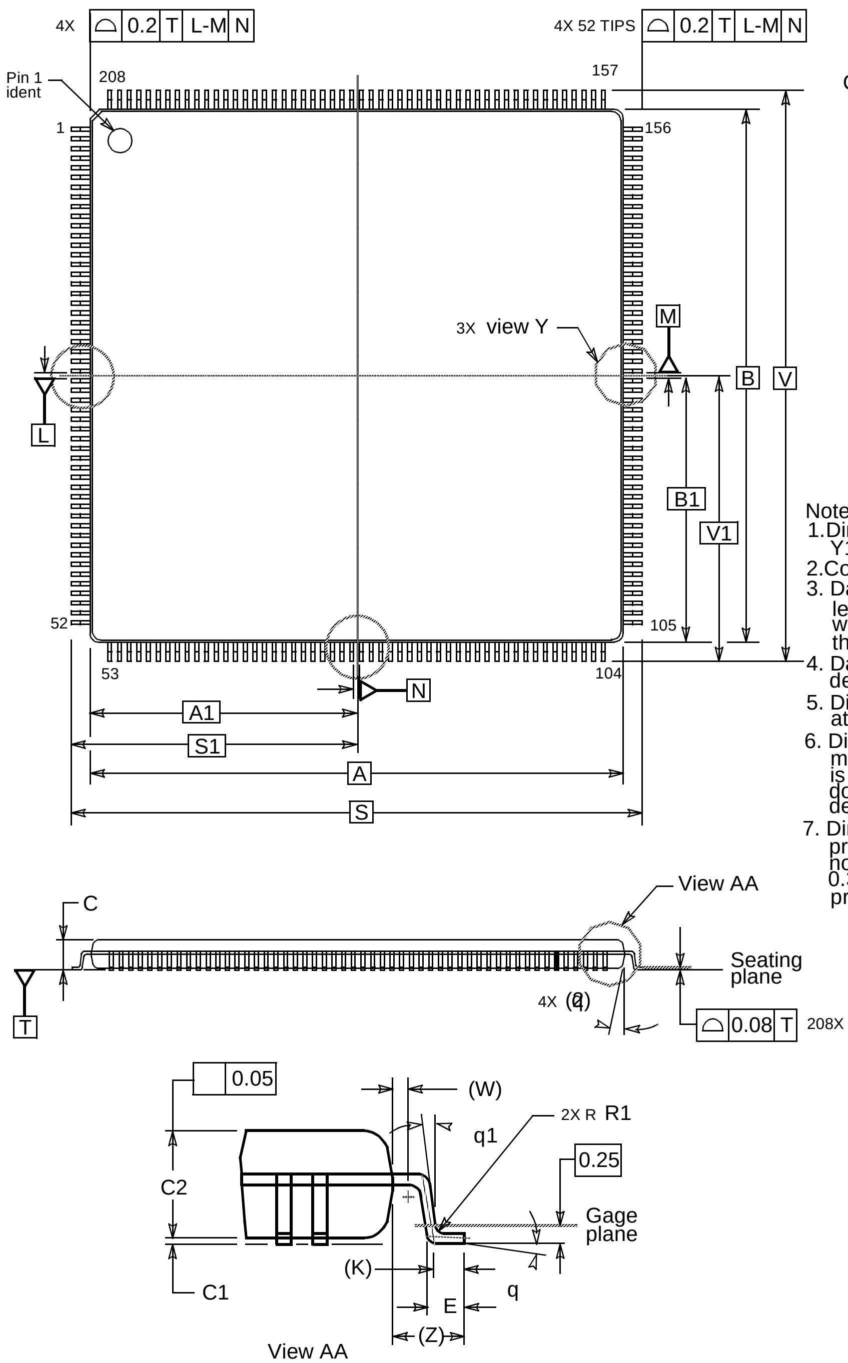


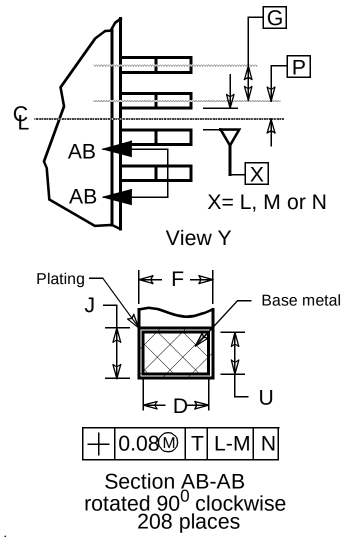
Figure 2-48. Test Access Port Timing Diagram

Table 3-1. DSP56301 TQFP Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	AA0/$\overline{\text{RAS0}}$	26	EXTAL	51	A14
2	AA1/$\overline{\text{RAS1}}$	27	GND_Q	52	A15
3	V_{CCN}	28	$\overline{\text{BCLK}}$	53	NC
4	GND_N	29	A0	54	NC
5	CLKOUT	30	A1	55	A16
6	BCLK	31	GND_A	56	A17
7	$\overline{\text{CAS}}$	32	V_{CCA}	57	GND_A
8	$\overline{\text{TA}}$	33	A2	58	V_{CCA}
9	PINIT/$\overline{\text{NMI}}$	34	A3	59	A18
10	$\overline{\text{RESET}}$	35	A4	60	A19
11	V_{CCP}	36	A5	61	A20
12	PCAP	37	GND_A	62	A21
13	GND_P	38	V_{CCA}	63	GND_A
14	GND_{P1}	39	A6	64	V_{CCA}
15	$\overline{\text{BB}}$	40	A7	65	A22
16	$\overline{\text{BG}}$	41	A8	66	A23
17	$\overline{\text{BR}}$	42	A9	67	D0
18	V_{CCN}	43	GND_A	68	D1
19	GND_N	44	V_{CCA}	69	D2
20	AA2/$\overline{\text{RAS2}}$	45	A10	70	GND_D
21	AA3/$\overline{\text{RAS3}}$	46	A11	71	V_{CCD}
22	$\overline{\text{WR}}$	47	A12	72	D3
23	$\overline{\text{RD}}$	48	A13	73	D4
24	XTAL	49	GND_A	74	D5
25	V_{CCQ}	50	V_{CCA}	75	D6

3.2 TQFP Package Mechanical Drawing





Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Datum plane **-H-** is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums **-L-**, **-M-**, and **-N-** to be determined at datum plane **-H-**.
5. Dimensions **S** and **V** to be determined at seating place **-T-**.
6. Dimensions **A** and **B** do not include mold protrusion. Allowable protrusion is 0.25 per side. Dimensions **A** and **B** do include mold mismatch and are determined at datum plane **-H-**.
7. Dimension d does not include dambar protrusion. Dambar protrusion shall not cause the lead width to exceed 0.35 minimum space between protrusion and adjacent lead 0.07.

	Millimeters	
DIM	MIN	MAX
A	28.00 BSC	
A1	14.00 BSC	
B	28.00 BSC	
B1	14.00 BSC	
C	---	1.60
C1	0.05	---
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.10	0.20
S	30.00 BSC	
S1	15.00 BSC	
U	0.09	0.16
V	30.00 REF	
V1	15.00 REF	
W	0.20 REF	
Z	1.00 REF	
q	0	7
q1	0	---
q2	12 REF	

Figure 3-3. DSP56301 Mechanical Information, 208-pin TQFP Package

Table 3-3. DSP56301 MAP-BGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
K9	GND	M2	$\overline{DE}$	N11	V_{CC}
K10	GND	M3	TDO	N12	V_{CC}
K11	GND	M4	TMS	N13	A16
K12	V_{CC}	M5	V_{CC}	N14	A17
K13	V_{CC}	M6	V_{CC}	N15	A20
K14	D3	M7	V_{CC}	N16	NC
K15	D6	M8	V_{CC}	P1	$\overline{TRST}$
K16	D4	M9	V_{CC}	P2	$\overline{BS}$
L1	SRD1 or PD4	M10	V_{CC}	P3	AA0/$\overline{RAS0}$
L2	STD0 or PC5	M11	V_{CC}	P4	CLKOUT
L3	SC02 or PC2	M12	V_{CC}	P5	PINIT/$\overline{NMI}$
L4	SC01 or PC1	M13	A19	P6	GND_P
L5	V_{CC}	M14	A21	P7	$\overline{BG}$
L6	GND	M15	A22	P8	AA3/$\overline{RAS3}$
L7	GND	M16	A23	P9	EXTAL
L8	GND	N1	TCK	P10	A5
L9	GND	N2	TDI	P11	A8
L10	GND	N3	NC	P12	A12
L11	GND	N4	$\overline{BL}$	P13	NC
L12	V_{CC}	N5	$\overline{TA}$	P14	A15
L13	V_{CC}	N6	V_{CC}	P15	NC
L14	D0	N7	V_{CC}	P16	A18
L15	D2	N8	V_{CC}	R1	NC
L16	D1	N9	A1	R2	NC
M1	SC00 or PC0	N10	A2	R3	AA1/$\overline{RAS1}$

Design Considerations 4

4.1 Thermal Design Considerations

An estimate of the chip junction temperature, T_J, in °C can be obtained from this equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A	=	ambient temperature °C
$R_{\theta JA}$	=	package junction-to-ambient thermal resistance °C/W
P_D	=	power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance, as in this equation:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$	=	package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$	=	package junction-to-case thermal resistance °C/W
$R_{\theta CA}$	=	package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB) or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90 percent of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system-level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimates obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system-level model may be appropriate.

A complicating factor is the existence of three common ways to determine the junction-to-case thermal resistance in plastic packages.

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to the point at which the leads attach to the case.

```
M_WRP EQU 19      ; Extended WRaP flag in OMR.
M_SEN EQU 20      ; Stack Extension Enable bit in OMR.
;***************************************************************************
;
;     EQUATES for DSP56301 interrupts
;     Reference: DSP56301 Specifications Revision 3.00
;
;     Last update: November 15 1993 (Debug request & HI32 interrupts)
;                  December 19 1993 (cosmetic - page and opt directives)
;              August 16 1994 (change interrupt addresses to be
;                        relative to I_VEC)
;
;***************************************************************************

       page   132,55,0,0,0
       opt    mex

intequ  ident   1,0

       if     @DEF(I_VEC)
       ;leave user definition as is.
       else
I_VEC  equ    $0
       endif

;--------------------------------------------------------------------------
; Non-Maskable interrupts
;--------------------------------------------------------------------------
I_RESET  EQU  I_VEC+$00   ; Hardware RESET
I_STACK  EQU  I_VEC+$02   ; Stack Error
I_ILL    EQU  I_VEC+$04   ; Illegal Instruction
I_DBG    EQU  I_VEC+$06   ; Debug Request
I_TRAP   EQU  I_VEC+$08   ; Trap
I_NMI    EQU  I_VEC+$0A   ; Non Maskable Interrupt

;--------------------------------------------------------------------------
; Interrupt Request Pins
;--------------------------------------------------------------------------
I_IRQA   EQU  I_VEC+$10   ; IRQA
I_IRQB   EQU  I_VEC+$12   ; IRQB
I_IRQC   EQU  I_VEC+$14   ; IRQC
I_IRQD   EQU  I_VEC+$16   ; IRQD

;--------------------------------------------------------------------------
; DMA Interrupts
;--------------------------------------------------------------------------
I_DMA0   EQU  I_VEC+$18   ; DMA Channel 0
I_DMA1   EQU  I_VEC+$1A   ; DMA Channel 1
I_DMA2   EQU  I_VEC+$1C   ; DMA Channel 2
I_DMA3   EQU  I_VEC+$1E   ; DMA Channel 3
I_DMA4   EQU  I_VEC+$20   ; DMA Channel 4
I_DMA5   EQU  I_VEC+$22   ; DMA Channel 5



;--------------------------------------------------------------------------
; Timer Interrupts
;--------------------------------------------------------------------------
I_TIM0C  EQU  I_VEC+$24   ; TIMER 0 compare
I_TIM0OF EQU  I_VEC+$26   ; TIMER 0 overflow
```