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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	80MHz
Non-Volatile Memory	ROM (9kB)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56301ag80b1

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Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Indicates a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

DSP56301	PCI Bus	Universal Bus	Port B GPIO	Host Port (HP) Reference
Host Interface (HI32)/ Port B Signals	HAD0	HA3	PB0	HP0
	HAD1	HA4	PB1	HP1
	HAD2	HA5	PB2	HP2
	HAD3	HA6	PB3	HP3
	HAD4	HA7	PB4	HP4
	HAD5	HA8	PB5	HP5
	HAD6	HA9	PB6	HP6
	HAD7	HA10	PB7	HP7
	HAD8	HD0	PB8	HP8
	HAD9	HD1	PB9	HP9
	HAD10	HD2	PB10	HP10
	HAD11	HD3	PB11	HP11
	HAD12	HD4	PB12	HP12
	HAD13	HD5	PB13	HP13
	HAD14	HD6	PB14	HP14
	HAD15	HD7	PB15	HP15
	HC0/$\overline{\text{HBE0}}$	HA0	PB16	HP16
	HC1/$\overline{\text{HBE1}}$	HA1	PB17	HP17
	HC2/$\overline{\text{HBE2}}$	HA2	PB18	HP18
	HC3/$\overline{\text{HBE3}}$	Tie to pull-up or V_{CC}	PB19	HP19
	$\overline{\text{HTRDY}}$	$\overline{\text{HDBEN}}$	PB20	HP20
	$\overline{\text{HIRDY}}$	$\overline{\text{HDBDR}}$	PB21	HP21
	$\overline{\text{HDEVSEL}}$	$\overline{\text{HSA}}$K	PB22	HP22
	HLOCK	$\overline{\text{HBS}}$	PB23	HP23
	$\overline{\text{HPAR}}$	$\overline{\text{HDAK}}$	Internal disconnect	HP24
	$\overline{\text{HPERR}}$	HDRQ	Internal disconnect	HP25
	$\overline{\text{HGNT}}$	$\overline{\text{HAEN}}$	Internal disconnect	HP26
	$\overline{\text{HREQ}}$	$\overline{\text{HTA}}$	Internal disconnect	HP27
	$\overline{\text{HSERR}}$	$\overline{\text{HIRQ}}$	Internal disconnect	HP28
	HSTOP	$\overline{\text{HWR}}$/$\overline{\text{HRW}}$	Internal disconnect	HP29
	$\overline{\text{HIDSEL}}$	$\overline{\text{HRD}}$/$\overline{\text{HDS}}$	Internal disconnect	HP30
	$\overline{\text{HFRAME}}$	Tie to pull-up or V_{CC}	Internal disconnect	HP31
	HCLK	Tie to pull-up or V_{CC}	Internal disconnect	HP32
	HAD16	HD8	Internal disconnect	HP33
	HAD17	HD9	Internal disconnect	HP34
	HAD18	HD10	Internal disconnect	HP35
	HAD19	HD11	Internal disconnect	HP36
	HAD20	HD12	Internal disconnect	HP37
	HAD21	HD13	Internal disconnect	HP38
	HAD22	HD14	Internal disconnect	HP39
	HAD23	HD15	Internal disconnect	HP40
	HAD24	HD16	Internal disconnect	HP41
	HAD25	HD17	Internal disconnect	HP42
	HAD26	HD18	Internal disconnect	HP43
	HAD27	HD19	Internal disconnect	HP44
	HAD28	HD20	Internal disconnect	HP45
	HAD29	HD21	Internal disconnect	HP46
	HAD30	HD22	Internal disconnect	HP47
	HAD31	HD23	Internal disconnect	HP48
	$\overline{\text{HRST}}$	$\overline{\text{HRST}}$	Internal disconnect	HP49
	HINTA	HINTA	Internal disconnect	HP50
	PVCL	Leave unconnected	Leave unconnected	PVCL

Note: HPxx is a reference only and is not a signal name. GPIO references formerly designated as HIOxx have been renamed PBxx for consistency with other Freescale DSPs.

Figure 1-2. Host Interface/Port B Detail Signal Diagram

1.1 Power

Table 1-2. Power Inputs

Power Name	Description
V_{CCP}	**PLL Power** Isolated power for the Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
V_{CCQ}	**Quiet Power** Isolated power for the internal processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCA}	**Address Bus Power** Isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCD}	**Data Bus Power** Isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCN}	**Bus Control Power** Isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCH}	**Host Power** Isolated power for the HI32 I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCS}	**ESSI, SCI, and Timer Power** Isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
Note: These designations are package-dependent. Some packages connect all V_{CC} inputs except V_{CCP} to each other internally. On those packages, all power input except V_{CCP} are labeled V_{CC}.	

1.2 Ground

Table 1-3. Grounds

Ground Name	Description
GND_P	**PLL Ground** Ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 µF capacitor located as close as possible to the chip package.
GND_{P1}	**PLL Ground 1** Ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground.
GND_Q	**Quiet Ground** Isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_A	**Address Bus Ground** Isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_D	**Data Bus Ground** Isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.

Table 1-9. Interrupt and Mode Control (Continued)

Signal Name	Type	State During Reset	Signal Description
MODD	Input	Input	**Mode Select D** Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQD during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
IRQD	Input		**External Interrupt Request D** Internally synchronized to CLKOUT. If IRQD is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQD to exit the Wait state. If the processor is in the Stop stand-by state and IRQD is asserted, the processor exits the Stop state. These inputs are 5 V tolerant.
RESET	Input	Input	**Reset** Deassertion of RESET is internally synchronized to the clock out (CLKOUT). When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. If RESET is deasserted synchronous to CLKOUT, exact start-up timing is guaranteed, allowing multiple processors to start synchronously and operate together in “lock-step.” When the RESET signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The RESET signal must be asserted after power-up. This input is 5 V tolerant.

1.7 Host Interface (HI32)

The Host Interface (HI32) provides fast parallel data to a 32-bit port directly connected to the host bus. The HI32 supports a variety of standard buses and directly connects to a PCI bus and a number of industry-standard microcomputers, microprocessors, DSPs, and DMA hardware.

1.7.1 Host Port Usage Considerations

Careful synchronization is required when the system reads multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in **Table 1-10**.

Table 1-10. Host Port Usage Considerations

Action	Description
Asynchronous read of receive byte registers	When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), use interrupts or poll the Receive register Data Full (RXDF) flag that indicates data is available. This assures that the data in the receive byte registers is valid.
Asynchronous write to transmit byte registers	Do not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set, indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers transfer valid data to the Host Receive (HRX) register.

1.9 Enhanced Synchronous Serial Interface 1 (ESSI1)

Table 1-13. Enhanced Synchronous Serial Interface 1 (ESSI1)

Signal Name	Type	State During Reset	Signal Description
SC10	Input or Output	Input	**Serial Control 0** Selection of Synchronous or Asynchronous mode determines function. For Asynchronous mode, this signal is the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is either Transmitter 1 output or Serial I/O Flag 0.
PD0			**Port D 0** The default configuration following reset is GPIO. For PD0, signal direction is controlled through the Port Directions Register (PRR1). The signal can be configured as an ESSI signal SC10 through the Port Control Register (PCR1). This input is 5 V tolerant.
SC11	Input/Output	Input	**Serial Control 1** Selection of Synchronous or Asynchronous mode determines function. For Asynchronous mode, this signal is the receiver frame sync I/O. For Synchronous mode, this signal is either Transmitter 2 output or Serial I/O Flag 1.
PD1	Input or Output		**Port D 1** The default configuration following reset is GPIO. For PD1, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SC11 through PCR1. This input is 5 V tolerant.
SC12	Input/Output	Input	**Serial Control Signal 2** Frame sync for both the transmitter and receiver in Synchronous mode, for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in Synchronous operation).
PD2	Input or Output		**Port D 2** The default configuration following reset is GPIO. For PD2, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SC12 through PCR1. This input is 5 V tolerant.
SCK1	Input/Output	Input	**Serial Clock** Provides the serial bit rate clock for the ESSI interface. Clock input or output can be used by the transmitter and receiver in Synchronous modes, by the transmitter only in Asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3** The default configuration following reset is GPIO. For PD3, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SCK1 through PCR1. This input is 5 V tolerant.

2.2 Absolute Maximum Ratings

Table 2-1. Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CC}	–0.3 to +4.0	V
All input voltages excluding “5 V tolerant” inputs[3]	V_{IN}	GND – 0.3 to V_{CC} + 0.3	V
All “5 V tolerant” input voltages[3]	V_{IN5}	GND – 0.3 to V_{CC} + 3.95	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range	T_J	–40 to +100	°C
Storage temperature	T_{STG}	–55 to +150	°C

Notes:
1. GND = 0 V, V_{CC} = 3.3 V ± 0.3 V, T_J = –40°C to +100°C, CL = 50 pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. **CAUTION**: All “5 V Tolerant” input voltages cannot be more than 3.95 V greater than the supply voltage; this restriction applies to “power on,” as well as during normal operation. In any case, the input voltages must not be higher than 5.75 V. “5 V Tolerant” inputs are inputs that tolerate 5 V.

2.3 Thermal Characteristics

Table 2-2. Thermal Characteristics

Characteristic	Symbol	TQFP Value	PBGA[3] Value	PBGA[4] Value	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	49.5	48.4	25.2	°C/W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	7.2	9	—	°C/W
Thermal characterization parameter	Ψ_{JT}	4.7	5	—	°C/W

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per JEDEC Specification JESD51-3.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. These are simulated values. See note 1 for test board conditions.
4. These are simulated values. The test board has two 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board.

2.4 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics[6]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
28	DMA Request Rate						
	• Data read from HI32, ESSI, SCI	$6 \times T_C$	—	75.0	—	60.0	ns
	• Data write to HI32, ESSI, SCI	$7 \times T_C$	—	87.5	—	70.0	ns
	• Timer	$2 \times T_C$	—	25.0	—	20.0	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$3 \times T_C$	—	37.5	—	30.0	ns
29	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory (DMA source) access address out valid	$4.25 \times T_C + 2.0$	55.1	—	44.5	—	ns

Notes:

1. When using fast interrupts and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. This timing depends on several settings:
   • For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure that the oscillator is stable before programs are executed. Resetting the Stop delay (Operating Mode Register Bit 6 = 0) provides the proper delay. While Operating Mode Register Bit 6 = 1 can be set, it is not recommended, and these specifications do not guarantee timings for that case.
   • For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery is minimal (Operating Mode Register Bit 6 setting is ignored).
   • For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time is defined by the PCTL Bit 17 and Operating Mode Register Bit 6 settings.
   • For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery ends when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.
   • PLC value for PLL disable is 0.
   • The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (that is, for 66 MHz it is 4096/66 MHz = 62 µs). During the stabilization period, T_C, T_H, and T_L is not constant, and their width may vary, so timing may vary as well.
3. Periodically sampled and not 100 percent tested.
4. Value depends on clock source:
   • For an external clock generator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.
   • For an internal oscillator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.
   • When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
5. If PLL does not lose lock.
6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100°C, C_L = 50 pF.
7. WS = number of wait states (measured in clock cycles, number of T_C).
8. Use the expression to compute a maximum value.

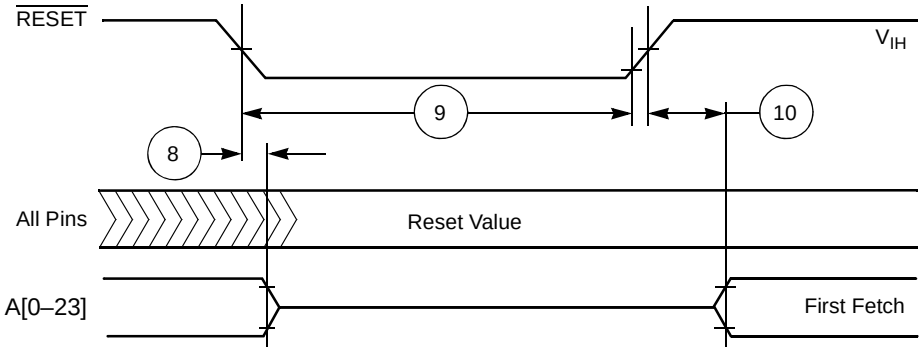
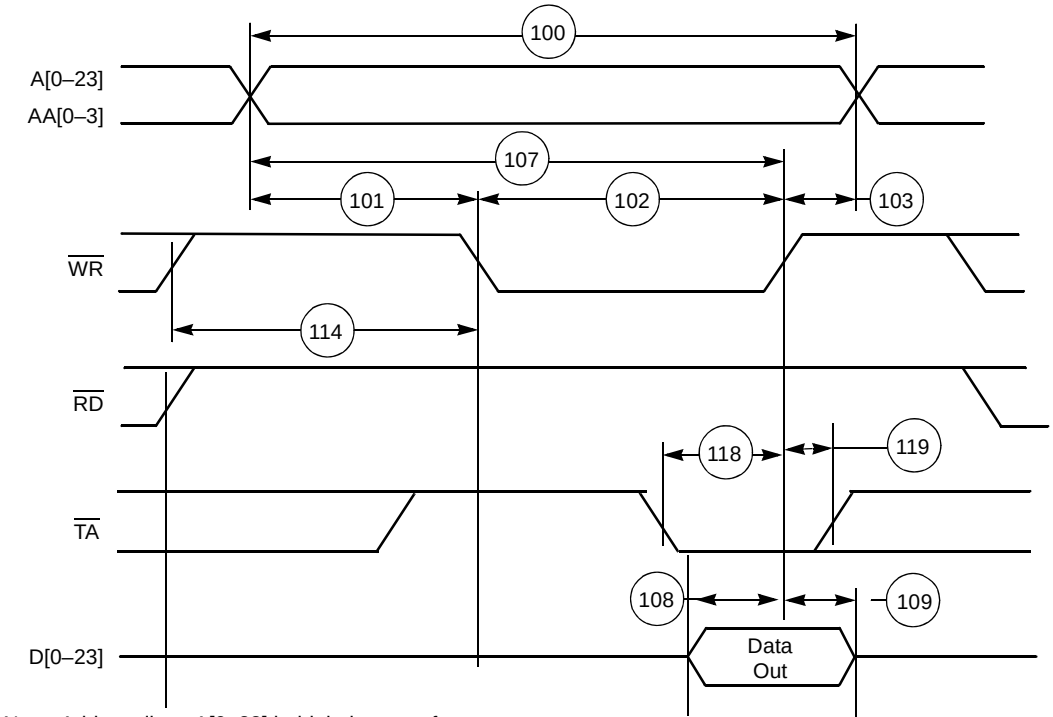


Figure 2-3. Reset Timing



Note: Address lines A[0–23] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-13. SRAM Write Access

Table 2-10. DRAM Page Mode Timings, Three Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction		$4 \times T_C$	50.0	—	40.0	—	ns
	Page mode cycle time for mixed (read and write) accesses	t_{PC}	$3.5 \times T_C$	43.7	—	35.0	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2 \times T_C - 5.7$	—	19.3	—	14.3	ns
133	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 5.7$	—	31.8	—	24.3	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	52.3	—	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	21.0	—	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1–0] = 00 • BRW[1–0] = 01 • BRW[1–0] = 10 • BRW[1–0] = 11	t_{CRP}	 Not supported $3.75 \times T_C - 6.0$ $4.75 \times T_C - 6.0$ $6.75 \times T_C - 6.0$	 — 40.9 53.4 78.4	 — — — —	 — 31.5 41.5 61.5	 — — — —	 ns ns ns ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	8.5	—	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	46.0	—	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	11.6	—	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times TC - 4.0$	5.4	—	3.5	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	23.9	—	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	39.3	—	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	42.6	—	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	36.3	—	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.8$	2.0	—	0.2	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	27.3	—	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	11.3	—	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	39.8	—	31.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$2.5 \times T_C - 5.7$	—	25.6	—	19.3	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	7.9	—	6.0	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56301.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1–0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 2-14. DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	80 MHz		100 MHz		Unit
				Min	Max	Min	Max	
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 6.0$	74.1	—	56.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C - 4.0$	30.4	—	23.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	5.4	—	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$7 \times T_C - 4.0$	83.5	—	66.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$5 \times T_C - 3.8$	58.7	—	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	18.2	—	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RRH}	**80 MHz**: $0.25 \times T_C - 2.6$ **100 MHz**: $0.25 \times T_C - 2.0$	0.5 —	— —	— 0.5	— —	ns ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$6 \times T_C - 4.2$	70.8	—	55.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$9.5 \times T_C - 4.2$	114.6	—	90.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$15.5 \times T_C - 4.5$	189.3	—	150.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$15.75 \times T_C - 4.3$	192.6	—	153.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$14.25 \times T_C - 4.3$	173.8	—	138.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$8.75 \times T_C - 4.0$	105.4	—	83.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C - 4.0$	74.1	—	58.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C - 4.0$	117.9	—	93.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$9.5 \times T_C - 4.3$	114.5	—	90.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	14.8	—	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C - 4.0$	55.4	—	43.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$15.5 \times T_C - 4.0$	189.8	—	151.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	**80 MHz**: $14 \times T_C - 6.5$ **100 MHz**: $14 \times T_C - 5.7$	— —	168.5 —	— —	— 134.3	ns ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	9.1	—	6.0	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for an out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

2.5.5.3 Synchronous Timings (SRAM)

Table 2-15. External Bus Synchronous Timings (SRAM Access)[3]

No.	Characteristics	Expression[1,2]	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
196	CLKOUT high to $\overline{BS}$ assertion	$0.25 \times T_C$ +5.2/–0.5	2.6	8.3	2.0	7.7	ns
197	CLKOUT high to $\overline{BS}$ deassertion	$0.75 \times T_C$ +4.2/–1.0	8.4	13.6	6.5	11.7	ns
198	CLKOUT high to address, and AA valid[4]	$0.25 \times T_C + 2.5$	—	5.6	—	5.0	ns
199	CLKOUT high to address, and AA invalid[4]	$0.25 \times T_C - 0.7$	2.4	—	1.8	—	ns
200	$\overline{TA}$ valid to CLKOUT high (setup time)		5.8	—	4.0	—	ns
201	CLKOUT high to $\overline{TA}$ invalid (hold time)		0.0	—	0.0	—	ns
202	CLKOUT high to data out active	$0.25 \times T_C$	3.1	—	2.5	—	ns
203	CLKOUT high to data out valid	**80 MHz**: $0.25 \times T_C + 4.5$ **100 MHz**: $0.25 \times T_C + 4.0$	— —	7.6 —	— —	— 6.5	ns ns
204	CLKOUT high to data out invalid	$0.25 \times T_C$	3.1	—	2.5	—	ns
205	CLKOUT high to data out high impedance	**80 MHz**: $0.25 \times T_C + 0.5$ **100 MHz**: $0.25 \times T_C$	— —	3.6 —	— —	— 2.5	ns ns
206	Data in valid to CLKOUT high (setup)		5.0	—	4.0	—	ns
207	CLKOUT high to data in invalid (hold)		0.0	—	0.0	—	ns
208	CLKOUT high to $\overline{RD}$ assertion	maximum: $0.75 \times T_C + 2.5$	10.4	 11.9	6.7	 10.0	ns ns
209	CLKOUT high to $\overline{RD}$ deassertion		0.0	4.5	0.0	4.0	ns
210	CLKOUT high to $\overline{WR}$ assertion[2]	$0.5 \times T_C + 4.3$ [WS = 1 or WS ≥ 4] [2 ≤ WS ≤ 3]	7.6 1.3	10.6 4.8	4.5 0.0	9.3 4.3	ns ns
211	CLKOUT high to $\overline{WR}$ deassertion		0.0	4.3	0.0	3.8	ns

Notes:
1. WS is the number of wait states specified in the BCR.
2. If WS > 1, $\overline{WR}$ assertion refers to the next rising edge of CLKOUT.
3. External bus synchronous timings should be used only for reference to the clock and *not* for relative timings.
4. T198 and T199 are valid for Address Trace mode if the ATE bit in the Operating Mode Register is set. Use the status of $\overline{BR}$ (See T212) to determine whether the access referenced by A[0–23] is internal or external in this mode.

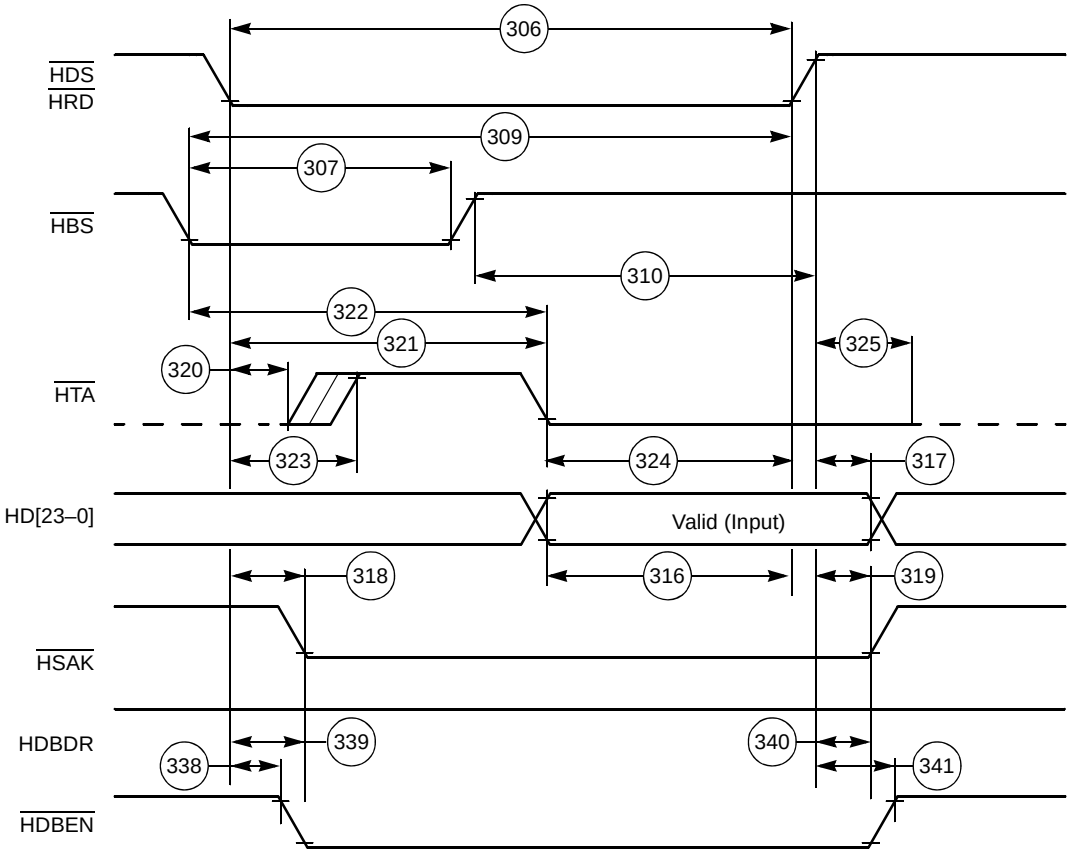


Figure 2-33. Write Timing

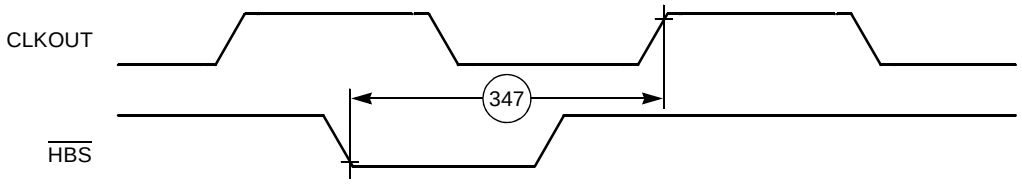


Figure 2-34. $\overline{\text{HBS}}$ Synchronous Timing

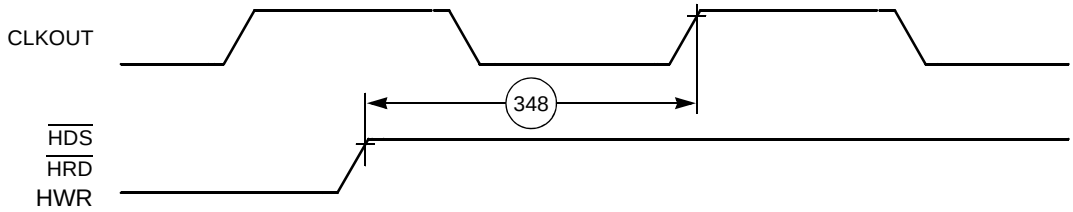


Figure 2-35. Data Strobe Synchronous Timing

Table 2-20. PCI Mode Timing Parameters[1]

No.	Characteristic[10]	Symbol	80 MHz		100 MHz		Unit
			Min	Max	Min	Max	
349	HCLK to Signal Valid Delay—Bussed Signals	t_{VAL}	2.0	11.0	2.0	11.0	ns
350	HCLK to Signal Valid Delay—Point to Point	$t_{VAL(ptp)}$	2.0	12.0	2.0	12.0	ns
351	Float to Active Delay	t_{ON}	2.0	—	2.0	—	ns
352	Active to Float Delay	t_{OFF}	—	28.0	—	28.0	ns
353	Input Set Up Time to HCLK—Bussed Signals	t_{SU}	7.0	—	7.0	—	ns
354	Input Set Up Time to HCLK—Point to Point	$t_{SU(ptp)}$	10.0, 12.0	—	10.0, 12.0	—	ns
355	Input Hold Time from HCLK	t_{H}	0.0	—	0.0	—	ns
356	Reset Active Time After Power Stable	t_{RST}	1.0	—	1.0	—	ms
357	Reset Active Time After HCLK Stable	$t_{RST-CLK}$	100.0	—	100.0	—	µs
358	Reset Active to Output Float Delay	$t_{RST-OFF}$	—	40.0	—	40.0	ns
359	HCLK Cycle Time	t_{CYC}	30.0	—	30.0	—	ns
360	HCLK High Time	t_{HIGH}	11.0	—	11.0	—	ns
361	HCLK Low Time	t_{LOW}	11.0	—	11.0	—	ns

Notes:
1. For standard PCI timing, see the *PCI Local Bus Specification*, Rev. 2.0, especially Chapters 3 and 4.
2. The HI32 supports these timings for a PCI bus operating at 33 MHz for a DSP clock frequency of 56 MHz and above. The DSP core operating frequency should be greater than 5/3 of the PCI bus frequency to maintain proper PCI operation.
3. $\overline{\text{HGNT}}$ has a setup time of 10 ns. $\overline{\text{HREQ}}$ has a setup time of 12 ns.

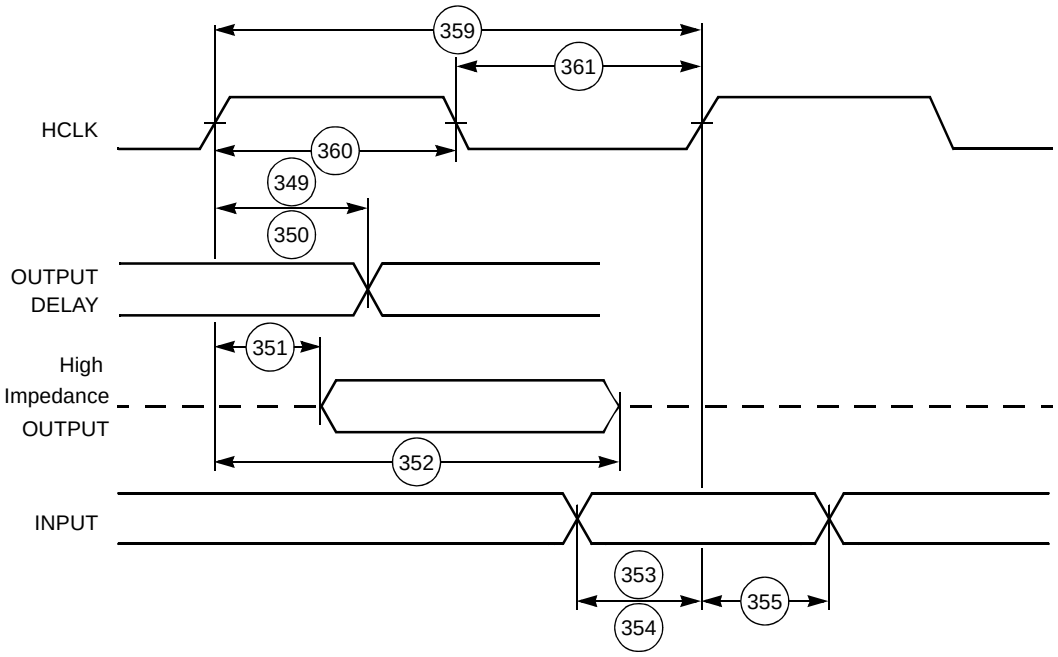


Figure 2-36. PCI Timing

Packaging 3

This section provides information on the available packages for the DSP56301, including diagrams of the package pinouts and tables showing how the signals discussed in **Section 1** are allocated for each package. The DSP56301 is available in two package types:

- 208-pin Thin Quad Flat Pack (TQFP)
- 252-pin Molded Array Process-Ball Grid Array (MAP-BGA)

Note: Both packages are available in lead-bearing and lead-free versions. Switching a design from a lead-bearing package device to a lead-free package device may require a change in the board manufacturing process. The lead-free package requires a higher solder flow temperature than the lead-bearing device. Refer to *Lead-Free BGA Solder Joint Assembly Evaluation* (EB635) for manufacturing considerations when incorporating lead-free package devices into a design.

Table 3-1. DSP56301 TQFP Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	AA0/$\overline{\text{RAS0}}$	26	EXTAL	51	A14
2	AA1/$\overline{\text{RAS1}}$	27	GND_Q	52	A15
3	V_{CCN}	28	$\overline{\text{BCLK}}$	53	NC
4	GND_N	29	A0	54	NC
5	CLKOUT	30	A1	55	A16
6	BCLK	31	GND_A	56	A17
7	$\overline{\text{CAS}}$	32	V_{CCA}	57	GND_A
8	$\overline{\text{TA}}$	33	A2	58	V_{CCA}
9	PINIT/$\overline{\text{NMI}}$	34	A3	59	A18
10	$\overline{\text{RESET}}$	35	A4	60	A19
11	V_{CCP}	36	A5	61	A20
12	PCAP	37	GND_A	62	A21
13	GND_P	38	V_{CCA}	63	GND_A
14	GND_{P1}	39	A6	64	V_{CCA}
15	$\overline{\text{BB}}$	40	A7	65	A22
16	$\overline{\text{BG}}$	41	A8	66	A23
17	$\overline{\text{BR}}$	42	A9	67	D0
18	V_{CCN}	43	GND_A	68	D1
19	GND_N	44	V_{CCA}	69	D2
20	AA2/$\overline{\text{RAS2}}$	45	A10	70	GND_D
21	AA3/$\overline{\text{RAS3}}$	46	A11	71	V_{CCD}
22	$\overline{\text{WR}}$	47	A12	72	D3
23	$\overline{\text{RD}}$	48	A13	73	D4
24	XTAL	49	GND_A	74	D5
25	V_{CCQ}	50	V_{CCA}	75	D6

Table 3-2. DSP56301 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND_N	19	HAD14	152	HAEN	149
GND_P	13	HAD15	151	$\overline{HBE0}$	163
GND_Q	27	HAD16	127	$\overline{HBE1}$	150
GND_Q	78	HAD17	126	$\overline{HBE2}$	128
GND_Q	132	HAD18	125	$\overline{HBE3}$	117
GND_Q	183	HAD19	124	$\overline{HBS}$	140
GND_Q	183	HAD2	171	HC0	163
GND_S	180	HAD20	121	HC1	150
GND_S	194	HAD21	120	HC2	128
HA0	163	HAD22	119	HC3	117
HA1	150	HAD23	118	HCLK	148
HA10	164	HAD24	116	HD0	162
HA2	128	HAD25	115	HD1	161
HA3	173	HAD26	114	HD10	125
HA4	172	HAD27	113	HD11	124
HA5	171	HAD28	110	HD12	121
HA6	170	HAD29	109	HD13	120
HA7	167	HAD3	170	HD14	119
HA8	166	HAD30	108	HD15	118
HA9	165	HAD31	107	HD16	116
HAD0	173	HAD4	167	HD17	115
HAD1	172	HAD5	166	HD18	114
HAD10	160	HAD6	165	HD19	113
HAD11	159	HAD7	164	HD2	160
HAD12	154	HAD8	162	HD20	110
HAD13	153	HAD9	161	HD21	109

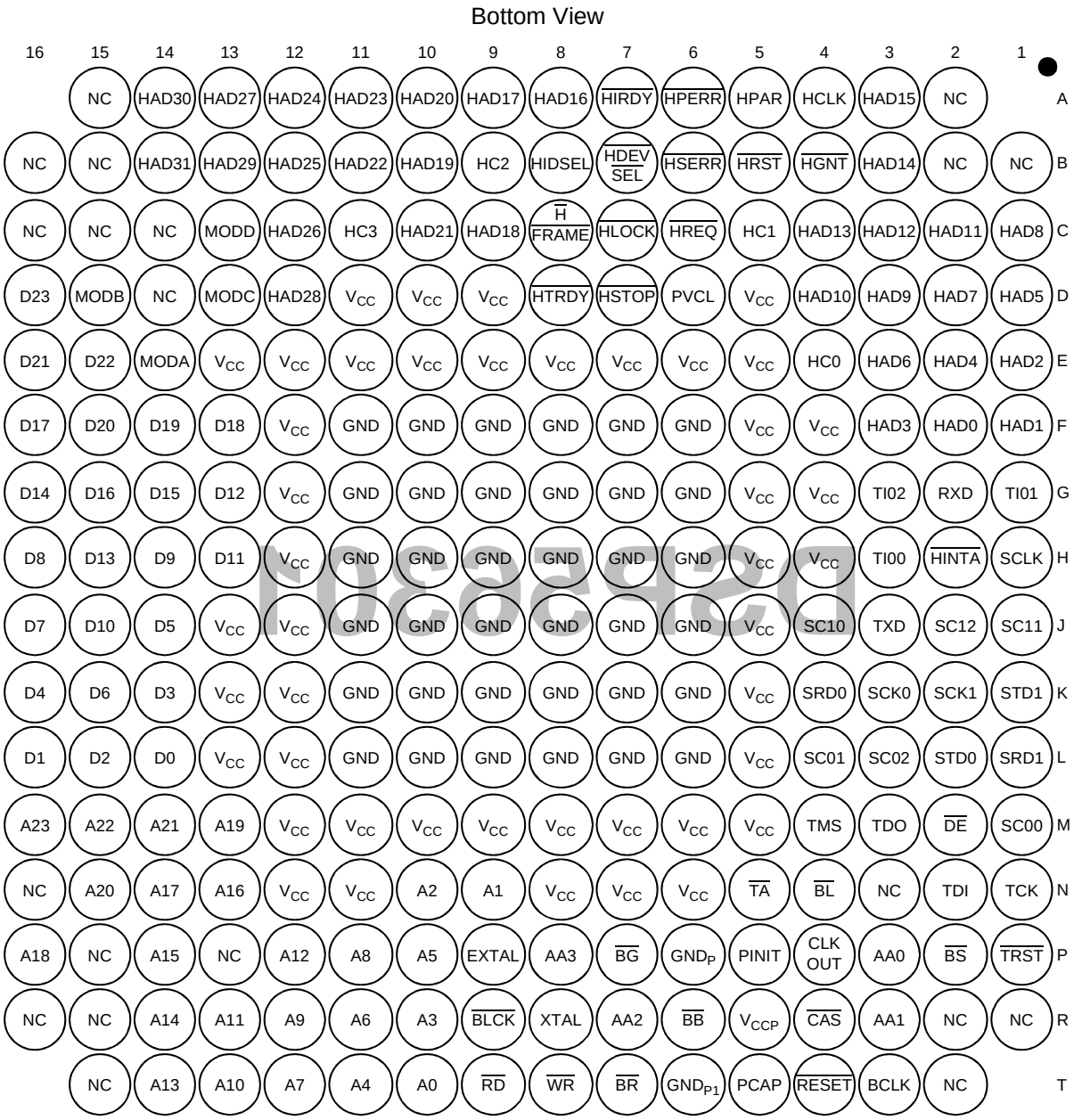


Figure 3-5. DSP56301 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

Table 3-4. DSP56301 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
NC	R15	PB6	E3	$\overline{\text{RAS3}}$	P8
NC	R16	PB7	D2	$\overline{\text{RD}}$	T9
NC	T2	PB8	C1	$\overline{\text{RESET}}$	T4
NC	T15	PB9	D3	RXD	G2
$\overline{\text{NMI}}$	P5	PC0	M1	SC00	M1
PB0	F2	PC1	L4	SC01	L4
PB1	F1	PC2	L3	SC02	L3
PB10	D4	PC3	K3	SC10	J4
PB11	C2	PC4	K4	SC11	J1
PB12	C3	PC5	L2	SC12	J2
PB13	C4	PCAP	T5	SCK0	K3
PB14	B3	PD0	J4	SCK1	K2
PB15	A3	PD1	J1	SCLK	H1
PB16	E4	PD2	J2	SRD0	K4
PB17	C5	PD3	K2	SRD1	L1
PB18	B9	PD4	L1	STD0	L2
PB19	C11	PD5	K1	STD1	K1
PB2	E1	PE0	G2	$\overline{\text{TA}}$	N5
PB20	D8	PE1	J3	TCK	N1
PB21	A7	PE2	H1	TDI	N2
PB22	B7	PINIT	P5	TDO	M3
PB23	C7	PVCL	D6	TIO0	H3
PB3	F3	$\overline{\text{RAS0}}$	P3	TIO1	G1
PB4	E2	$\overline{\text{RAS1}}$	R3	TIO2	G3
PB5	D1	$\overline{\text{RAS2}}$	R7	TMS	M4

```
M_STRQ EQU 1   ; Slave Transmit Data Request
M_SRRQ EQU 2   ; Slave Receive Data Request
M_HF02 EQU $38 ; Host Flag 0-2 Mask
M_HF0 EQU 3    ; Host Flag 0
M_HF1 EQU 4    ; Host Flag 1
M_HF2 EQU 5    ; Host Flag 2

;       DSP PCI Status Register Bit Flags

M_MWS EQU 0    ; PCI Master Wait States
M_MTRQ EQU 1   ; PCI Master Transmit Data Request
M_MRRQ EQU 2   ; PCI Master Receive Data Request
M_MARQ EQU 4   ; PCI Master Address Request
M_APER EQU 5      ; PCI Address Parity Error
M_DPER EQU 6      ; PCI Data Parity Error
M_MAB EQU 7      ; PCI Master Abort
M_TAB EQU 8      ; PCI Target Abort
M_TDIS EQU 9      ; PCI Target Disconnect
M_TRTY EQU 10     ; PCI Target Retry
M_TO EQU 11     ; PCI Time Out Termination
M_RDC EQU $3F0000; Remaining Data Count Mask (RDC5-RDC0)
M_RDC0 EQU 16     ; Remaining Data Count  0
M_RDC1 EQU 17     ; Remaining Data Count  1
M_RDC2 EQU 18     ; Remaining Data Count  2
M_RDC3 EQU 19     ; Remaining Data Count  3
M_RDC4 EQU 20     ; Remaining Data Count  4
M_RDC5 EQU 21     ; Remaining Data Count  5
M_HACT EQU 23     ; Hi32 Active


;---------------------------------------------------------------------
;
;       EQUATES for Serial Communications Interface (SCI)
;
;---------------------------------------------------------------------

;       Register Addresses

M_STXH EQU $FFFF97; SCI Transmit Data Register (high)
M_STXM EQU $FFFF96; SCI Transmit Data Register (middle)
M_STXL EQU $FFFF95; SCI Transmit Data Register (low)
M_SRXH EQU $FFFF9A; SCI Receive Data Register (high)
M_SRXM EQU $FFFF99; SCI Receive Data Register (middle)
M_SRXL EQU $FFFF98; SCI Receive Data Register (low)
M_STXA EQU $FFFF94; SCI Transmit Address Register
M_SCR EQU $FFFF9C; SCI Control Register
M_SSR EQU $FFFF93; SCI Status Register
M_SCCR EQU $FFFF9B; SCI Clock Control Register

;       SCI Control Register Bit Flags

M_WDS EQU $7     ; Word Select Mask (WDS0-WDS3)
M_WDS0 EQU 0      ; Word Select 0
M_WDS1 EQU 1      ; Word Select 1
M_WDS2 EQU 2      ; Word Select 2
M_SSFTD EQU 3      ; SCI Shift Direction
M_SBK EQU 4      ; Send Break
M_WAKE EQU 5      ; Wakeup Mode Select
M_RWU EQU 6      ; Receiver Wakeup Enable
M_WOMS EQU 7      ; Wired-OR Mode Select
```

```
M_D5L EQU $C00000; DMA5 Interrupt priority Level Mask
M_D5L0 EQU 22     ; DMA5 Interrupt Priority Level (low)
M_D5L1 EQU 23     ; DMA5 Interrupt Priority Level (high)


;       Interrupt Priority Register Peripheral (IPRP)

M_HPL EQU $3     ; Host Interrupt Priority Level Mask
M_HPL0 EQU 0      ; Host Interrupt Priority Level (low)
M_HPL1 EQU 1      ; Host Interrupt Priority Level (high)
M_S0L EQU $C     ; SSI0 Interrupt Priority Level Mask
M_S0L0 EQU 2      ; SSI0 Interrupt Priority Level (low)
M_S0L1 EQU 3      ; SSI0 Interrupt Priority Level (high)
M_S1L EQU $30    ; SSI1 Interrupt Priority Level Mask
M_S1L0 EQU 4      ; SSI1 Interrupt Priority Level (low)
M_S1L1 EQU 5      ; SSI1 Interrupt Priority Level (high)
M_SCL EQU $C0    ; SCI  Interrupt Priority Level  Mask
M_SCL0 EQU 6      ; SCI  Interrupt Priority Level  (low)
M_SCL1 EQU 7      ; SCI  Interrupt Priority Level  (high)
M_T0L EQU $300   ; TIMER Interrupt Priority Level Mask
M_T0L0 EQU 8      ; TIMER Interrupt Priority Level (low)
M_T0L1 EQU 9      ; TIMER Interrupt Priority Level (high)


;---------------------------------------------------------------------
;
;       EQUATES for TIMER
;
;---------------------------------------------------------------------

;       Register Addresses Of TIMER0

M_TCSR0 EQU $FFFF8F; TIMER0 Control/Status Register
M_TLR0 EQU $FFFF8E; TIMER0 Load Reg
M_TCPR0 EQU $FFFF8D; TIMER0 Compare Register
M_TCR0 EQU $FFFF8C ; TIMER0 Count Register

;       Register Addresses Of TIMER1

M_TCSR1 EQU $FFFF8B; TIMER1 Control/Status Register
M_TLR1 EQU $FFFF8A; TIMER1 Load Reg
M_TCPR1 EQU $FFFF89; TIMER1 Compare Register
M_TCR1 EQU $FFFF88; TIMER1 Count Register


;       Register Addresses Of TIMER2

M_TCSR2 EQU $FFFF87; TIMER2 Control/Status Register
M_TLR2 EQU $FFFF8; TIMER2 Load Reg
M_TCPR2 EQU $FFFF85; TIMER2 Compare Register
M_TCR2 EQU $FFFF84 ; TIMER2 Count Register
M_TPLR EQU $FFFF83 ; TIMER Prescaler Load Register
M_TPCR EQU $FFFF82 ; TIMER Prescalar Count Register


;       Timer Control/Status Register Bit Flags

M_TE EQU 0      ; Timer Enable
M_TOIE EQU 1      ; Timer Overflow Interrupt Enable
M_TCIE EQU 2      ; Timer Compare Interrupt Enable
```